FAIRCHILD SEMICONDUCTOR®

July 2009

# FDS8449_F085

## 40V N-Channel PowerTrench® MOSFET

### General Description

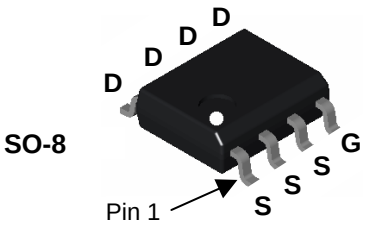
These N-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

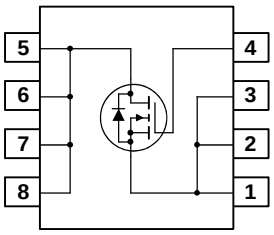
### Application

- Inverter
- Power Supplies

### Features

- 7.6 A, 40V $R_{DS(on)}$ = 29mΩ @ $V_{GS}$ = 10V
  $R_{DS(on)}$ = 36mΩ @ $V_{GS}$ = 4.5V
- High power handling capability in a widely used surface mount package
- RoHS compliant
- Qualified to AEC Q101




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 40 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | 7.6 | A |
| | – Pulsed | | 50 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 2.5 | W |
| | | (Note 1b) | 1 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 50 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1b) | 125 | |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 25 | |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| FDS8449 | FDS8449_F085 | 13'' | 12mm | 2500 units |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain-Source Avalanche Ratings (Note 3)** | | | | | | |
| $E_{AS}$ | Drain-Source Avalanche Energy | $V_{DD}$ = 40 V, $I_D$ = 7.3 A, L = 1 mH | | | 27 | mJ |
| $I_{AS}$ | Drain-Source Avalanche Current | | | 7.3 | | A |
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 40 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | 34 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 32 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics (Note 2)** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1 | 1.9 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | –5 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 10 V, $I_D$ = 7.6 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 6.8 A<br>$V_{GS}$= 10 V, $I_D$ = 7.6 A, $T_J$=125°C | | 21<br>26<br>29 | 29<br>36<br>43 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 7.6 A | | 21 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 760 | | pF |
| $C_{oss}$ | Output Capacitance | | | 100 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 60 | | pF |
| $R_G$ | Gate Resistance | f = 1.0 MHz | | 1.2 | | Ω |
| **Switching Characteristics (Note 2)** | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 20 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 9 | 18 | ns |
| $t_r$ | Turn–On Rise Time | | | 5 | 10 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 23 | 17 | ns |
| $t_f$ | Turn–Off Fall Time | | | 3 | 6 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 20 V, $I_D$ = 7.6 A, $V_{GS}$ = 5 V | | 7.7 | 11 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 2.4 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 2.8 | | nC |
| **Drain–Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.1 A (Note 2) | | 0.76 | 1.2 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = 7.6 A, $d_{iF}/d_t$ = 100 A/μs | | 17 | | nS |
| $Q_{rr}$ | Diode Reverse Recovery Charge | | | 7 | | nC |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 50°C/W when mounted on a 1in$^2$ pad of 2 oz copper

b) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

**2** Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. BV(avalanche) Single-Pulse rating is guaranteed if device is operated within the UIS SOA boundary of the device.

## Typical Characteristics

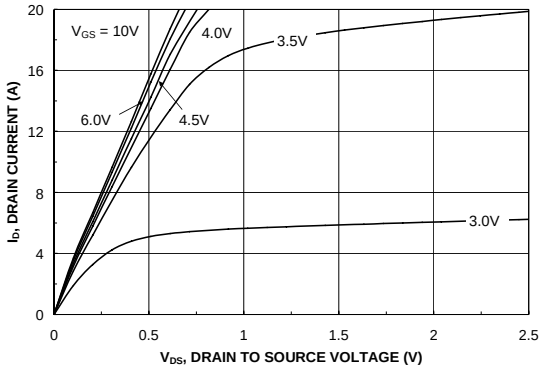



**Figure 1. On-Region Characteristics.**

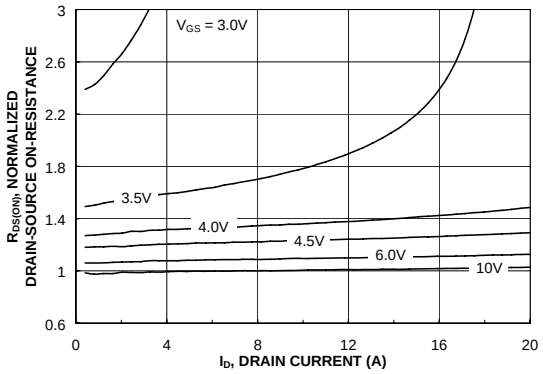



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

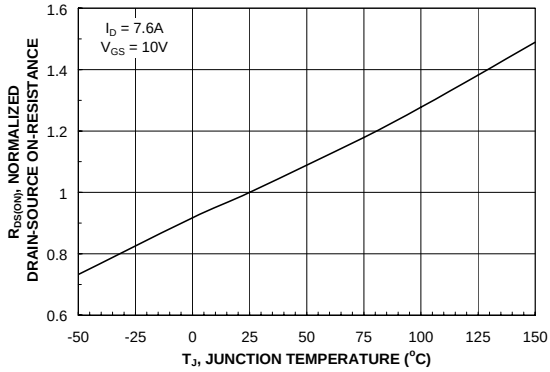



**Figure 3. On-Resistance Variation with Temperature.**

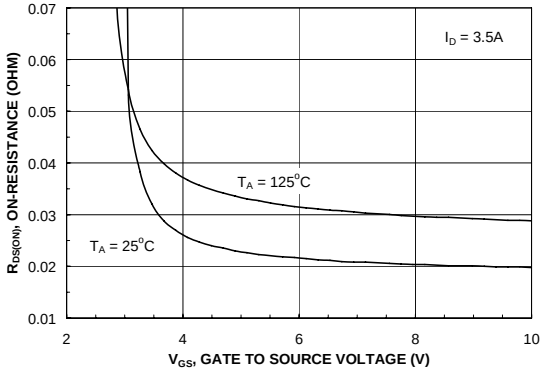



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

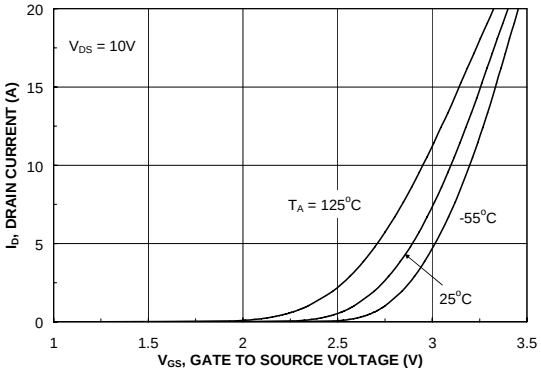



**Figure 5. Transfer Characteristics.**

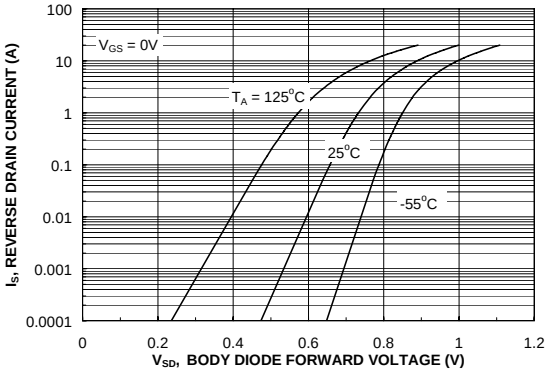



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

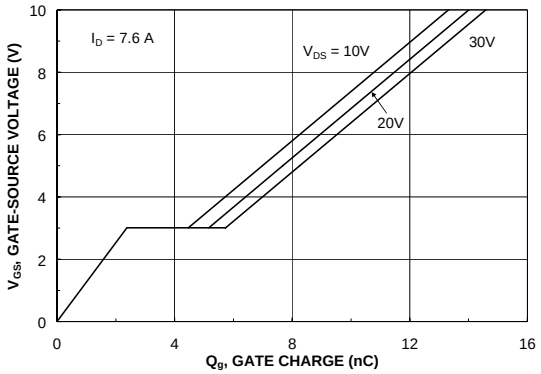



**Figure 7. Gate Charge Characteristics.**

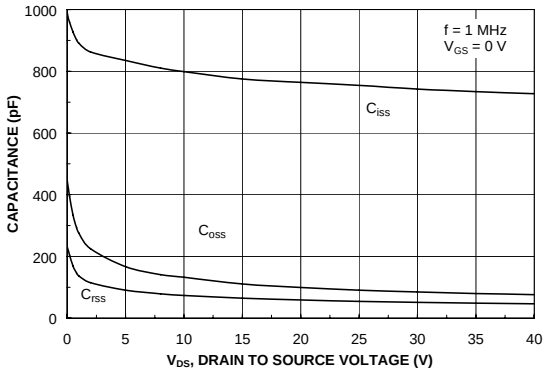



**Figure 8. Capacitance Characteristics.**

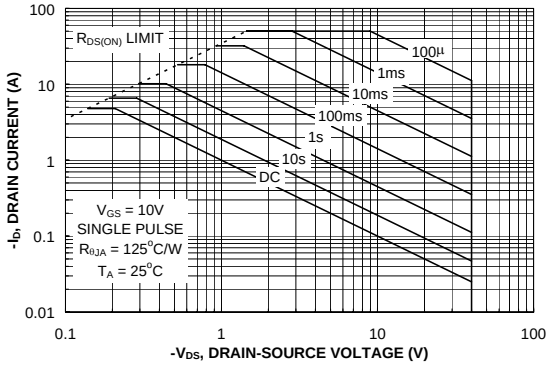



**Figure 9. Maximum Safe Operating Area.**

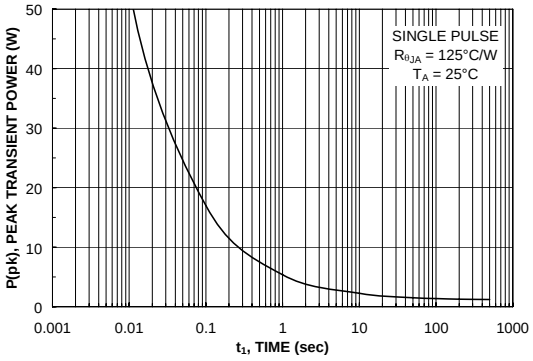



**Figure 10. Single Pulse Maximum Power Dissipation.**

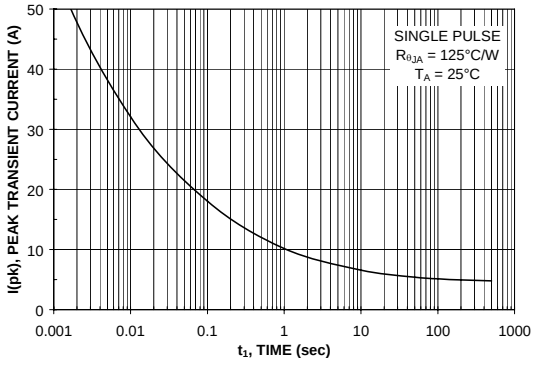



**Figure 11. Single Pulse Maximum Peak Current.**

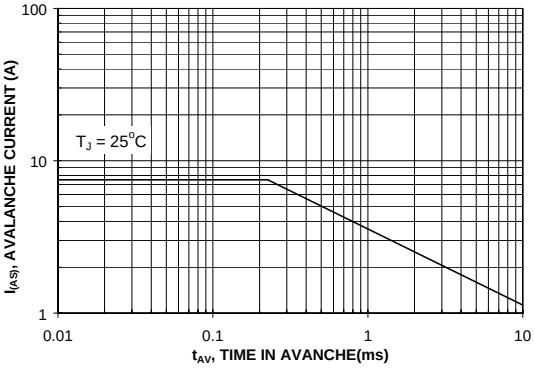



**Figure 12. Unclamped Inductive Switching Capability.**

## Typical Characteristics

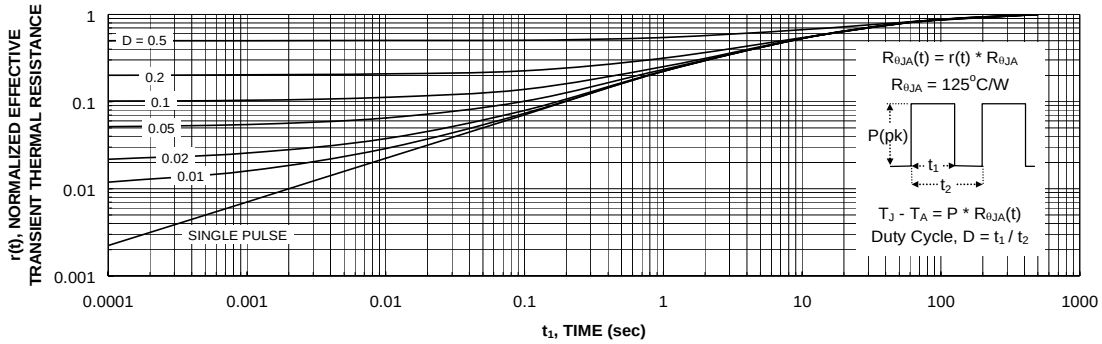



**Figure 13. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1c.**
**Transient thermal response will change depending on the circuit board design.**

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