

## FDR856P

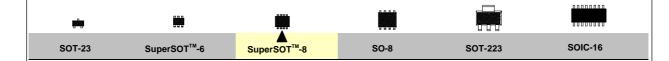
# P-Channel Logic Level Enhancement Mode Field Effect Transistor

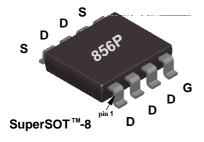
## **General Description**

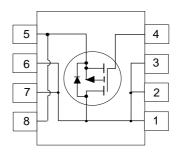
SuperSOT™-8 P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as battery powered circuits or portable electronics where low in-line power loss, fast switching and resistance to transients are needed.

## **Features**

- = 6.3 A, -30 V,  $R_{DS(ON)}$  =0.025  $\Omega$  @  $V_{GS}$  = -10 V  $R_{DS(ON)}$  =0.040  $\Omega$  @  $V_{GS}$  = -4.5 V.
- SuperSOT<sup>™</sup>-8 package: small footprint (40% less than SO-8);low profile (1mm thick);maximum power comperable to SO-8.
- High density cell design for extremely low R<sub>DS(ON)</sub>.







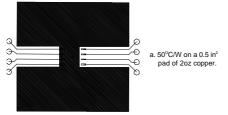
# **Absolute Maximum Ratings** $T_A = 25^{\circ}C$ unless other wise noted

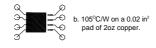
Symbol	Parameter		FDR856P	Units	
/ <sub>DSS</sub>	Drain-Source Voltage		-30	V	
/ <sub>GSS</sub>	Gate-Source Voltage - Continuous		±20	V	
)	Maximum Drain Current - Continuou	IS (Note 1a)	-5.1	A	
	- Pulsed		-50		
D D	Maximum Power Dissipation	(Note 1a)	1.8	W	
		(Note 1b)	1		
		(Note 1c)	0.9		
J,T <sub>STG</sub>	Operating and Storage Temperature	Range	-55 to 150	°C	
THERMA	L CHARACTERISTICS			·	
R <sub>OJA</sub>	Thermal Resistance, Junction-to-Am	nbient (Note 1a)	50	°C/W	
R <sub>⊕JC</sub>	Thermal Resistance, Junction-to-Ca	SE (Note 1)	25	°C/W	

Symbol	Parameter	Conditions	Min	Тур	Max	Units
OFF CHAR	ACTERISTICS					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \ I_{D} = -250 \ \mu\text{A}$	-30			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	$I_D = -250 \mu A$ , Referenced to 25 °C		-15		mV /°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V}, \ V_{GS} = 0 \text{ V}$			-1	μΑ
		T <sub>J</sub> = 55°C			-10	μΑ
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
I <sub>GSSR</sub>	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
	CTERISTICS (Note 2)	·	•			
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-1	-1.5	-3	V
$\Delta V_{GS(th)}/\Delta T_{J}$	Gate Threshold Voltage Temp. Coefficient	I <sub>D</sub> = -250 μA, Referenced to 25 °C		3		mV /°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = -10 \text{ V}, I_{D} = -6.3 \text{ A}$		0.022	0.025	Ω
		T <sub>J</sub> =125°C		0.03	0.042	
		$V_{GS} = -4.5 \text{ V}, I_{D} = -5 \text{ A}$		0.033	0.04	1
I <sub>D(ON)</sub>	On-State Drain Current	$V_{GS} = -10 \text{ V}, \ V_{DS} = -5 \text{ V}$	-50			Α
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = -10 \text{ V}, I_{D} = -6.3 \text{ A}$		15		S
DYNAMIC	CHARACTERISTICS	•				
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V},$		1370		pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		740		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			220		pF
SWITCHING	CHARACTERISTICS (Note 2)					
t <sub>D(on)</sub>	Tum - On Delay Time	$V_{DS} = -15 \text{ V}, I_{D} = -1 \text{ A}$		7	14	ns
t <sub>r</sub>	Turn - On Rise Time	$V_{GS} = -10 \text{ V}$ , $R_{G} = 6 \Omega$		12	19	ns
t <sub>D(off)</sub>	Turn - Off Delay Time			80	100	ns
t,	Turn - Off Fall Time			130	160	ns
$Q_g$	Total Gate Charge	$V_{DS} = -15 \text{ V}, I_{D} = -6.3 \text{ A},$		22	31	nC
$Q_{gs}$	Gate-Source Charge	V <sub>GS</sub> = -10 V		3.8		nC
$Q_{gd}$	Gate-Drain Charge			8.7		nC
DRAIN-SOL	IRCE DIODE CHARACTERISTICS AND MAX	(IMUM RATINGS				
Is	Maximum Continuous Drain-Source Diode Fo			-1.3	Α	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -1.3 \text{ A} \text{ (Note 2)}$		-0.73	-1.2	V

Notes:

1. R<sub>aw</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>avc</sub> is guaranteed by design while R<sub>avc</sub> is determined by the user's board design.







Scale 1 : 1 on letter size paper 2. Pulse Test: Pulse Width  $\leq$  300 $\mu$ s, Duty Cycle  $\leq$  2.0%.

# **Typical Electrical Characteristics**

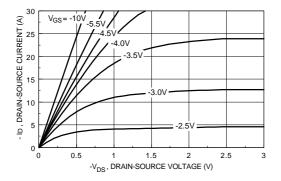


Figure 1. On-Region Characteristics.

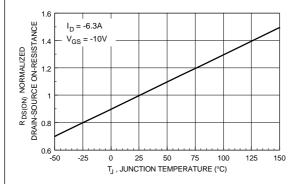


Figure 3. On-Resistance Variation with Temperature.

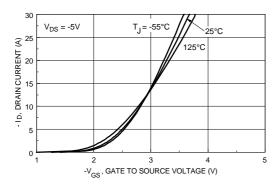


Figure 5 . Transfer Characteristics.

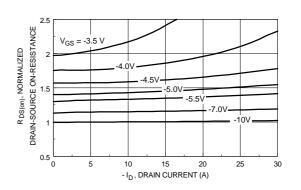


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

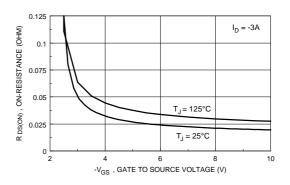


Figure 4 . On Resistance Variation with Gate-to-Source Voltage.

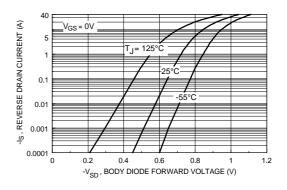


Figure 6 . Body Diode Forward Voltage Variation with Source Current and Temperature.

# Typical Electrical Characteristics (continued)

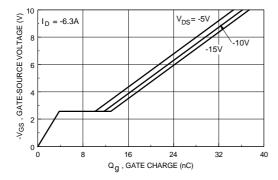


Figure 7. Gate Charge Characteristics.

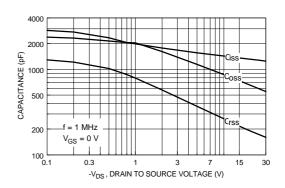


Figure 8. Capacitance Characteristics.

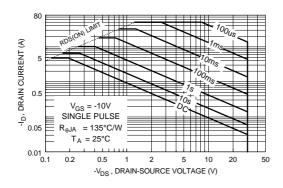


Figure 9. Maximum Safe Operating Area.

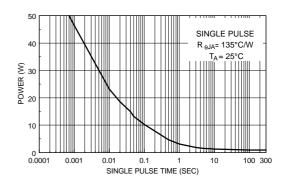


Figure 10. Single Pulse Maximum Power Dissipation.

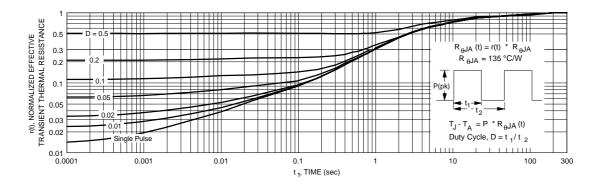
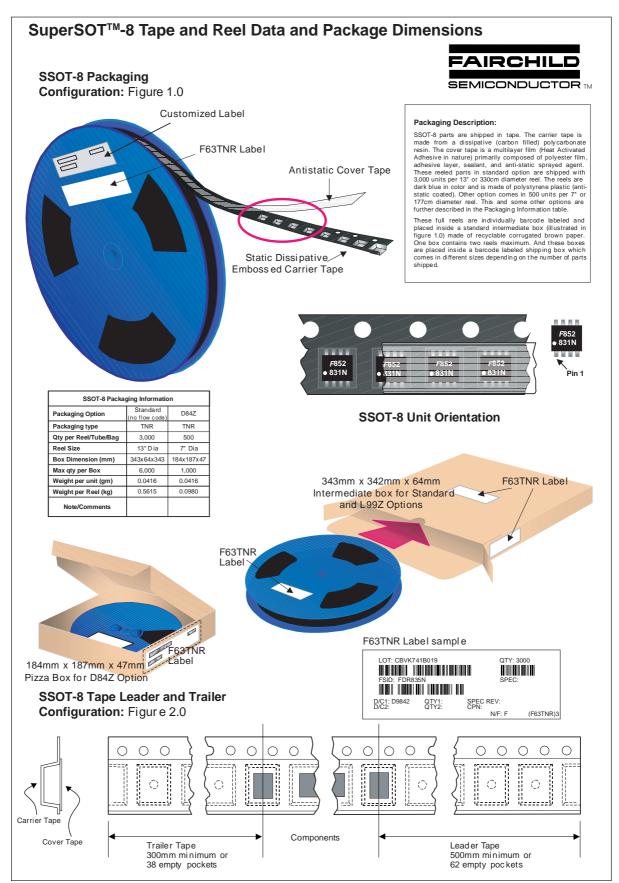


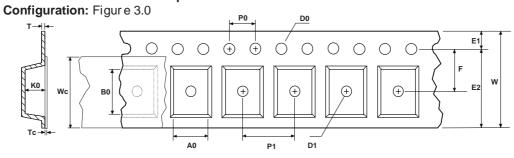
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.





# **SSOT-8 Embossed Carrier Tape**



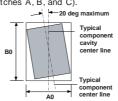
User Direction of Feed	

Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
<b>SSOT-8</b> (12mm)	4.47 +/-0.10	5.00 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.50 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.280 +/-0.150	9.5 +/-0.025	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

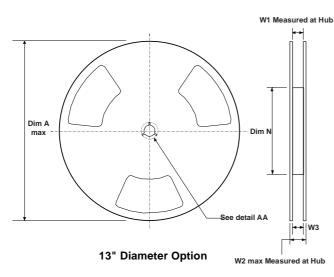


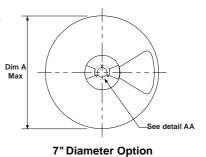
Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

# SSOT-8 Reel Configuration: Figur e 4.0



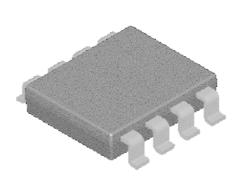


# Dim D min DETAIL AA

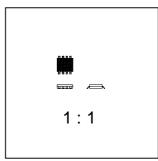
	Dimensions are in inches and millimeters								
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	5.906 150	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

# SuperSOT<sup>™</sup>-8 Tape and Reel Data and Package Dimensions, continued

# SuperSOT™-8 (FS PKG Code 34, 35)



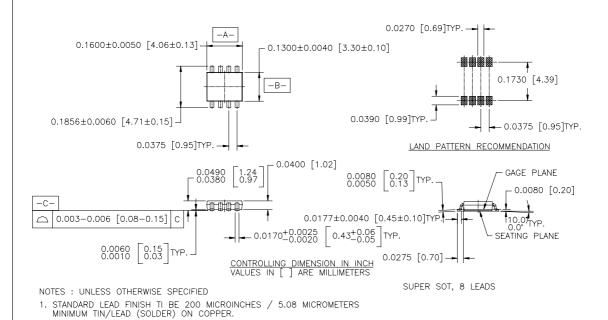
2. NO JEDEC REGISTRATION AS JAN. 1996



Scale 1:1 on letter size paper

Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 0.0416



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