

FEATURES

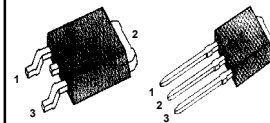
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- 175°C Operating Temperature
- Lower Leakage Current : 10 μA (Max.) @ V_{DS} = 200V
- Lower R_{DS(ON)} : 0.609 Ω (Typ.)

$$BV_{DSS} = 200 V$$

$$R_{DS(on)} = 0.8 \Omega$$

$$I_D = 5 A$$

D²-PAK I²-PAK



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V _{DSS}	Drain-to-Source Voltage	200	V
I _D	Continuous Drain Current (T _C =25°C)	5	A
	Continuous Drain Current (T _C =100°C)	3.2	
I _{DM}	Drain Current-Pulsed ①	18	A
V _{GS}	Gate-to-Source Voltage	+ 20	V
E _{AS}	Single Pulsed Avalanche Energy ②	33	mJ
I _{AR}	Avalanche Current ①	5	A
E _{AR}	Repetitive Avalanche Energy ①	3.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5	V/ns
P _D	Total Power Dissipation (T _A =25°C)*	3.1	W
	Total Power Dissipation (T _C =25°C)	39	W
	Linear Derating Factor	0.31	W/°C
T _J , T _{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	°C
T _L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	--	3.17	°C/W
R _{θJA}	Junction-to-Ambient *	--	40	
R _{θJA}	Junction-to-Ambient	--	62.5	

* When mounted on the minimum pad size recommended (PCB Mount).

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	200	--	--	V	$V_{GS}=0V, I_D=250\ \mu\text{A}$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.18	--	V/ $^\circ\text{C}$	$I_D=250\ \mu\text{A}$ See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	1.0	--	2.0	V	$V_{DS}=5V, I_D=250\ \mu\text{A}$
I_{GSS}	Gate-Source Leakage, Forward	--	--	100	nA	$V_{GS}=20V$
	Gate-Source Leakage, Reverse	--	--	-100		$V_{GS}=-20V$
I_{DSS}	Drain-to-Source Leakage Current	--	--	10	μA	$V_{DS}=200V$
		--	--	100		$V_{DS}=160V, T_C=125^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.8	Ω	$V_{GS}=5V, I_D=2.5A$ ④
g_{fs}	Forward Transconductance	--	3.3	--	$\bar{\Omega}$	$V_{DS}=40V, I_D=2.5A$ ④
C_{iss}	Input Capacitance	--	330	430	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ See Fig 5
C_{oss}	Output Capacitance	--	55	70		
C_{rss}	Reverse Transfer Capacitance	--	25	30		
$t_{d(on)}$	Turn-On Delay Time	--	8	25	ns	$V_{DD}=100V, I_D=5A,$ $R_G=9\ \Omega$ See Fig 13 ④ ⑤
t_r	Rise Time	--	6	20		
$t_{d(off)}$	Turn-Off Delay Time	--	24	60		
t_f	Fall Time	--	6	20		
Q_g	Total Gate Charge	--	10.3	15	nC	$V_{DS}=160V, V_{GS}=5V,$ $I_D=5A$ See Fig 6 & Fig 12 ④ ⑤
Q_{gs}	Gate-Source Charge	--	2.0	--		
Q_{gd}	Gate-Drain("Miller") Charge	--	4.4	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	5	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	18		
V_{SD}	Diode Forward Voltage ④	--	--	1.5	V	$T_J=25^\circ\text{C}, I_S=5A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	--	140	--	ns	$T_J=25^\circ\text{C}, I_F=5A$
Q_{rr}	Reverse Recovery Charge	--	0.59	--	μC	$di_F/dt=100A/\mu\text{s}$ ④

Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② $L=2\text{mH}, I_{AS}=5A, V_{DD}=50V, R_G=27\ \Omega,$ Starting $T_J=25^\circ\text{C}$
- ③ $I_{SD} \leq 5A, di/dt \leq 180A/\mu\text{s}, V_{DD} \leq BV_{DSS},$ Starting $T_J=25^\circ\text{C}$
- ④ Pulse Test : Pulse Width = $250\ \mu\text{s},$ Duty Cycle $\leq 2\%$
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

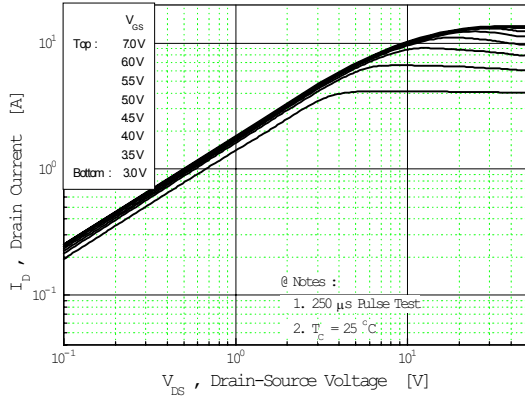


Fig 2. Transfer Characteristics

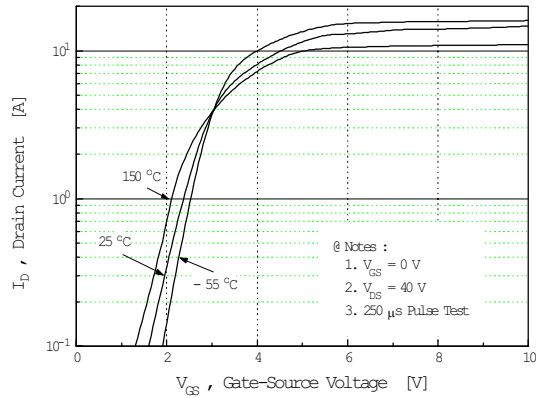


Fig 3. On-Resistance vs. Drain Current

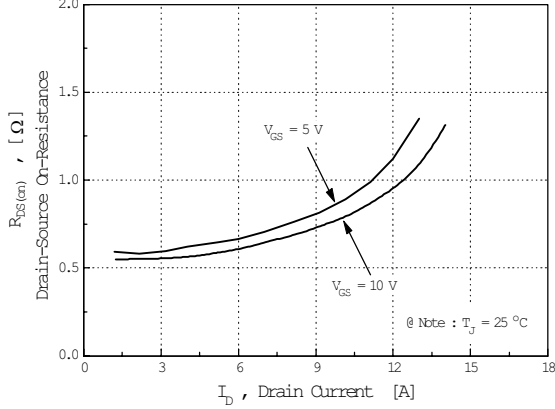


Fig 4. Source-Drain Diode Forward Voltage

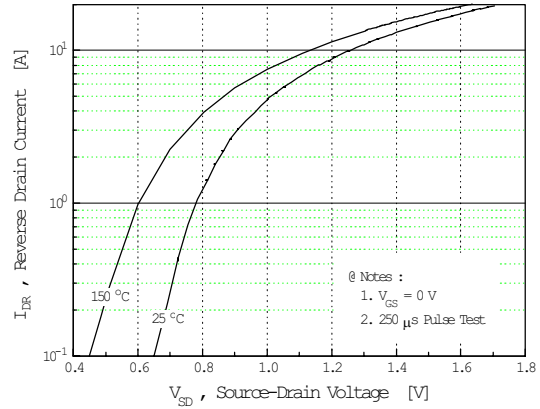


Fig 5. Capacitance vs. Drain-Source Voltage

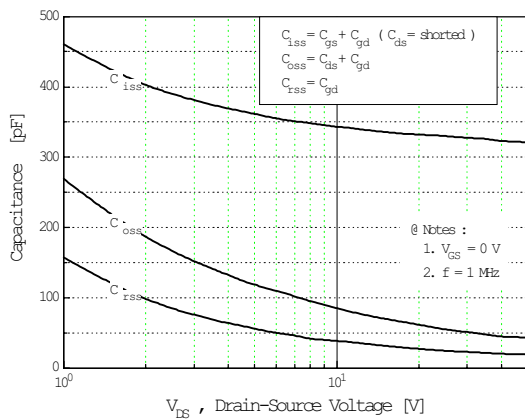
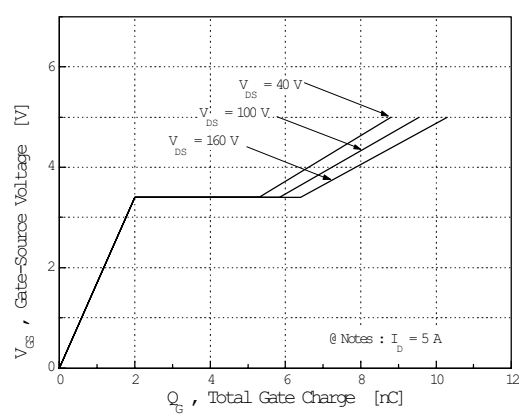


Fig 6. Gate Charge vs. Gate-Source Voltage



IRLW/I620A

N-CHANNEL POWER MOSFET

Fig 7. Breakdown Voltage vs. Temperature

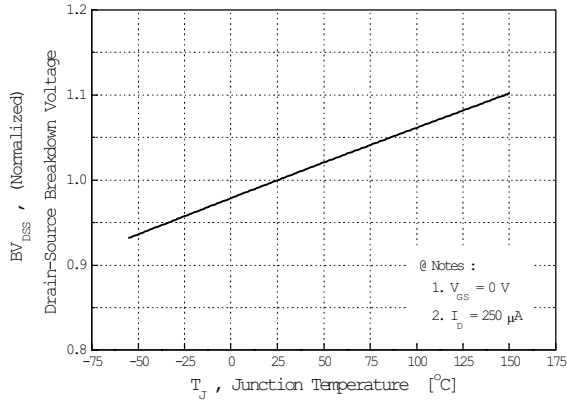


Fig 8. On-Resistance vs. Temperature

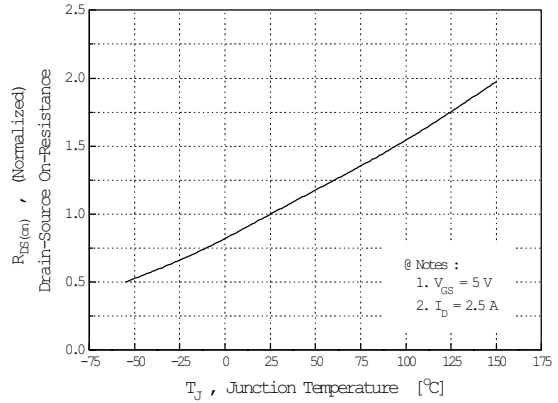


Fig 9. Max. Safe Operating Area

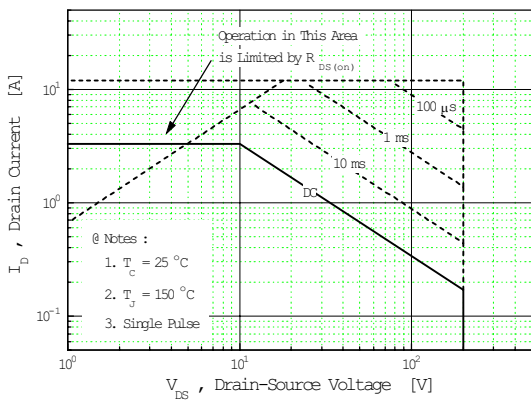


Fig 10. Max. Drain Current vs. Case Temperature

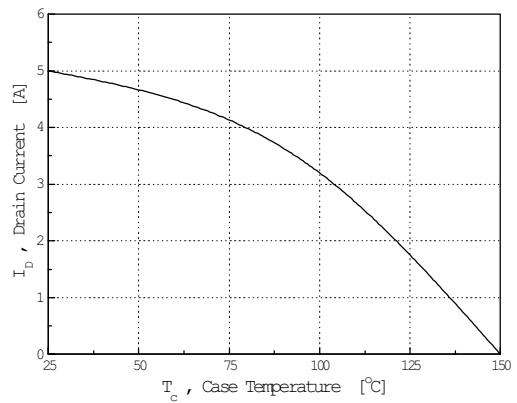


Fig 11. Thermal Response

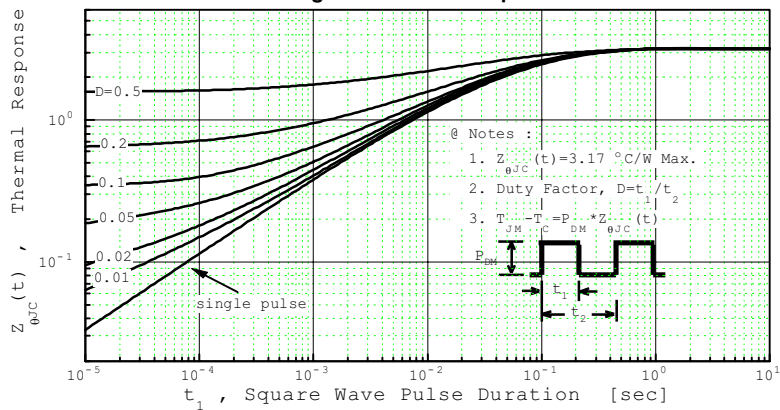


Fig 12. Gate Charge Test Circuit & Waveform

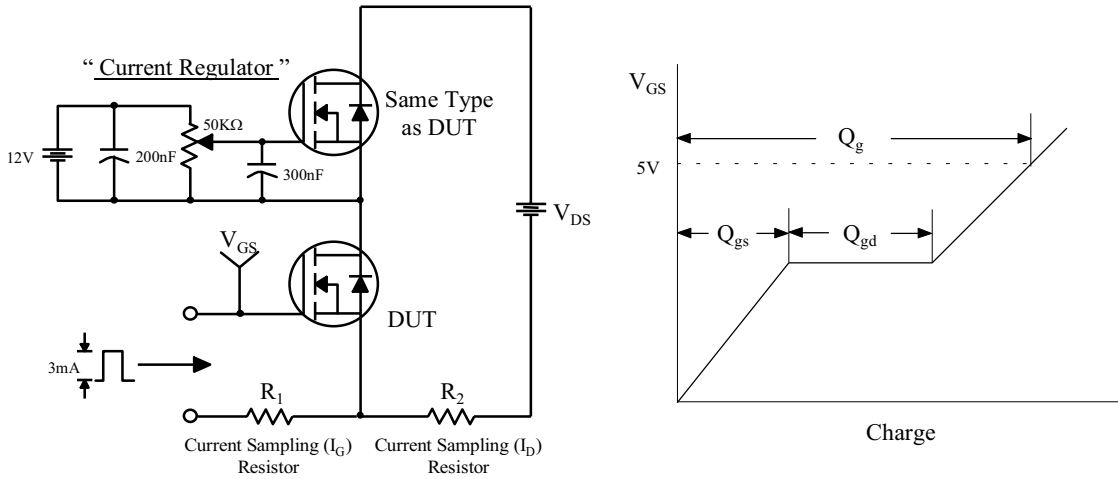


Fig 13. Resistive Switching Test Circuit & Waveforms

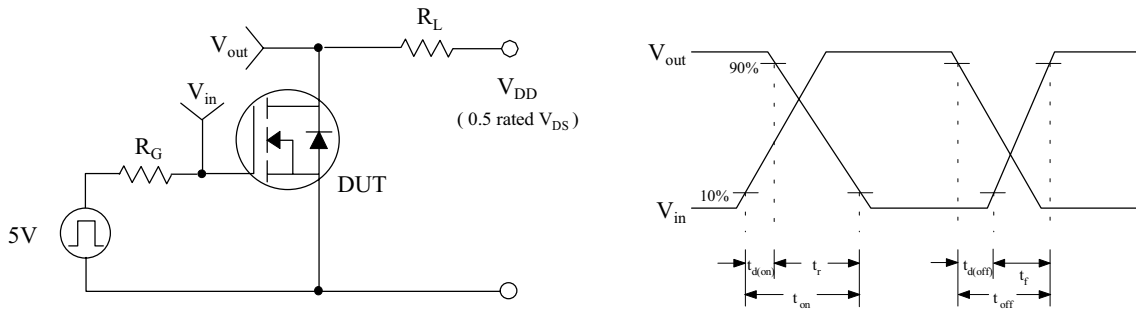


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

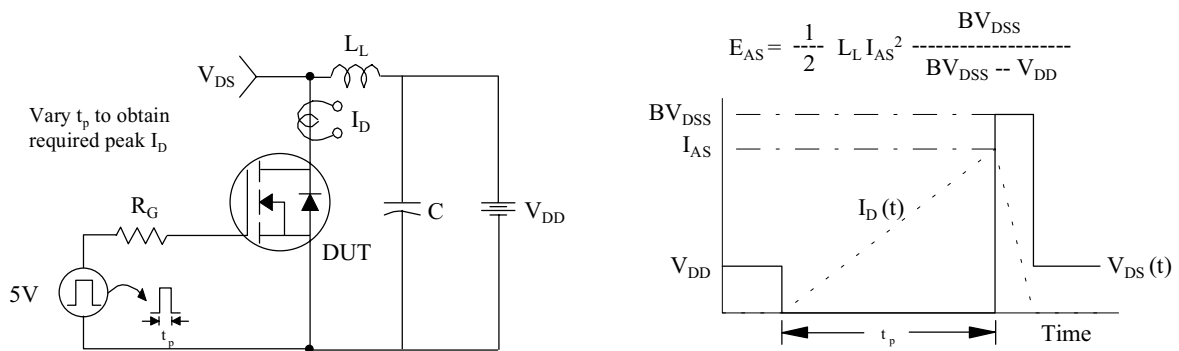


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

