## M-MOS Semiconductor Hong Kong Limited

# 8V Dual P-Channel Enhancement-Mode MOSFET

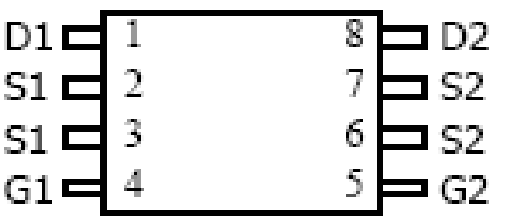
**$V_{DS}$= -8V**

**$R_{DS(ON)}$, $V_{gs}$@-4.5V, $I_{ds}$@-5.0A = 30mΩ**
**$R_{DS(ON)}$, $V_{gs}$@-2.5V, $I_{ds}$@-4.0A = 45mΩ**
**$R_{DS(ON)}$, $V_{gs}$@-1.8V, $I_{ds}$@-3.0A = 70mΩ**

## Features

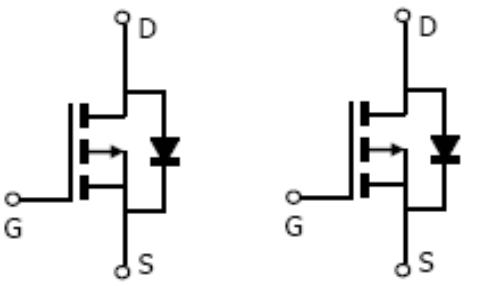
Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance
Ideal for battery multiplexing applications

**TSSOP-8**




**Top View**

**Internal Schematic Diagram**




**P-Channel MOSFET**

**Maximum Ratings and Thermal Characteristics** ($T_A$ = 25°C unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -8 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 8 | |
| Continuous Drain Current | | $I_D$ | -5 | A |
| Pulsed Drain Current [1)] | | $I_{DM}$ | -30 | |
| Maximum Power Dissipation | TA = 25°C | $P_D$ | 1.1 | W |
| | TA = 75°C | | 0.72 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to 150 | °C |
| Junction-to-Ambient Thermal Resistance (PCB mounted) [2)] | | $R_{\theta JA}$ | 62.5 | °C/W |

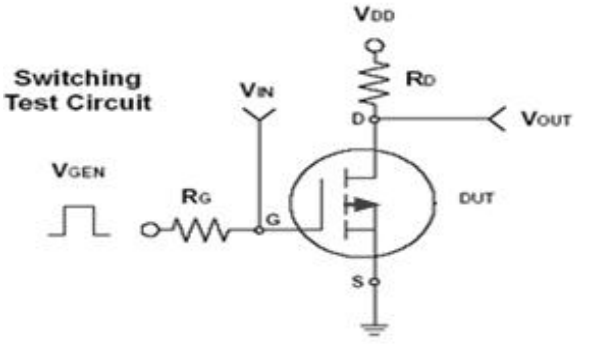
**Note:** 1. Repetitive Rating: Pulse width limited by the maximum junction temperature
2. 1-in$^2$ 2oz Cu PCB board

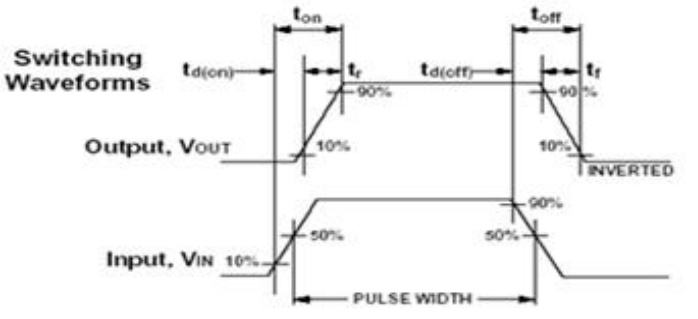
## ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250uA | -8 | | | V |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = -4.5V, $I_D$ = -5.0A | | 24.0 | 30.0 | mΩ |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = -2.5V, $I_D$ = -4.0A | | 33.0 | 45.0 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = -1.8V, $I_D$ = -3.0A | | 48.0 | 70.0 | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ =$V_{GS}$, $I_D$ = -250uA | -0.4 | 0.6 | -1 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -8V, $V_{GS}$ = 0V | | | -1 | uA |
| Gate Body Leakage | $I_{GSS}$ | $V_{GS}$ = ± 8V, $V_{DS}$ = 0V | | | ±100 | nA |
| **Dynamic**[3)] | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = -6V, $I_D$ = -5.0A<br>$V_{GS}$ = -4.5V | | | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | | | |
| Gate-Drain Charge | $Q_{gd}$ | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = -6V, RL= 6Ω<br>$I_D$ = -1A, $V_{GEN}$ = -4.5V<br>$R_G$ = 6Ω | | | | ns |
| Turn-On Rise Time | $t_r$ | | | | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | | | |
| Turn-Off Fall Time | $t_f$ | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = -6V, $V_{GS}$ = 0V<br>f = 1.0 MHz | | | | pF |
| Output Capacitance | $C_{oss}$ | | | | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | | | |
| **Source-Drain Diode** | | | | | | |
| Max. Diode Forward Current | $I_S$ | | | | | A |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = -1.25A, $V_{GS}$ = 0V | | | -1.1 | V |

**Note**: Pulse test: pulse width <= 300us, duty cycle<= 2%

3. Guaranteed by design; not subject to production testing



# Notice

**1. Specification of the products displayed herein are subject to change without notice. Continuous development may necessitate changes in technical data without notice. M-MOS Semiconductor Sdn. Bhd. or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.**

**2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**