Product Preview

HDTMOS E-FET™ High Energy Power FET D²PAK for Surface Mount

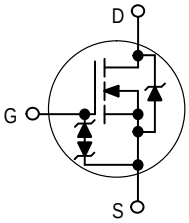
N–Channel Enhancement–Mode Silicon Gate

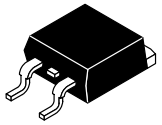
MTB35N06ZL

TMOS POWER FET
35 AMPERES
60 VOLTS
$R_{DS(on)}$ = 26 mΩ

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor–Absorbs High Energy in the Avalanche Mode
- ESD Protected. 400 V Machine Model Level and 4000 V Human Body Model Level.





CASE 418B–02, Style 2
D²PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±15 ±20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	35 22.8 105	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	94 0.63 3.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{DS} = 60 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 35 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	184	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.6 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

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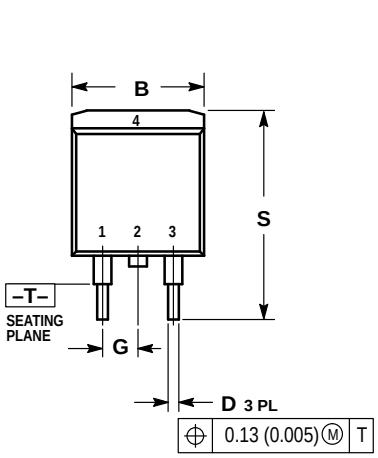
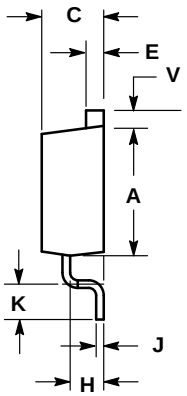
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 3.0) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 60 —	 — 52	 — —	 Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	5.0	μAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (Cpk ≥ 3.0) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 —	 1.5 4.0	 2.0 —	 Vdc mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (V_{GS} = 5.0 Vdc, I_D = 11.5 Adc)		$R_{DS(on)}$	—	22	26	mΩ
Drain–to–Source On–Voltage (V_{GS} = 5.0 Vdc) (I_D = 23 Adc) (I_D = 11.5 Adc, T_J = 125°C)		$V_{DS(on)}$	 — —	 0.78 0.7	 1.1 1.0	Vdc
Forward Transconductance (V_{DS} = 4.0 Vdc, I_D = 11.5 Adc)		g_{FS}	10	12	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1600	—	pF
Output Capacitance		C_{oss}	—	560	—	
Transfer Capacitance		C_{rss}	—	140	—	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 23 Adc, $V_{GS(on)}$ = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	40		ns
Rise Time		t_r	—	250		
Turn–Off Delay Time		$t_{d(off)}$	—	130		
Fall Time		t_f	—	170		
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 23 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	45		nC
		Q_1	—	8.0	—	
		Q_2	—	22	—	
		Q_3	—	19	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 23 Adc, V_{GS} = 0 Vdc) (I_S = 23 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 0.92 0.81	 1.1 —	Vdc
Reverse Recovery Time	(I_S = 23 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	43	—	ns
		t_a	—	24	—	
		t_b	—	20	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.055	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from drain lead 0.25″ from package to center of die)		L_D	 — —	 3.5 4.5	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS





STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

CASE 418B–02
ISSUE B

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