

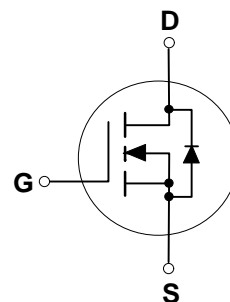
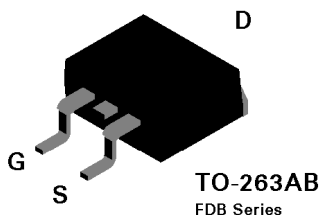
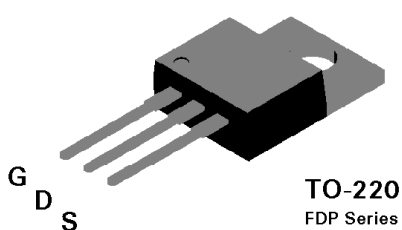
FDP6030L / FDB6030L N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 52 A, 30 V. $R_{DS(ON)} = 0.0135 \Omega @ V_{GS}=10 \text{ V}$
 $R_{DS(ON)} = 0.020 \Omega @ V_{GS}=4.5 \text{ V}$.
- Improved replacement for **NDP6030L/NDB6030L**.
- Low gate charge (typical 34 nC).
- Low Crss (typical 175 pF).
- Fast switching speed.



Absolute Maximum Ratings $T_c = 25^\circ\text{C}$ unless otherwise note

Symbol	Parameter	FDP6030L	FDB6030L	Units
V_{DSS}	Drain-Source Voltage	30		V
V_{GSS}	Gate-Source Voltage - Continuous	±20		V
I_D	Drain Current - Continuous	52		A
	- Pulsed	156		
P_D	Maximum Power Dissipation @ $T_c = 25^\circ\text{C}$	75		W
	Derate above 25°C	0.5		W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C

THERMAL CHARACTERISTICS

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

Electrical Characteristics $T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 15\text{ V}, I_D = 21\text{ A}$			150	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				21	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		37		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			10	μA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.6	3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-4		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 26\text{ A}$		0.0095	0.0135	Ω
		$T_J = 125^\circ\text{C}$		0.014	0.023	
		$V_{GS} = 4.5\text{ V}, I_D = 21\text{ A}$		0.015	0.02	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$	60			A
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}$	15			A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 26\text{ A}$		37		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1230		pF
C_{oss}	Output Capacitance			640		pF
C_{riss}	Reverse Transfer Capacitance			175		pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 15\text{ V}, I_D = 52\text{ A}$		7.6	15	nS
t_r	Turn - On Rise Time	$V_{GS} = 10\text{ V}, R_{GEN} = 24\ \Omega$		150	210	nS
$t_{D(off)}$	Turn - Off Delay Time			29	46	nS
t_f	Turn - Off Fall Time			17	27	nS
Q_g	Total Gate Charge	$V_{DS} = 12\text{ V}$		34	46	nC
Q_{gs}	Gate-Source Charge	$I_D = 26\text{ A}, V_{GS} = 10\text{ V}$		6		nC
Q_{gd}	Gate-Drain Charge			8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				52	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 26\text{ A}$ (Note 1)		0.91	1.3	V
		$T_J = 125^\circ\text{C}$		0.8	1.2	

Note

 1. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

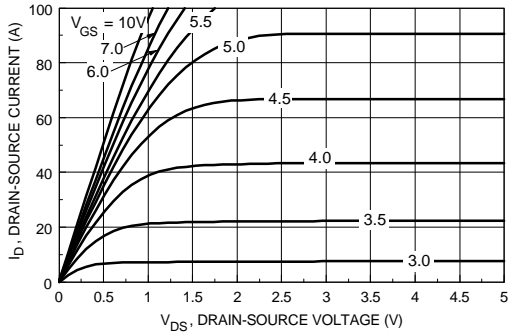


Figure 1. On-Region Characteristics.

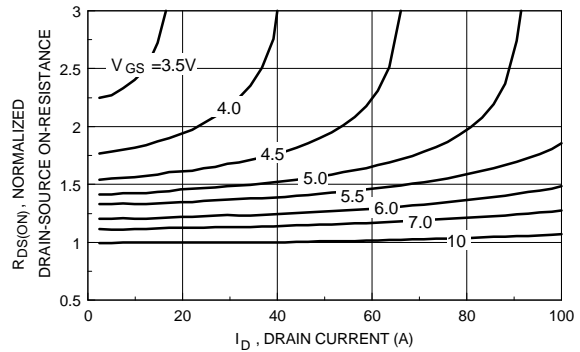


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

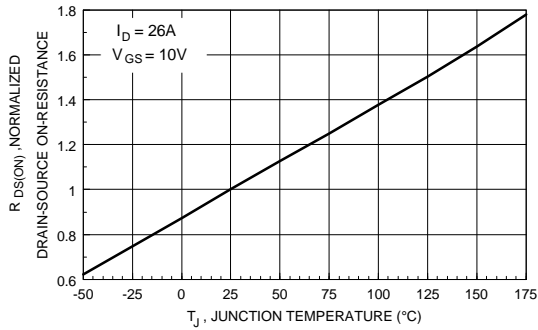


Figure 3. On-Resistance Variation with Temperature.

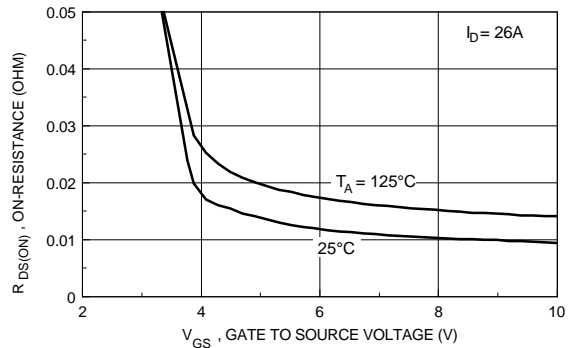


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

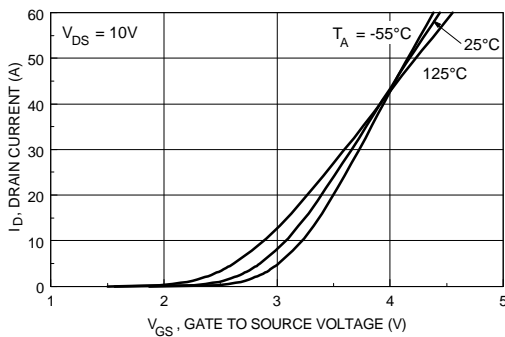


Figure 5. Transfer Characteristics.

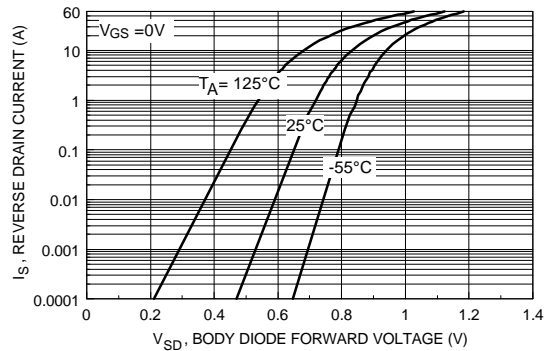


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics (continued)

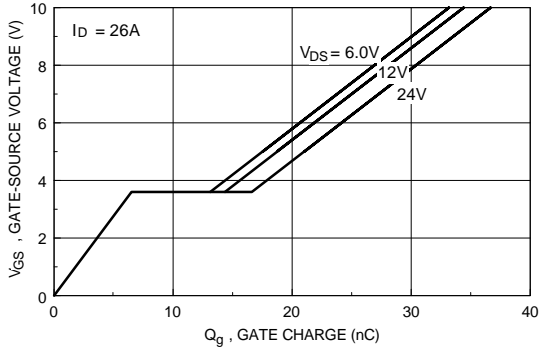


Figure 7. Gate Charge Characteristics.

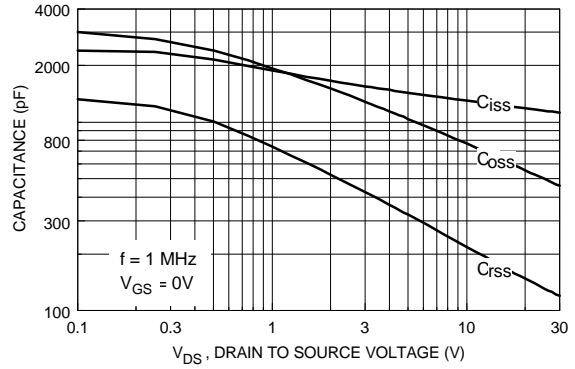


Figure 8. Capacitance Characteristics.

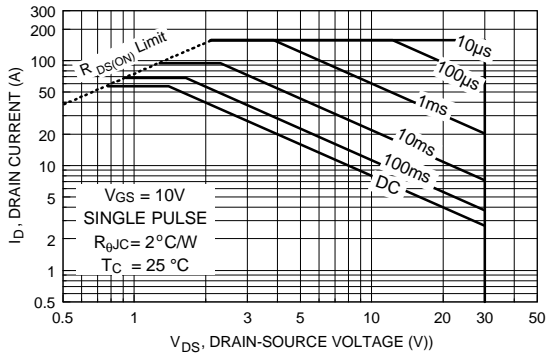


Figure 9. Maximum Safe Operating Area.

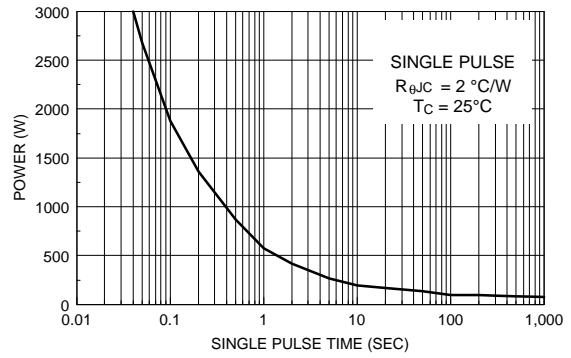


Figure 10. Single Pulse Maximum Power Dissipation.

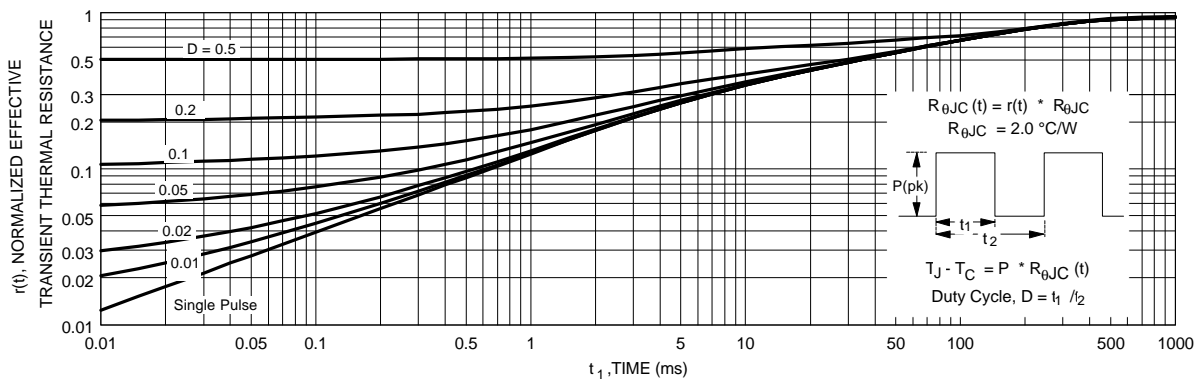


Figure 11. Transient Thermal Response Curve.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE _x TM	FAST [®]	OPTOLOGIC TM	SMART START TM	VCX TM
Bottomless TM	FAST _r TM	OPTOPLANAR TM	STAR*POWER TM	
CoolFET TM	FRFET TM	PACMAN TM	Stealth TM	
CROSSVOLT TM	GlobalOptoisolator TM	POPT TM	SuperSOT TM -3	
DenseTrench TM	GTO TM	Power247 TM	SuperSOT TM -6	
DOMET TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QST TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
FACT Quiet Series TM	MICROWIRE TM	SILENT SWITCHER [®]	UltraFET [®]	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.