

NP50N04YUK

Feb 08, 2013

Data Sheet

Description

The NP50N04YUK is N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

• Super low on-state resistance

 $R_{DS(on)} = 4.8 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 25 \text{ A})$

- Non logic level drive type
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Pac	Package	
NP50N04YUK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP50N04YUK-E2-AY *1			Taping (E2 type)	

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 V$)	V _{DSS}	40	V
Gate to Source Voltage ($V_{DS} = 0 V$)	V _{GSS}	±20	V
Drain Current (DC) ($T_c = 25^{\circ}C$)	I _{D(DC)}	±50	A
Drain Current (pulse) *1	I _{D(pulse)}	±200	A
Total Power Dissipation ($T_c = 25^{\circ}C$)	P _{T1}	97	W
Total Power Dissipation $(T_A = 25^{\circ}C)^{*2}$	P _{T2}	1.0	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Repetitive Avalanche Current *3	I _{AR}	23	A
Repetitive Avalanche Energy *3	E _{AR}	53	mJ

Notes: *1 $T_C = 25^{\circ}C$, $P_W \le 10 \ \mu s$, Duty Cycle $\le 1\%$

*2 Mounted on glass epoxy substrate of 40 mm \times 40 mm \times 1.6 mmt with 4% Copper area (35 $\mu m)$

*3 $R_G = 25 \Omega$, $V_{GS} = 20 V \rightarrow 0 V$

Thermal Resistance

Channel to Case Thermal Resistance	R _{th(ch-C)}	1.55	°C/W
Channel to Ambient Thermal Resistance	R _{th(ch-A)}	150	°C/W



Electrical Characteristics (T_A = 25°C)

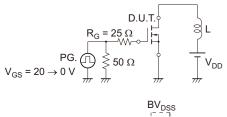
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions	
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	
Gate Leakage Current	I _{GSS}	_		±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	
Gate to Source Threshold Voltage	V _{GS(th)}	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	
Forward Transfer Admittance *1	y _{fs}	20	40	_	S	$V_{DS} = 5 V, I_{D} = 25 A$	
Drain to Source On-state Resistance *1	R _{DS(on)}	—	3.8	4.8	mΩ	V_{GS} = 10 V, I_{D} = 25 A	
Input Capacitance	Ciss	—	2100	3200	pF	V _{DS} = 25 V	
Output Capacitance	C _{oss}	—	300	450	pF	$V_{GS} = 0 V$	
Reverse Transfer Capacitance	Crss	—	130	240	pF	f = 1 MHz	
Turn-on Delay Time	t _{d(on)}	—	18	36	ns	$V_{DD} = 20 \text{ V}, \text{ I}_{D} = 25 \text{ A}$	
Rise Time	tr	—	11	27	ns	V _{GS} = 10 V	
Turn-off Delay Time	t _{d(off)}	—	45	90	ns	$R_G = 0 \Omega$	
Fall Time	t _f	—	5	12	ns		
Total Gate Charge	Q _G	—	38	57	nC	V _{DD} = 32 V	
Gate to Source Charge	Q _{GS}	—	10	_	nC	V _{GS} = 10 V	
Gate to Drain Charge	Q _{GD}	_	10		nC	I _D = 50 A	
Body Diode Forward Voltage *1	V _{F(S-D)}	_	0.9	1.5	V	$I_F = 50 \text{ A}, V_{GS} = 0 \text{ V}$	
Reverse Recovery Time	t _{rr}	—	35		ns	$I_F = 50 \text{ A}, V_{GS} = 0 \text{ V}$	
Reverse Recovery Charge	Q _{rr}	—	35	—	nC	di/dt = 100 A/µs	

 V_{GS}

0

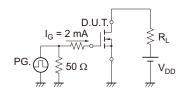
Note: *1 Pulsed test

TEST CIRCUIT 1 AVALANCHE CAPABILITY

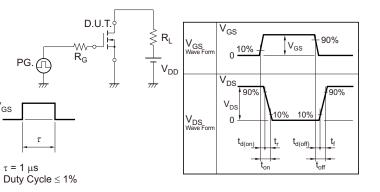


 I_{AS} I_{DS} V_{DD} Starting T_{ch}

TEST CIRCUIT 3 GATE CHARGE



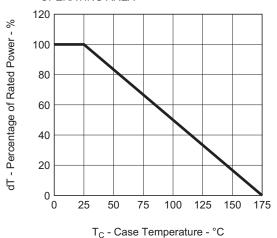
TEST CIRCUIT 2 SWITCHING TIME

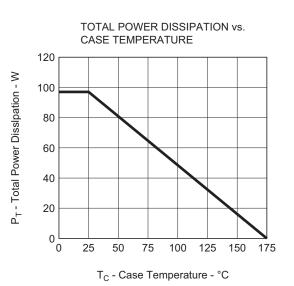




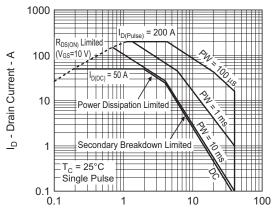
Typical Characteristics ($T_A = 25^{\circ}C$)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



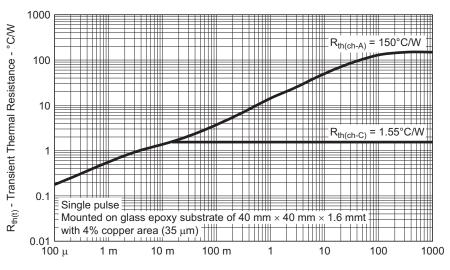


FORWARD BIAS SAFE OPERATING AREA



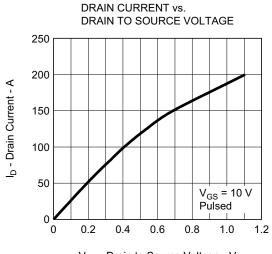


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

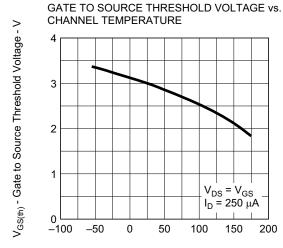


PW - Pulse Width - s

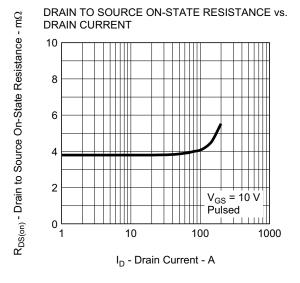




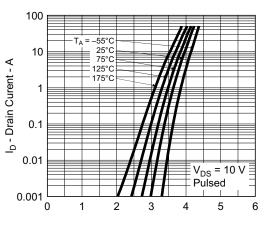
V_{DS} - Drain to Source Voltage - V



T_{ch} - Channel Temperature - °C

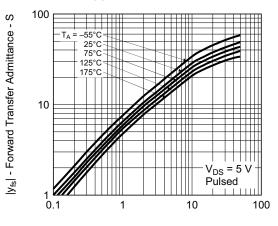


FORWARD TRANSFER CHARACTERISTICS

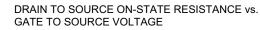


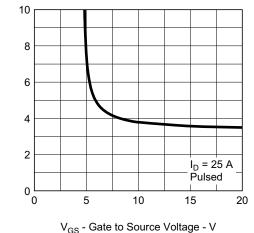


FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



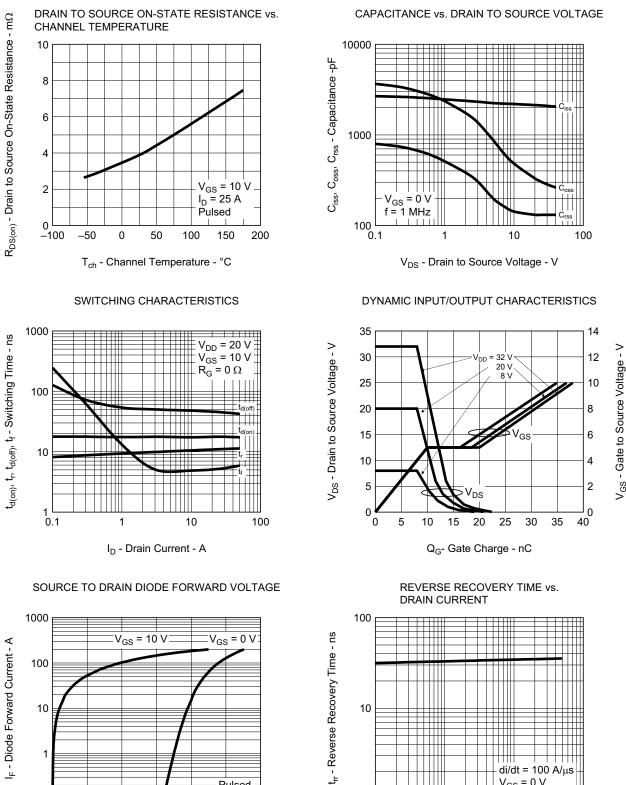
I_D - Drain Current - A

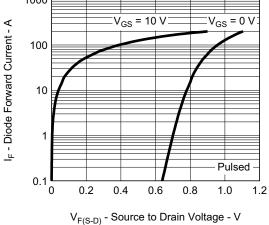




R07DS1003EJ0100 Rev.1.00 Feb 08, 2013 $R_{DS(on)}$ - Drain to Source On-State Resistance - $m\Omega$

NP50N04YUK







1 └ 0.1

10

I_F - Drain Current - A

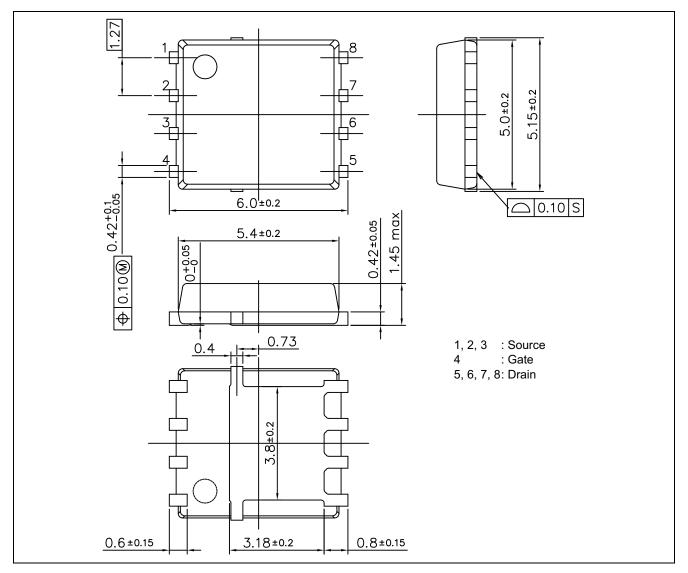
1

di/dt = 100 A/µs V_{GS} = 0 V

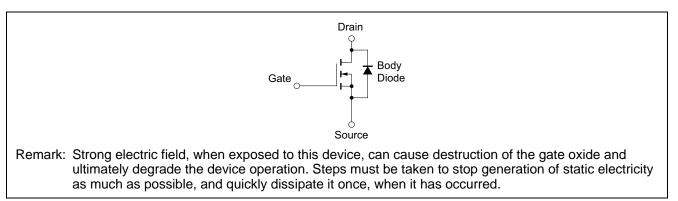
100

Package Drawing (Unit: mm)

8-pin HSON (Mass: 0.128 g TYP.)



Equivalent Circuit



Revision Histo	ry
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NP50N04YUK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Feb 08, 2013	—	First Edition Issued	

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