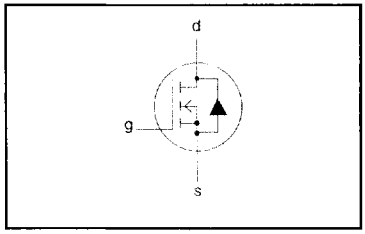
PowerMOS transistors Avalanche energy rated

PHP3N50E, PHB3N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 3.4 A

$R_{DS(ON)} \leq 3\ \Omega$

GENERAL DESCRIPTION

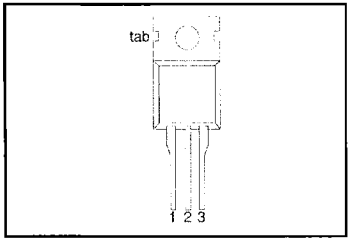
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP3N50E is supplied in the SOT78 (TO220AB) conventional leaded package.
The PHB3N50E is supplied in the SOT404 surface mounting package.

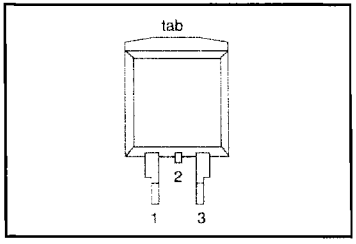
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 °C to 150°C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 °C to 150°C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 °C; V_{GS} = 10 V	-	3.4	A
		T_{mb} = 100 °C; V_{GS} = 10 V	-	2.2	A
I_{DM}	Pulsed drain current	T_{mb} = 25 °C	-	14	A
P_D	Total dissipation	T_{mb} = 25 °C	-	83	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	°C

1 It is not possible to make connection to pin 2 of the SOT404 package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_D = 2.5 A; $V_{DD} \leq 50$ V; starting T_j = 25°C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	210	mJ
E_{AR}	Repetitive avalanche energy[2]		-	5	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	2.5	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	1.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 1.7 A	-	2.5	3	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 1.7 A	1	2	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	-	30	250	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 3.4 A; V_{DD} = 400 V; V_{GS} = 10 V	-	26	30	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	13	17	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 68 Ω;	-	10	-	ns
t_r	Turn-on rise time	R_G = 18 Ω	-	29	-	ns
$t_{d(off)}$	Turn-off delay time		-	66	-	ns
t_f	Turn-off fall time		-	32	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	310	-	pF
C_{oss}	Output capacitance		-	50	-	pF
C_{rss}	Feedback capacitance		-	28	-	pF

2 pulse width and repetition rate limited by T_j max.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25°C	-	-	3.4	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25°C	-	-	14	A
V_{SD}	Diode forward voltage	I_S = 3.4 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 3.4 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	370	-	ns
Q_{rr}	Reverse recovery charge		-	2.7	-	µC

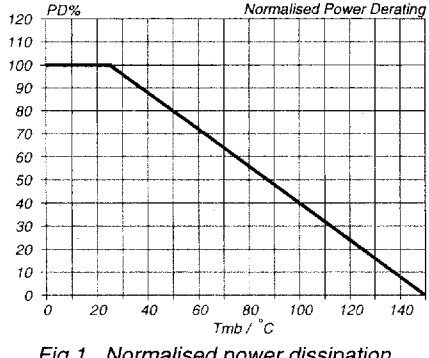


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

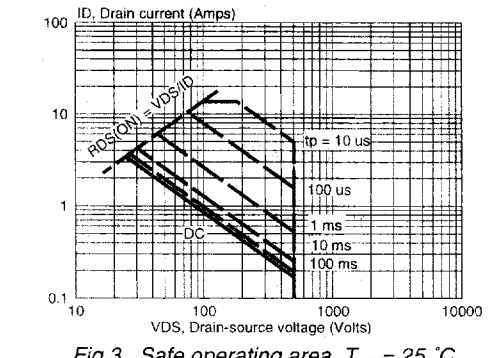


Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

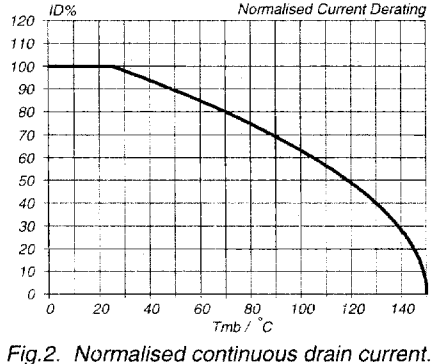


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

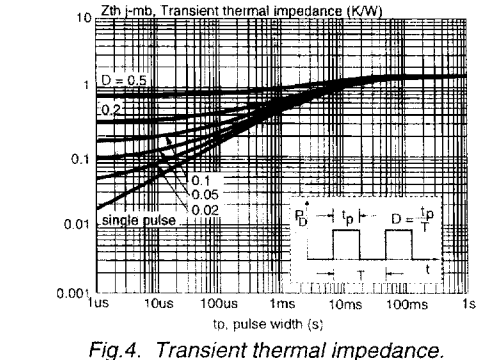


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

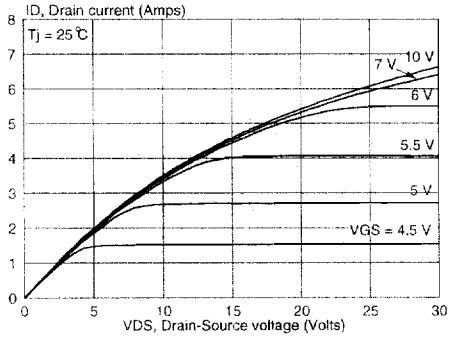


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

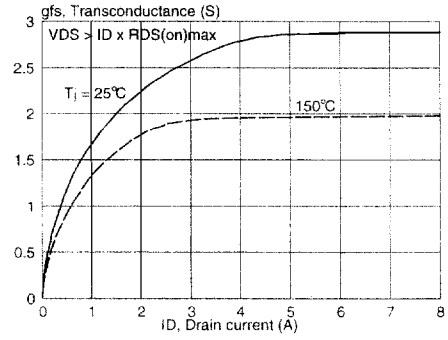


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

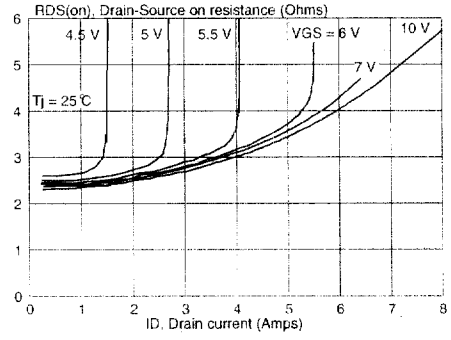


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

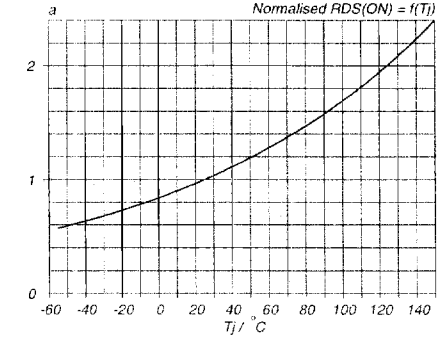


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 1.7 A; V_{GS} = 10 V

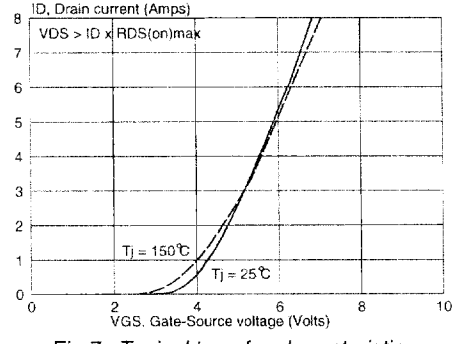


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

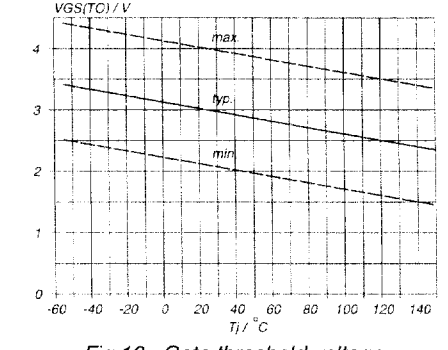


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

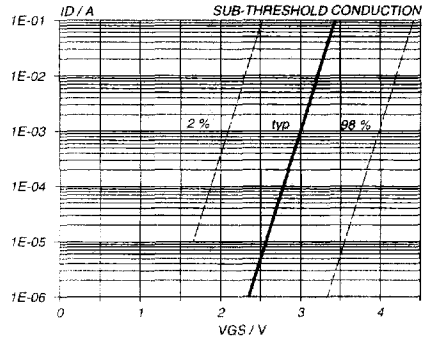


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ °C; $V_{DS} = V_{GS}$

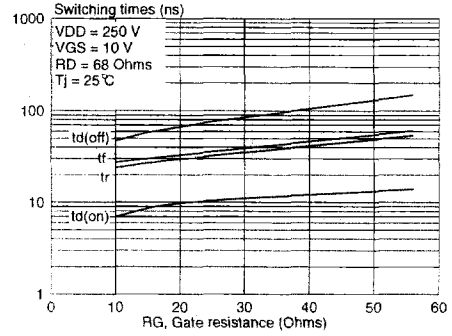


Fig.14. Typical switching times.
$t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

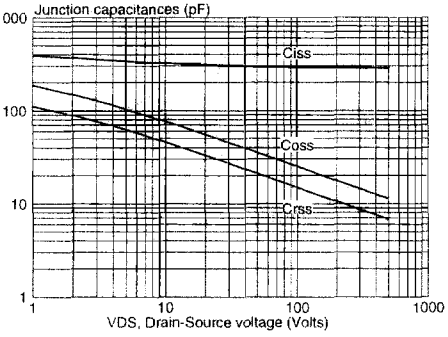


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

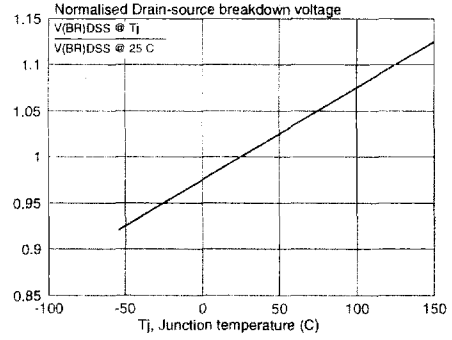


Fig.15. Normalised drain-source breakdown voltage.
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ °C} = f(T_j)$

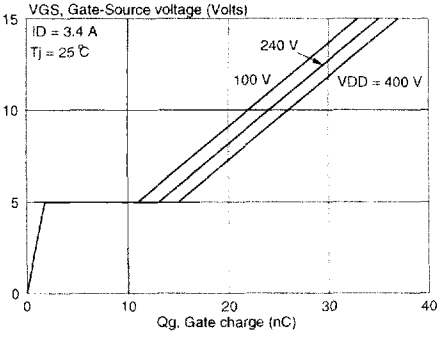


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

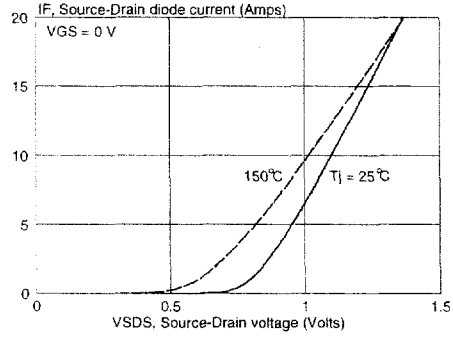


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

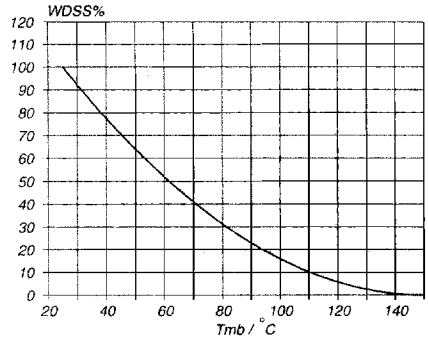


Fig.17. Normalised non-repetitive avalanche energy rating.
$E_{AS}\% = f(T_{mb})$

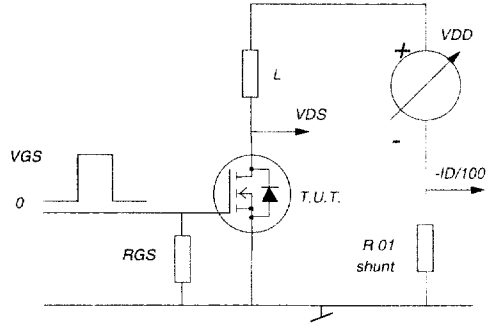


Fig.18. Unclamped inductive test circuit.

$$E_{AS} = 0.5 \cdot LI_D^2 \cdot \frac{V_{(BR)DSS}}{(V_{(BR)DSS} - V_{DD})}$$