

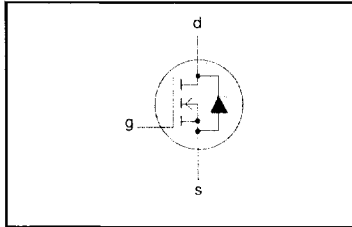
**PowerMOS transistors  
FREDFET, Avalanche energy rated**

**PHP4ND40E, PHB4ND40E**

**FEATURES**

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance
- Fast reverse recovery diode

**SYMBOL**



**QUICK REFERENCE DATA**

$V_{DSS} = 400\text{ V}$
$I_D = 4.4\text{ A}$
$R_{DS(ON)} \leq 1.8\ \Omega$
$t_{rr} = 180\text{ ns}$

**GENERAL DESCRIPTION**

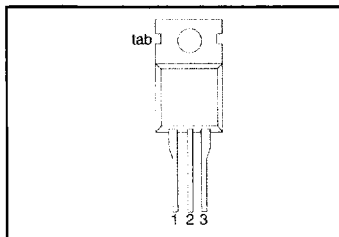
N-channel, enhancement mode field-effect power transistor, incorporating a **F**ast **R**ecovery **E**pitaxial **D**iode (FRED). This gives improved switching performance in half bridge and full bridge converters making this device particularly suitable for inverters, lighting ballasts and motor control circuits.

The PHP4ND40E is supplied in the SOT78 (TO220AB) conventional leaded package.  
The PHB4ND40E is supplied in the SOT404 surface mounting package.

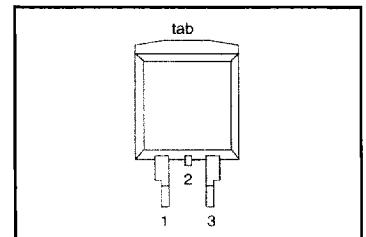
**PINNING**

PIN	DESCRIPTION
1	gate
2	drain <sup>1</sup>
3	source
tab	drain

**SOT78 (TO220AB)**



**SOT404**



**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DSS}$	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	-	400	V
$V_{DGR}$	Drain-gate voltage	$T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	400	V
$V_{GS}$	Gate-source voltage		-	$\pm 30$	V
$I_D$	Continuous drain current	$T_{mb} = 25\text{ }^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$	-	4.4	A
		$T_{mb} = 100\text{ }^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$	-	2.7	A
$I_{DM}$	Pulsed drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	18	A
$P_D$	Total dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	83	W
$T_j, T_{stg}$	Operating junction and storage temperature range		- 55	150	$^\circ\text{C}$

1 It is not possible to make connection to pin 2 of the SOT404 package.

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## PHP4ND40E, PHB4ND40E

### AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$E_{AS}$	Non-repetitive avalanche energy	Unclamped inductive load, $I_D = 3.3$ A; $V_{DD} \leq 50$ V; starting $T_j = 25^\circ\text{C}$ ; $R_{GS} = 50 \Omega$ ; $V_{GS} = 10$ V	-	190	mJ
$E_{AR}$ $I_{AS}, I_{AR}$	Repetitive avalanche energy <sup>2</sup> Repetitive and non-repetitive avalanche current		-	5 3.3	mJ A

### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th(j-mb)}$	Thermal resistance junction to mounting base		-	-	1.5	K/W
$R_{th(j-a)}$	Thermal resistance junction to ambient	SOT78 package, in free air SOT404 package, pcb mounted, minimum footprint	-	60 50	-	K/W K/W

### ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0.25$ mA	400	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	$V_{DS} = V_{GS}$ ; $I_D = 0.25$ mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	$V_{GS} = 10$ V; $I_D = 2.2$ A	-	1.3	1.8	$\Omega$
$V_{GS(TH)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ ; $I_D = 0.25$ mA	2.0	3.0	4.0	V
$g_{fs}$	Forward transconductance	$V_{DS} = 30$ V; $I_D = 2.2$ A	1.3	2.2	-	S
$I_{DSS}$	Drain-source leakage current	$V_{DS} = 400$ V; $V_{GS} = 0$ V	-	1	25	$\mu\text{A}$
$I_{GSS}$	Gate-source leakage current	$V_{DS} = 320$ V; $V_{GS} = 0$ V; $T_j = 125^\circ\text{C}$ $V_{GS} = \pm 30$ V; $V_{DS} = 0$ V	-	30 10	250 200	$\mu\text{A}$ nA
$Q_{g(tot)}$	Total gate charge	$I_D = 4.4$ A; $V_{DD} = 320$ V; $V_{GS} = 10$ V	-	26	30	nC
$Q_{gs}$	Gate-source charge		-	2	4	nC
$Q_{gd}$	Gate-drain (Miller) charge		-	14	17	nC
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 200$ V; $R_D = 47 \Omega$ ;	-	10	-	ns
$t_r$	Turn-on rise time	$R_G = 18 \Omega$	-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	55	-	ns
$t_f$	Turn-off fall time		-	38	-	ns
$L_d$	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
$L_d$	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
$L_s$	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
$C_{iss}$	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; $f = 1$ MHz	-	310	-	pF
$C_{oss}$	Output capacitance		-	60	-	pF
$C_{riss}$	Feedback capacitance		-	36	-	pF

2 pulse width and repetition rate limited by  $T_j$  max.

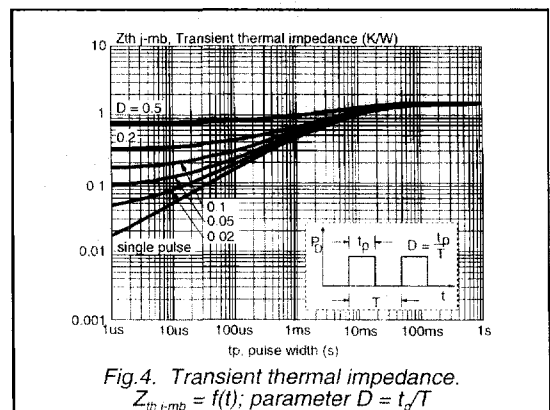
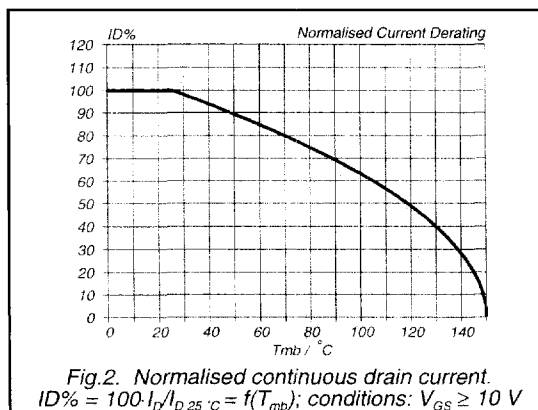
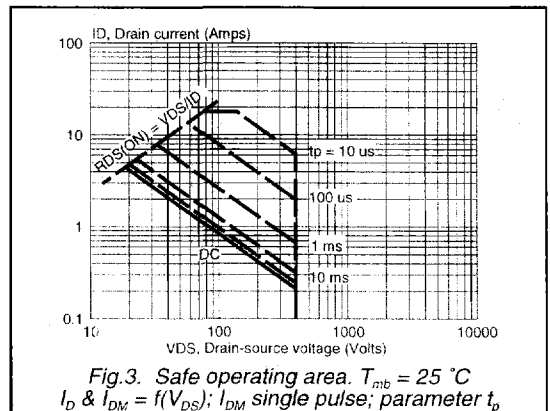
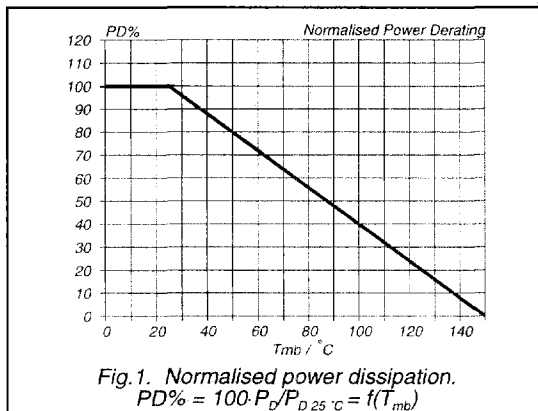
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SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

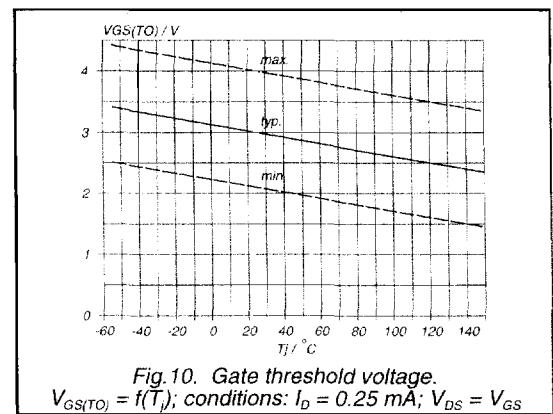
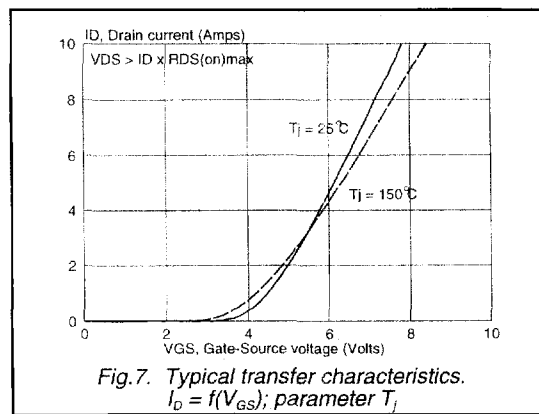
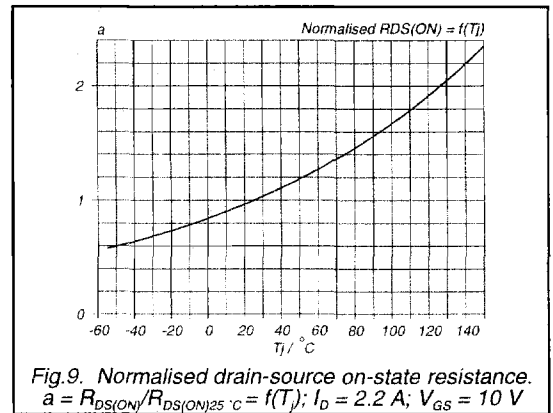
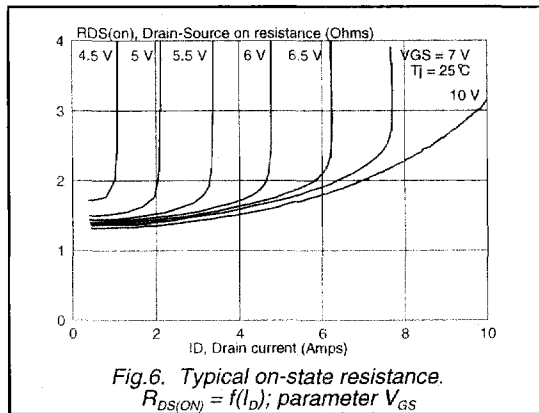
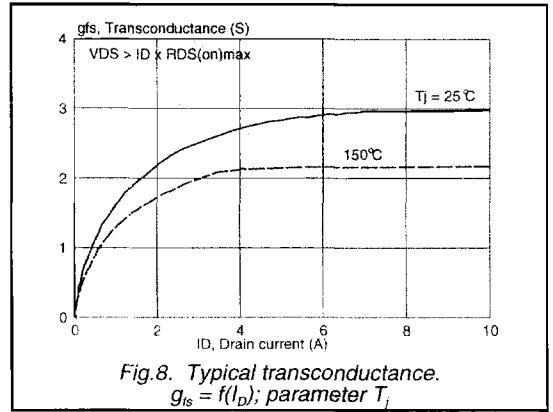
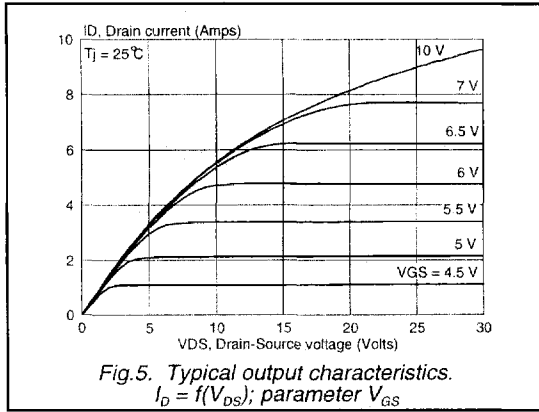
$T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_S$	Continuous source current (body diode)	$T_{mb} = 25^\circ\text{C}$	-	-	4.4	A
$I_{SM}$	Pulsed source current (body diode)	$T_{mb} = 25^\circ\text{C}$	-	-	18	A
$V_{SD}$	Diode forward voltage	$I_S = 4.4\text{ A}; V_{GS} = 0\text{ V}$	-	-	1.5	V
$t_{rr}$	Reverse recovery time	$I_S = 4.4\text{ A}; V_{GS} = 0\text{ V}; dl/dt = 100\text{ A}/\mu\text{s}; 125^\circ\text{C}$	-	180 220	-	ns ns
$Q_{rr}$	Reverse recovery charge	$I_S = 4.4\text{ A}; V_{GS} = 0\text{ V}; dl/dt = 100\text{ A}/\mu\text{s}; 125^\circ\text{C}$	-	0.65 2.6	-	$\mu\text{C}$ $\mu\text{C}$
$I_{rm}$	Peak reverse recovery current	$I_S = 4.4\text{ A}; V_{GS} = 0\text{ V}; dl/dt = 100\text{ A}/\mu\text{s}; 125^\circ\text{C}$	-	15	-	A



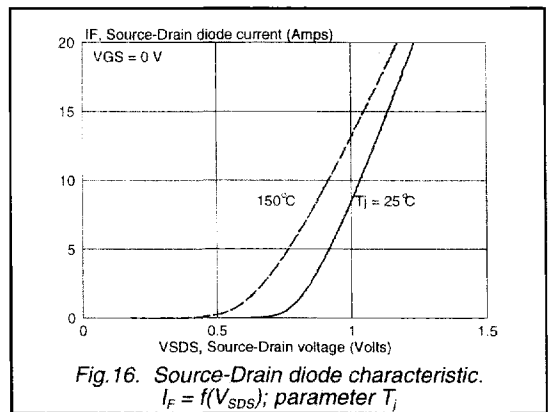
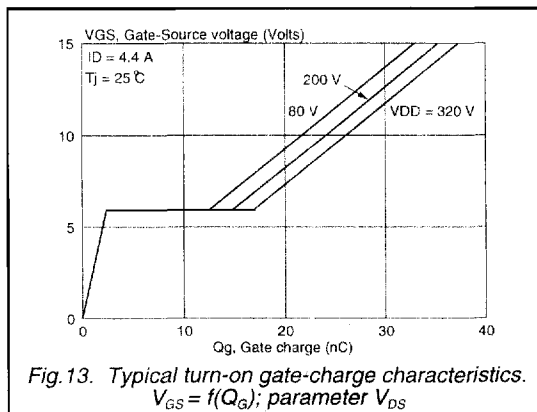
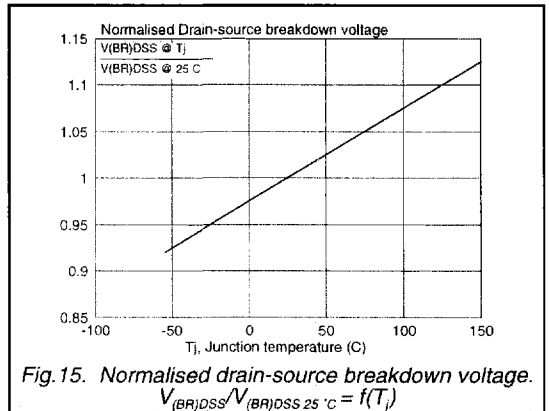
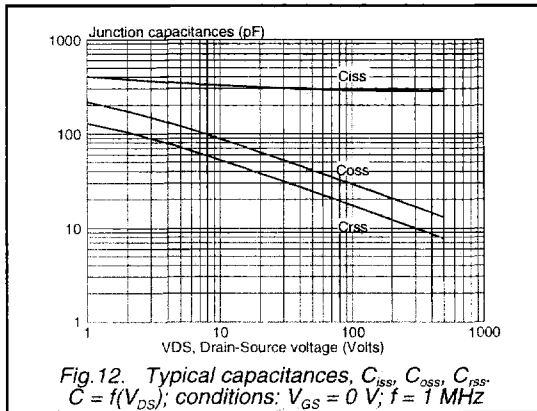
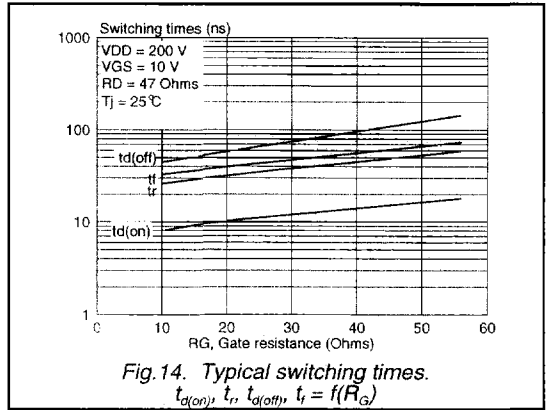
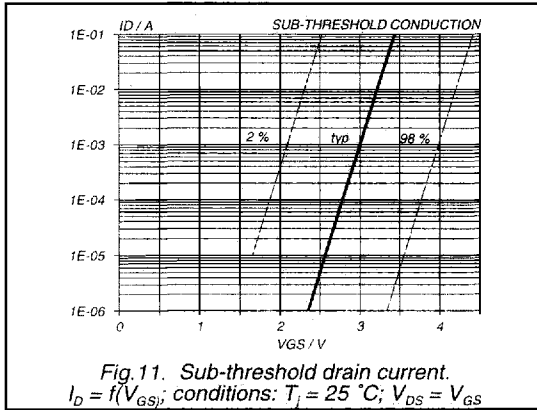
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