

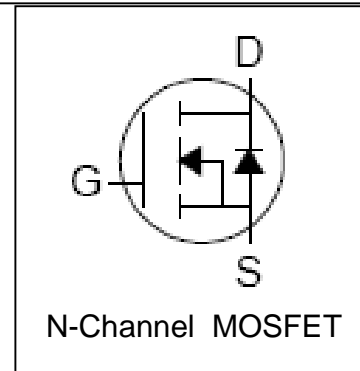
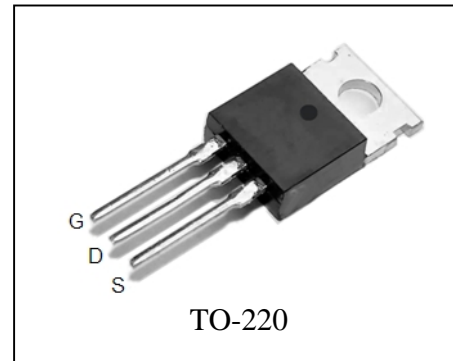
Features

- 100V/32A,
 $R_{DS(ON)} = 34m$ (Typ.) @ $V_{GS} = 10V$
- Super High Dense Cell Design
- Ultra Low On-Resistance
- 100% avalanche tested
- Lead Free and Green Devices Available
 (RoHS Compliant)

Applications

- DC-DC Converters
- Synchronous Rectifier

Pin Description



Absolute Maximum Ratings

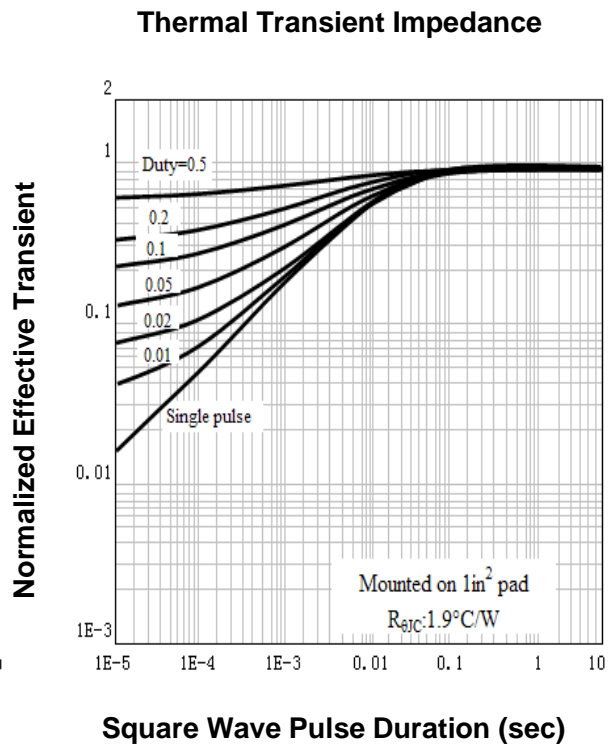
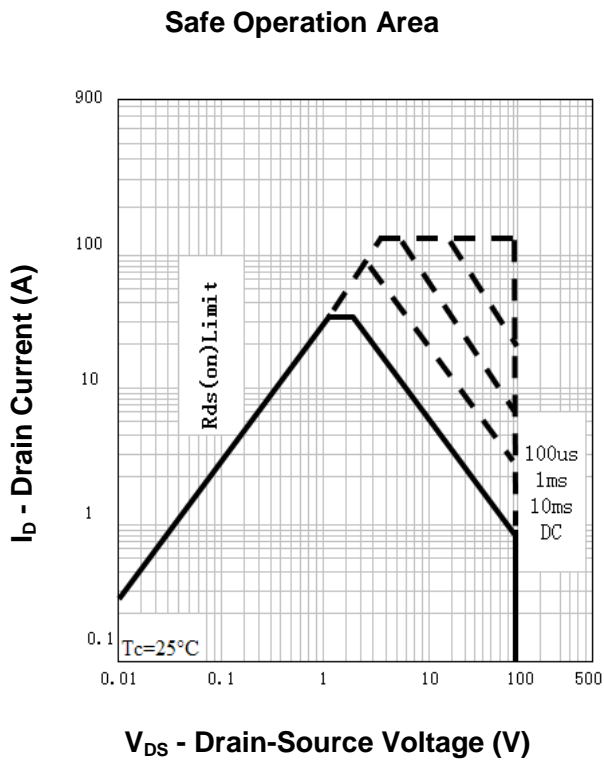
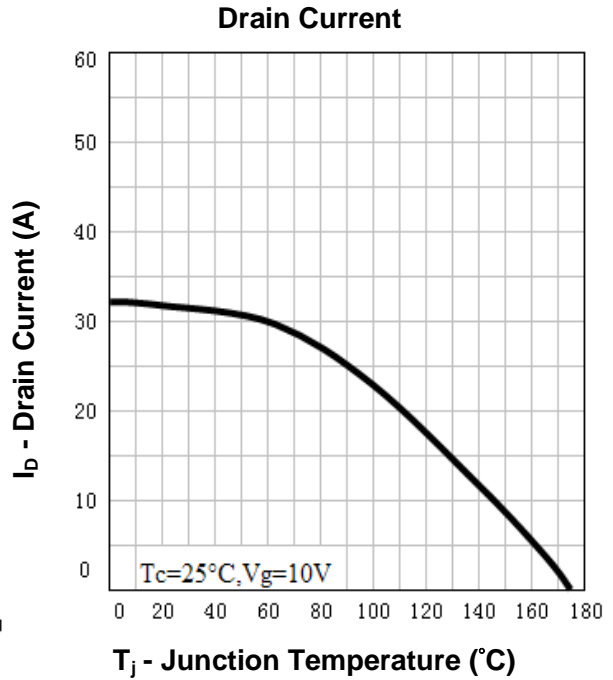
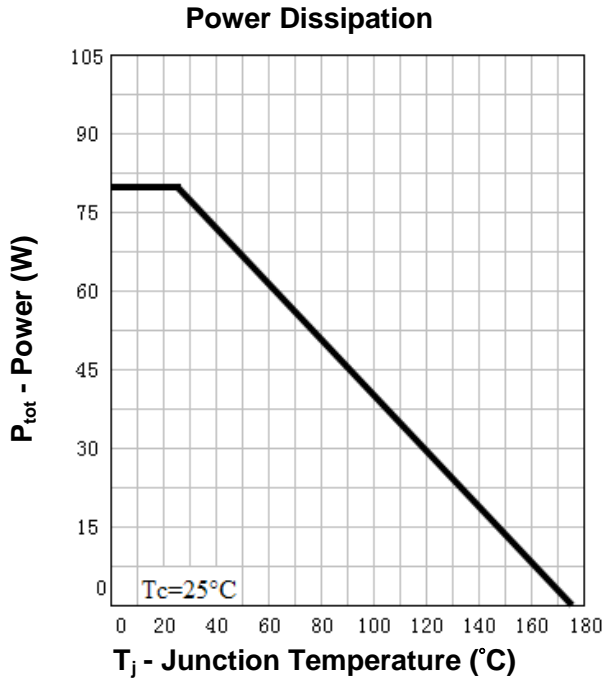
Symbol	Parameter	Rating	Unit
Common Ratings ($T_C = 25^\circ C$ Unless Otherwise Noted)			
V_{DSS}	Drain-Source Voltage	100	V
V_{GSS}	Gate-Source Voltage	± 20	
T_J	Maximum Junction Temperature	175	$^\circ C$
T_{STG}	Storage Temperature Range	-55 to 175	$^\circ C$
I_S	Diode Continuous Forward Current	$T_C = 25^\circ C$ 32	A
Mounted on Large Heat Sink			
I_{DP}	300 μs Pulse Drain Current Tested	$T_C = 25^\circ C$ 128 ^①	A
I_D	Continuous Drain Current	$T_C = 25^\circ C$ 32	A
		$T_C = 100^\circ C$ 23	
P_D	Maximum Power Dissipation	$T_C = 25^\circ C$ 79	W
		$T_C = 100^\circ C$ 39	W
$R_{\theta JC}$	Thermal Resistance-Junction to Case	1.9	$^\circ C/W$
Drain-Source Avalanche Ratings			
E_{AS} ^②	Avalanche Energy, Single Pulsed	64	mJ

Electrical Characteristics ($T_C=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Condition	RU1H36R			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	100			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V$ $T_J=85^\circ\text{C}$			1 30	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	2	3	4	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
$R_{DS(ON)}^{(3)}$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=30A$		34	40	m Ω
Diode Characteristics						
$V_{SD}^{(3)}$	Diode Forward Voltage	$I_{SD}=30A, V_{GS}=0V$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD}=30A, di_{SD}/dt=100A/\mu s$		32		ns
Q_{rr}	Reverse Recovery Charge			45		nC
Dynamic Characteristics ⁽⁴⁾						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$		1		Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=50V,$ Frequency=1.0MHz		1600		pF
C_{oss}	Output Capacitance			230		
C_{riss}	Reverse Transfer Capacitance			95		
$t_{d(ON)}$	Turn-on Delay Time			14		
t_r	Turn-on Rise Time	$V_{DD}=50V, R_L=1.7\Omega,$ $I_{DS}=30A, V_{GEN}=10V,$ $R_G=4.7\Omega$		95		
$t_{d(OFF)}$	Turn-off Delay Time			53		
t_f	Turn-off Fall Time			26		
Gate Charge Characteristics ⁽⁴⁾						
Q_g	Total Gate Charge	$V_{DS}=80V, V_{GS}=10V,$ $I_{DS}=30A$		28		nC
Q_{gs}	Gate-Source Charge			9		
Q_{gd}	Gate-Drain Charge			8		

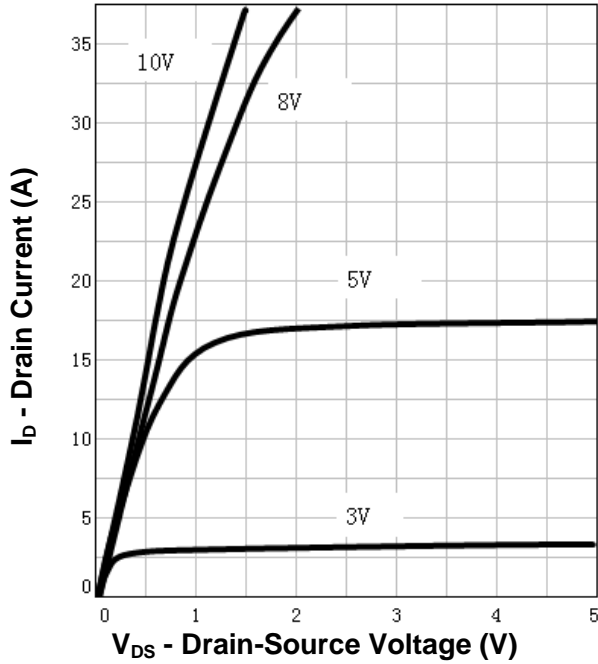
- Notes: ① Pulse width limited by safe operating area.
 ② Limited by T_{Jmax} , $I_{AS}=16A$, $V_{DD}=48V$, $R_G=50\Omega$, Starting $T_J=25^\circ\text{C}$.
 ③ Pulse test; Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
 ④ Guaranteed by design, not subject to production testing.

Typical Characteristics

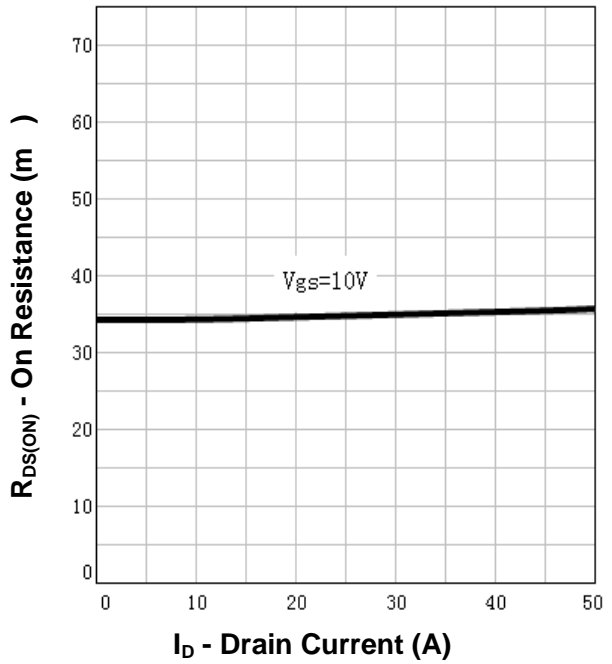


Typical Characteristics

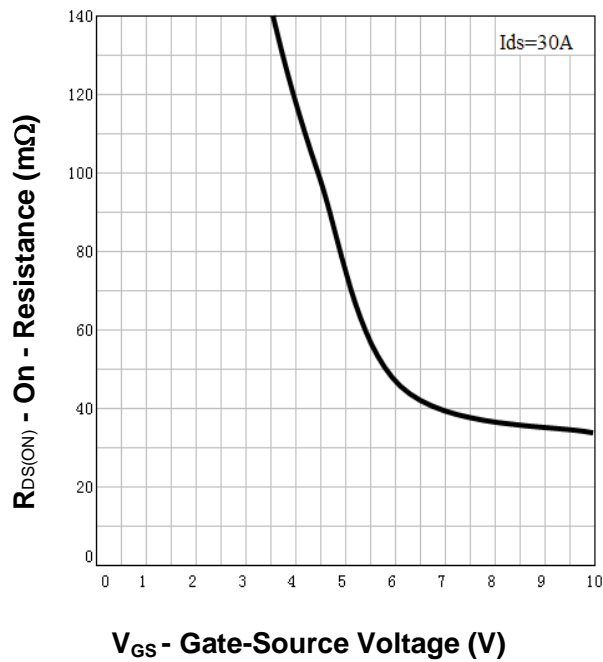
Output Characteristics



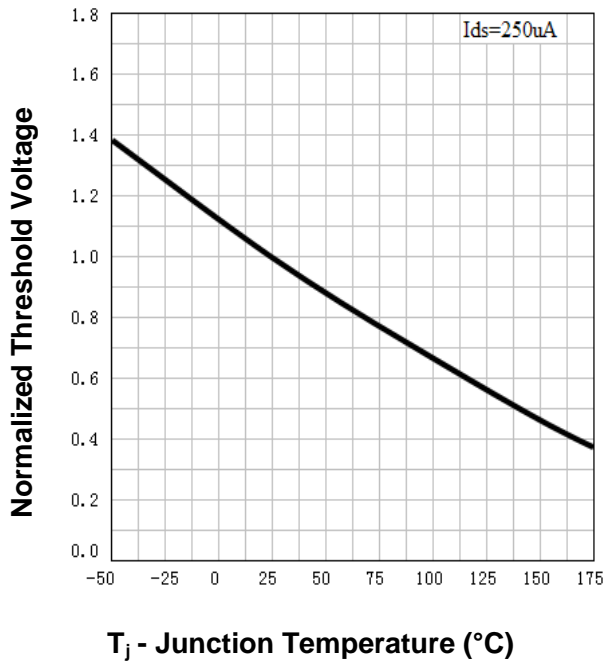
Drain-Source On Resistance



Drain-Source On Resistance

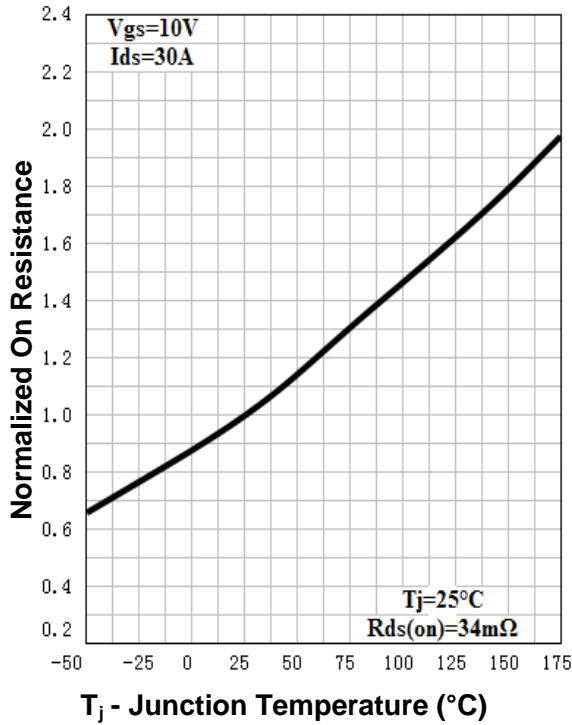


Gate Threshold Voltage

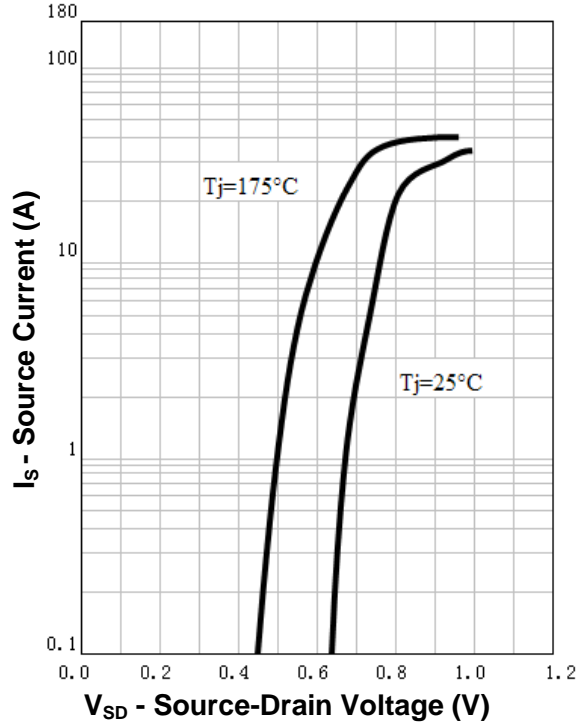


Typical Characteristics

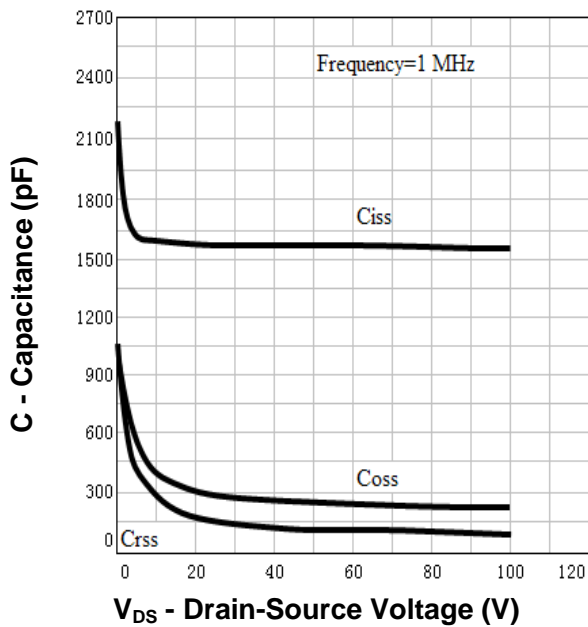
Drain-Source On Resistance



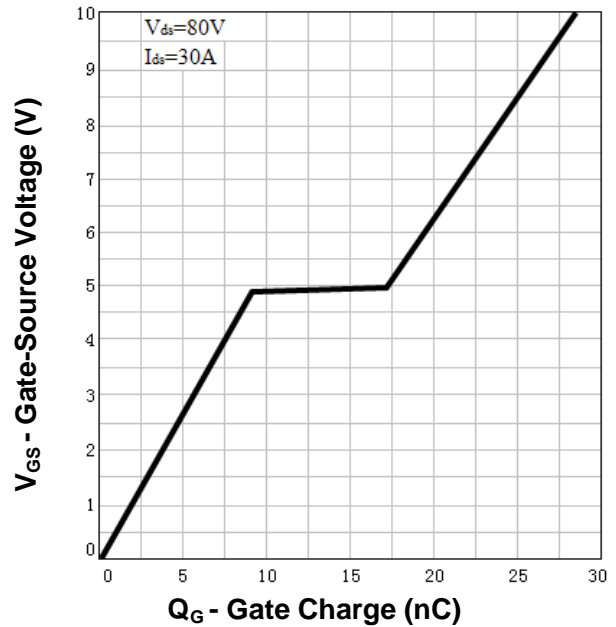
Source-Drain Diode Forward



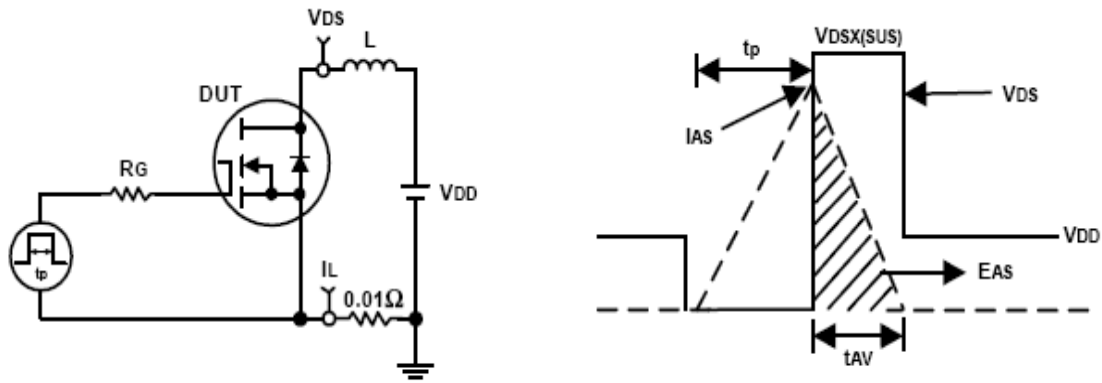
Capacitance



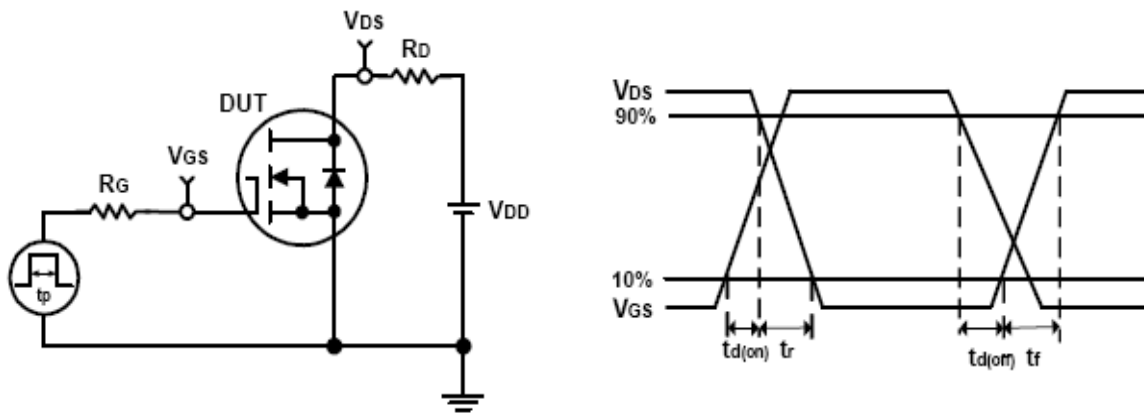
Gate Charge



Avalanche Test Circuit and Waveforms



Switching Time Test Circuit and Waveforms



Ordering and Marking Information

Device	Marking	Package	Packaging	Quantity	Reel Size	Tape width
RU1H36R	RU1H36R	TO-220	Tube	50	-	-

Package Information

TO-220FB-3L



SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185	$\phi p1$	1.40	1.50	1.60	0.055	0.059	0.063
A1	1.27	1.30	1.33	0.050	0.051	0.052	e	2.54BSC			0.1BSC		
A2	2.35	2.40	2.50	0.093	0.094	0.098	e1	5.08BSC			0.2BSC		
b	0.77	-	0.90	0.030	-	0.035	H1	6.40	6.50	6.60	0.252	0.256	0.260
b2	1.23	-	1.36	0.048	-	0.054	L	12.75	-	13.17	0.502	-	0.519
C	0.48	0.50	0.52	0.019	0.020	0.021	L1	-	-	3.95	-	-	0.156
D	15.40	15.60	15.80	0.606	0.614	0.622	L2	2.50REF.			0.098REF.		
D1	9.00	9.10	9.20	0.354	0.358	0.362	ϕp	3.57	3.60	3.63	0.141	0.142	0.143
DEP	0.05	0.10	0.20	0.002	0.004	0.008	Q	2.73	2.80	2.87	0.107	0.110	0.113
E	9.70	9.90	10.10	0.382	0.389	0.398	$\theta 1$	5°	7°	9°	5°	7°	9°
E1	-	8.70	-	-	0.343	-	$\theta 2$	1°	3°	5°	1°	3°	5°
E2	9.80	10.00	10.20	0.386	0.394	0.401							

ALL DIMENSIONS REFER TO JEDEC STANDARD
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS

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