



Solid State Devices, Inc.

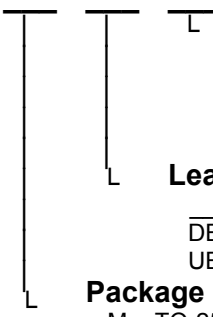
14701 Firestone Blvd * La Mirada, Ca 90638
 Phone: (562) 404-4474 * Fax: (562) 404-1773
 ssdi@ssdi-power.com * www.ssdi-power.com

SFF27N50M SFF27N50Z

27 AMP , 500 Volts, 175 mΩ Avalanche Rated N-channel MOSFET

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}
SFF27N50



Screening ^{2/}

— = Not Screened
 TX = TX Level
 TXV = TXV Level
 S = S Level

Lead Option ^{3/}

— = Straight Leads
 DB = Down Bend
 UB = Up Bend

Package ^{3/ 4/}

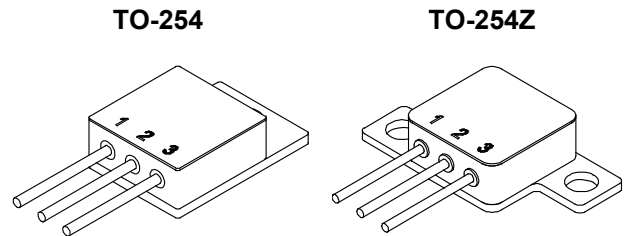
M = TO-254
 Z = TO-254Z

- Features:**
- Rugged poly-Si gate
 - Lowest ON-resistance in the industry
 - Avalanche rated
 - Hermetically Sealed, Isolated Package
 - Low Total Gate Charge
 - Fast Switching
 - TX, TXV, S-Level screening available
 - Improved ($R_{DS(ON)}$, Q_G) figure of merit

Maximum Ratings	Symbol	Value	Units
Drain - Source Voltage	V_{DSS}	500	V
Gate – Source Voltage	V_{GS}	±20 ±30	V
Max. Continuous Drain Current (package limited)	I_{D1}	27	A
Max. Instantaneous Drain Current (Tj limited)	I_{D2} I_{D3}	27 18	A
Max. Avalanche current	I_{AR}	35	A
Single and Repetitive Avalanche Energy	E_{AS} E_{AR}	1500 50	mJ
Total Power Dissipation	P_D	100	W
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +150	°C
Maximum Thermal Resistance (Junction to Case)	$R_{\theta JC}$	1.0 (typ.0.75)	°C /W

NOTES:

- *Pulse Test: Pulse Width = 300µsec, Duty Cycle = 2%.
- 1/ For ordering information, price, and availability - contact factory.
- 2/ Screening based on MIL-PRF-19500. Screening flows available on request.
- 3/ For package outlines / lead bending options / pinout configurations - contact factory.
- 4/ Maximum current limited by package configuration
- 5/ Unless otherwise specified, all electrical characteristics @25°C.





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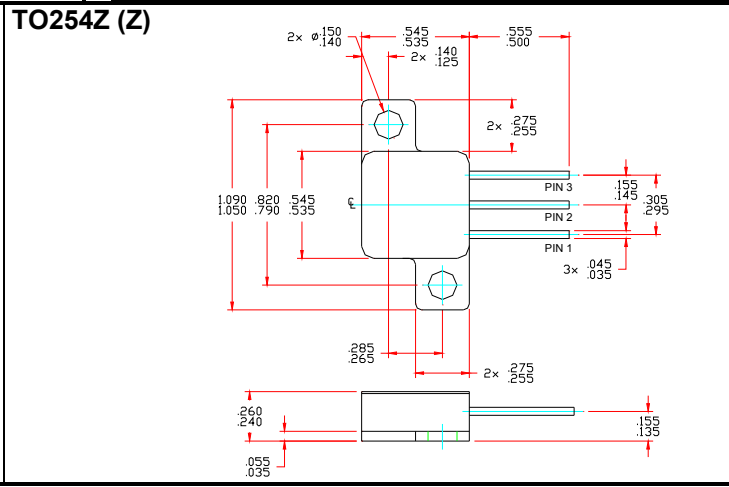
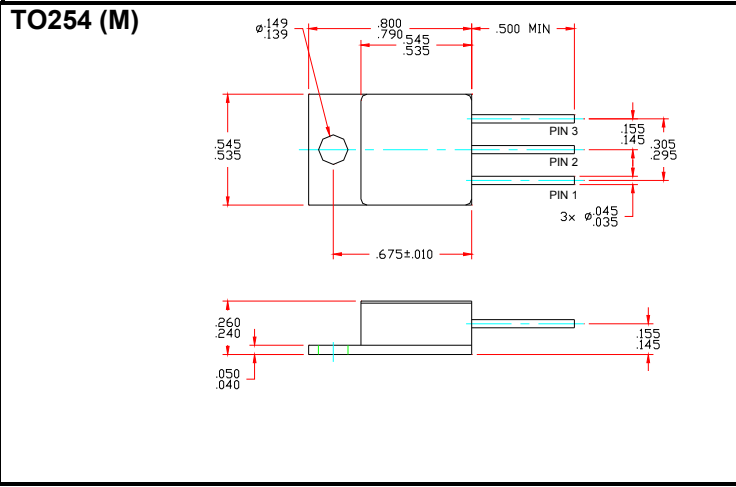
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Electrical Characteristics ^{5/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	500	510	—	V
Drain to Source On State Resistance	$V_{GS} = 10V, I_D = 18A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 18A, T_j = 125^\circ C$	$R_{DS(on)}$	— — —	150 400	175 —	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 4.0mA, T_j = 25^\circ C$ $V_{DS} = V_{GS}, I_D = 4.0mA, T_j = 125^\circ C$ $V_{DS} = V_{GS}, I_D = 4.0mA, T_j = -55^\circ C$	$V_{GS(th)}$	3.0 2.0 —	4.0 3.0 5.0	5.0 — 6	V
Gate to Source Leakage	$V_{GS} = \pm 20V, T_j = 25^\circ C$ $V_{GS} = \pm 20V, T_j = 125^\circ C$	I_{GSS}	— —	10 30	± 100 —	nA
Zero Gate Voltage Drain Current	$V_{DS} = 500V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = 500V, V_{GS} = 0V, T_j = 125^\circ C$	I_{DSS}	— —	0.01 5.0	25 500	μA μA
Forward Transconductance	$V_{DS} = 20V, I_D = 18A, T_j = 25^\circ C$	g_{fs}	15	35	—	Mho
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	75	150	nC
Gate to Source Charge	$V_{DS} = 250V$	Q_{gs}	—	25	—	
Gate to Drain Charge	$I_D = 18A$	Q_{gd}	—	25	—	
Turn on Delay Time	$V_{GS} = 10V$	$t_{d(on)}$	—	55	75	nsec
Rise Time	$V_{DS} = 250V$	t_r	—	30	50	
Turn off Delay Time	$I_D = 35A$	$t_{d(off)}$	—	65	150	
Fall Time	$R_G = 3.0\Omega, pw = 3\mu s$	t_f	—	25	50	
Diode Forward Voltage	$I_F = 35A, V_{GS} = 0V$	V_{SD}	—	0.95	1.5	V
Diode Reverse Recovery Time	$I_F = 25A, di/dt = 100A/\mu sec$	t_{rr}	—	180	250	nsec
Diode Reverse Recovery Current		I_{RM}	—	8.0	—	A
Reverse Recovery Charge		Q_{rr}	—	0.85	—	μC
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	4700	—	pF
Output Capacitance	$V_{DS} = 25V$	C_{oss}	—	540	—	
Reverse Transfer Capacitance	$f = 1 MHz$	C_{rss}	—	20	—	

Available Part Numbers:
 Consult Factory

PIN ASSIGNMENT (Standard)			
Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: F00165H

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