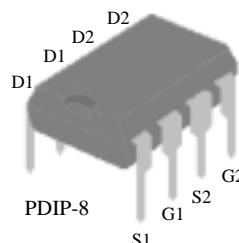
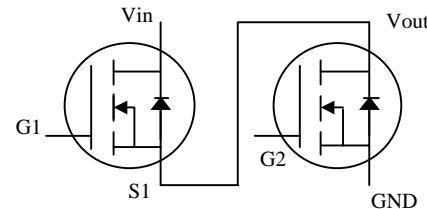


N AND P-CHANNEL
 ENHANCEMENT-MODE POWER MOSFETS

Simple drive requirement
Low on-resistance
Fast switching

Description

Power MOSFETs from Silicon Standard provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

N-ch	BV_{DSS}	20V
	$R_{DS(ON)}$	60mΩ
	I_D	2.6A
P-ch	BV_{DSS}	-20V
	$R_{DS(ON)}$	80mΩ
	I_D	-2.3A


Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 12	± 12	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current	2.6	-2.3	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current	2.1	-1.8	A
I_{DM}	Pulsed Drain Current ¹	15	-10	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation	0.625		W
	Linear Derating Factor	0.005		W/°C
T_{STG}	Storage Temperature Range	-55 to 150		°C
T_J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max. 200	°C/W

N-ch Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_{\text{D}}=250\mu\text{A}$	25	-	-	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_{\text{D}}=1\text{mA}$	-	0.037	-	$\text{V}/^\circ\text{C}$
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}}=4.5\text{V}$, $I_{\text{D}}=2.6\text{A}$	-	-	60	$\text{m}\Omega$
		$V_{\text{GS}}=2.5\text{V}$, $I_{\text{D}}=1.8\text{A}$	-	-	90	$\text{m}\Omega$
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$, $I_{\text{D}}=250\mu\text{A}$	0.5	-	1.2	V
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_{\text{D}}=2.6\text{A}$	-	3.6	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^\circ\text{C}$)	$V_{\text{DS}}=20\text{V}$, $V_{\text{GS}}=0\text{V}$	-	-	1	μA
	Drain-Source Leakage Current ($T_j=70^\circ\text{C}$)	$V_{\text{DS}}=16\text{V}$, $V_{\text{GS}}=0\text{V}$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{\text{GS}}=\pm 12\text{V}$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_{\text{D}}=2.6\text{A}$	-	9	-	nC
Q_{gs}	Gate-Source Charge	$V_{\text{DS}}=10\text{V}$	-	1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{\text{GS}}=4.5\text{V}$	-	4	-	nC
$t_{\text{d(on)}}$	Turn-on Delay Time ²	$V_{\text{DS}}=10\text{V}$	-	6.5	-	ns
t_r	Rise Time	$I_{\text{D}}=1\text{A}$	-	14	-	ns
$t_{\text{d(off)}}$	Turn-off Delay Time	$R_G=6\Omega$, $V_{\text{GS}}=4.5\text{V}$	-	20	-	ns
t_f	Fall Time	$R_{\text{D}}=10\Omega$	-	15	-	ns
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}$	-	300	-	pF
C_{oss}	Output Capacitance	$V_{\text{DS}}=8\text{V}$	-	255	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	115	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_s	Continuous Source Current (Body Diode)	$V_D=V_G=0\text{V}$, $V_S=1.2\text{V}$	-	-	1.7	A
I_{SM}	Pulsed Source Current (Body Diode) ¹		-	-	15	A
V_{SD}	Forward On Voltage ²	$T_j=25^\circ\text{C}$, $I_s=1.7\text{A}$, $V_{\text{GS}}=0\text{V}$	-	-	1.2	V

Notes:

- 1.Pulse width limited by safe operating area.
- 2.Pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$.

P-ch Electrical Characteristics@T_j=25°C(unless otherwise specified)

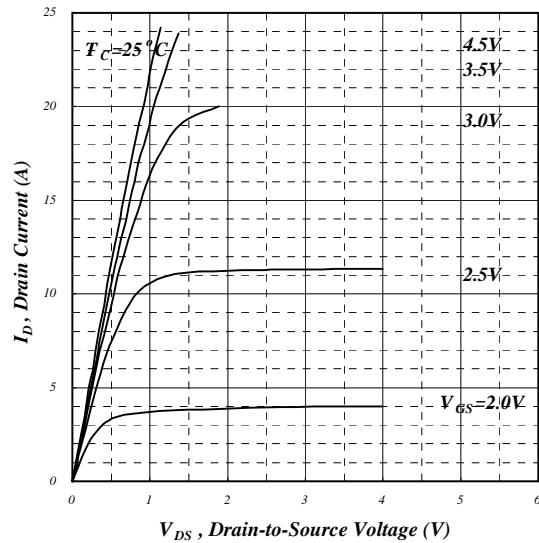
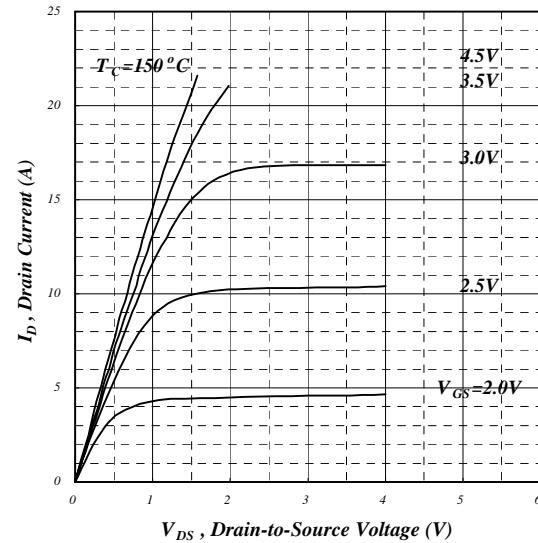
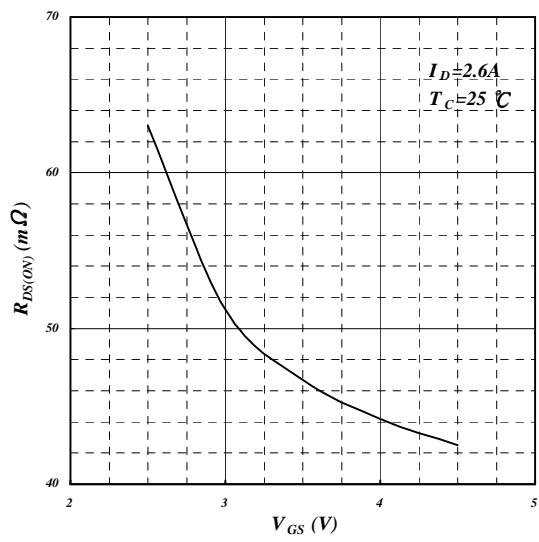
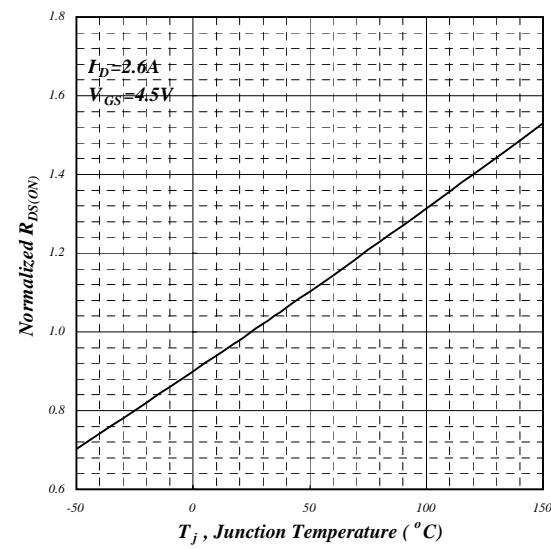
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	-25	-	-	V
Δ BV _{DSS} /Δ T _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =-1mA	-	-0.037	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-4.5V, I _D =-2.2A	-	-	80	mΩ
		V _{GS} =-2.5V, I _D =-1.8A	-	-	135	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-0.5	-	-1	V
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-2.2A	-	2.7	-	S
I _{DSS}	Drain-Source Leakage Current (T=25°C)	V _{DS} =-20V, V _{GS} =0V	-	-	-1	uA
	Drain-Source Leakage Current (T=70°C)	V _{DS} =-16V, V _{GS} =0V	-	-	-25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±12V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =-2.2A	-	11.5	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-6V	-	3.2	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-4.5V	-	1.5	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =-10V	-	10	-	ns
t _r	Rise Time	I _D =-2.2A	-	25	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω, V _{GS} =-4.5V	-	50	-	ns
t _f	Fall Time	R _D =4.5Ω	-	30	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	940	-	pF
C _{oss}	Output Capacitance	V _{DS} =-15V	-	440	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	130	-	pF

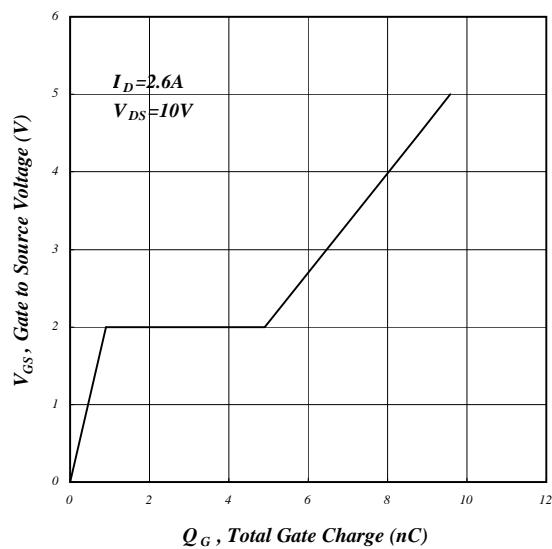
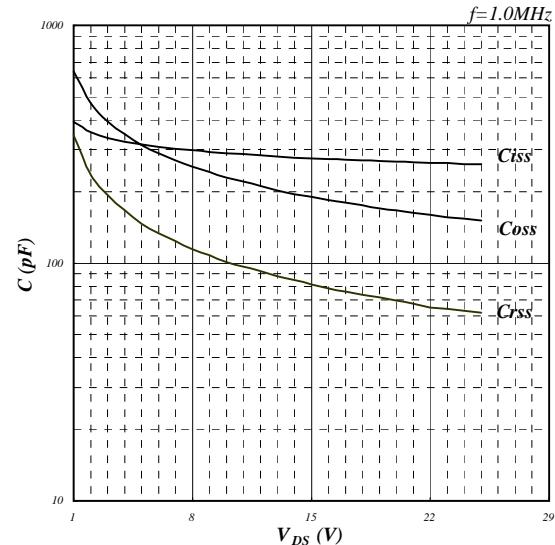
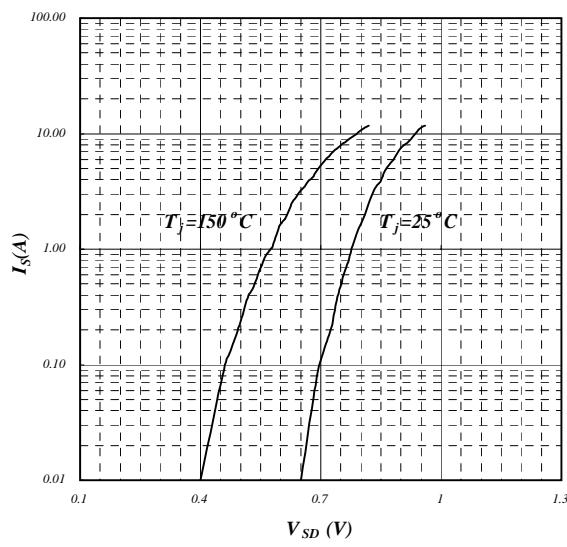
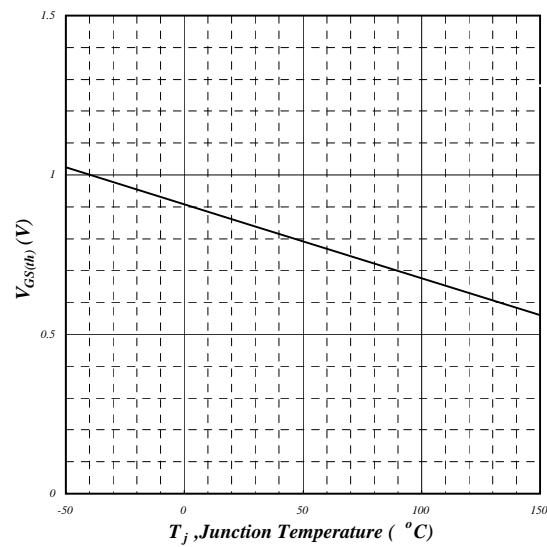
Source-Drain Diode

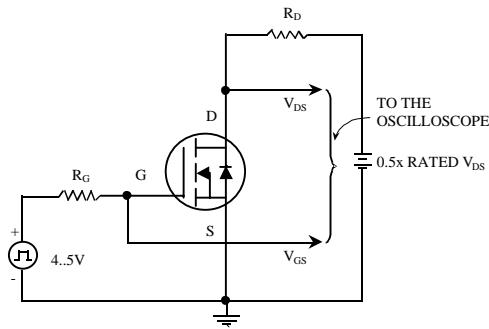
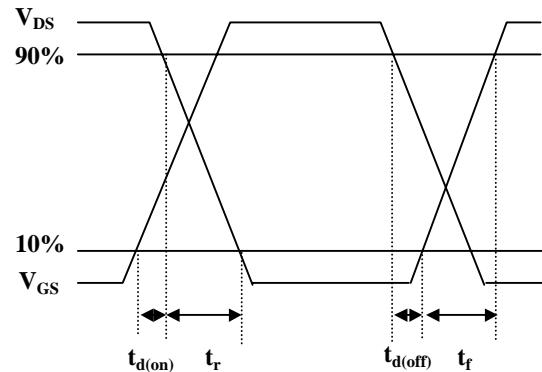
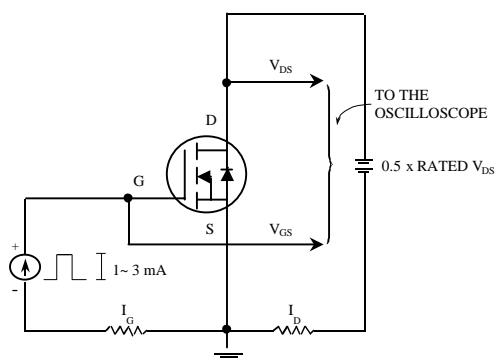
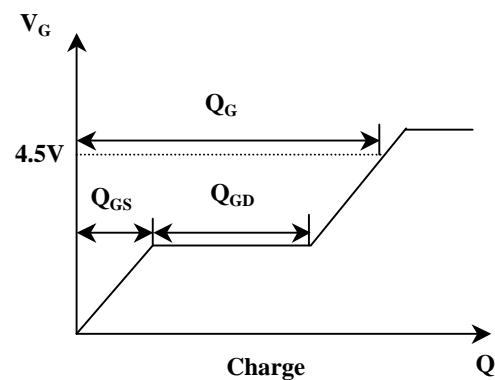
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V, V _S =-1.2V	-	-	-1.8	A
I _{SM}	Pulsed Source Current (Body Diode) ¹		-	-	-10	A
V _{SD}	Forward On Voltage ²	T _j =25°C, I _S =-1.8A, V _{GS} =0V	-	-	-1.2	V

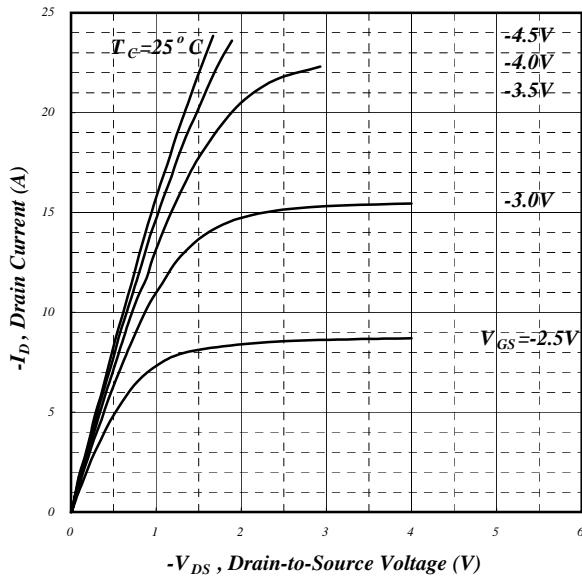
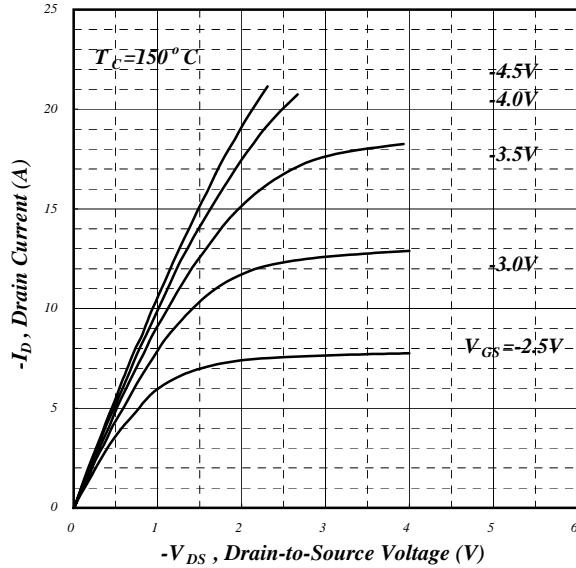
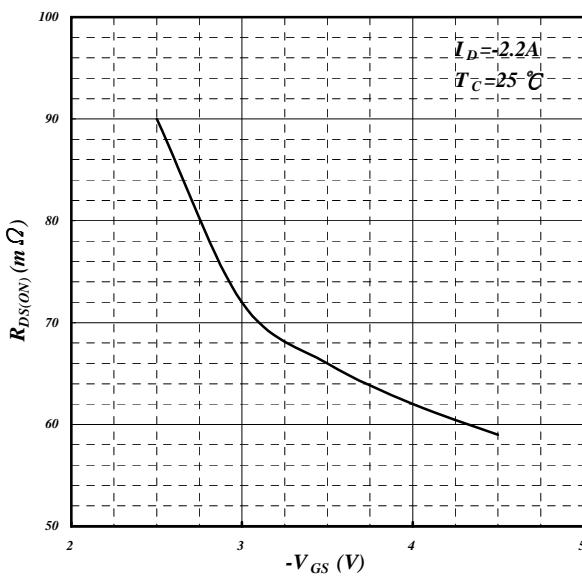
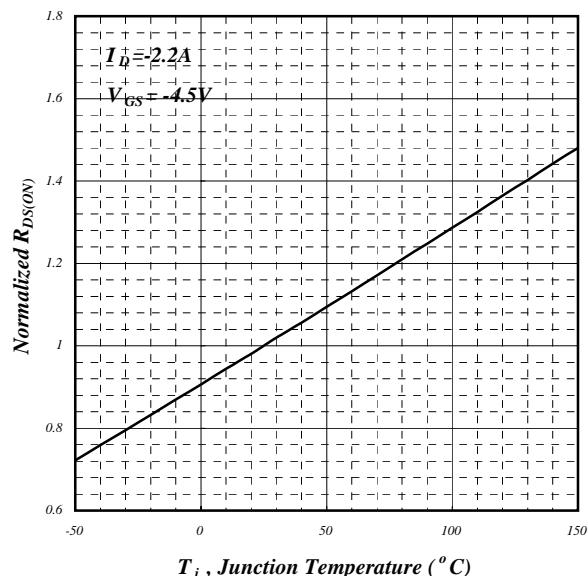
Notes:

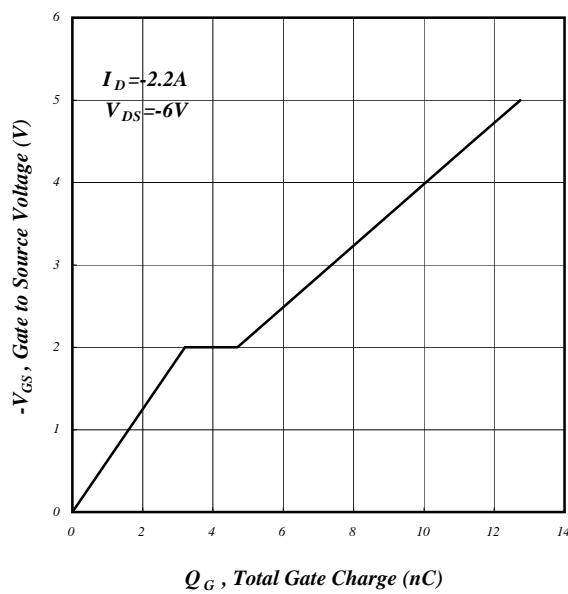
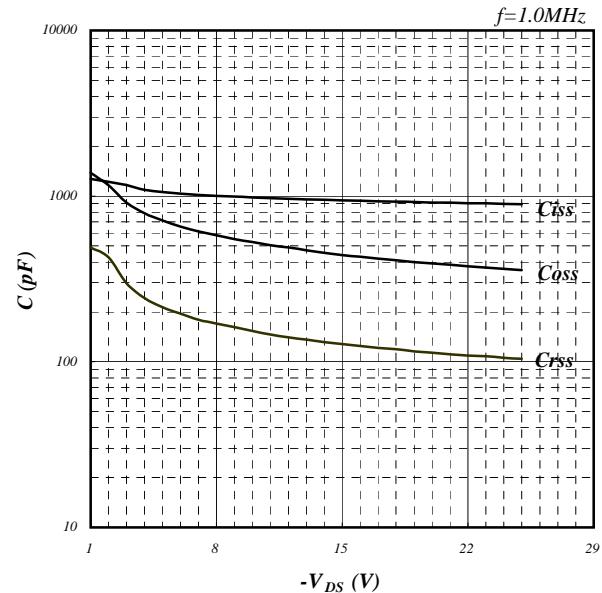
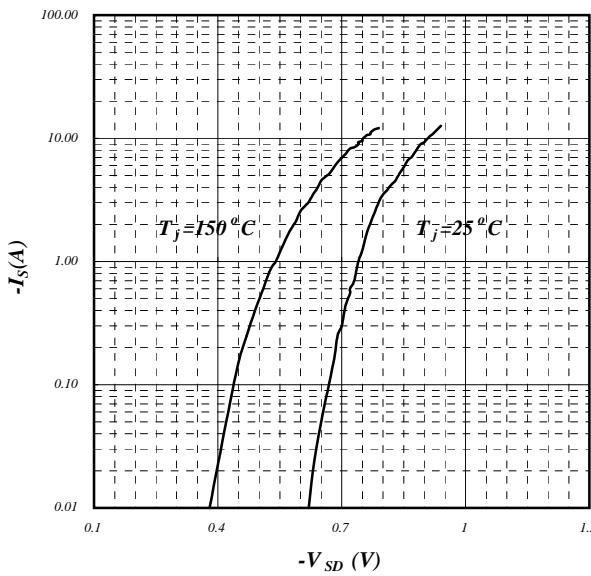
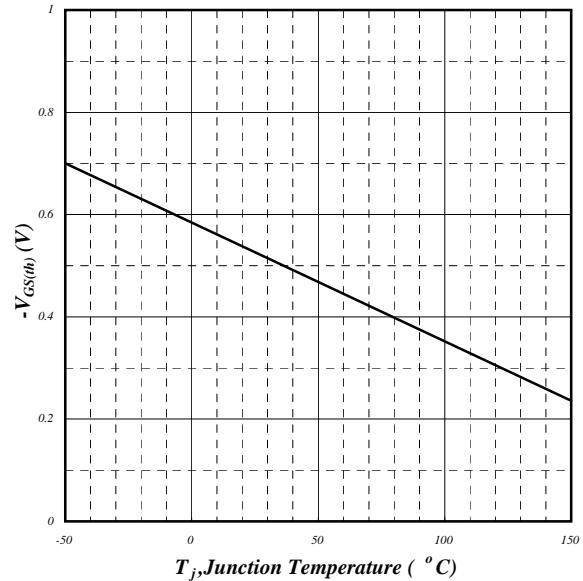
- 1.Pulse width limited by safe operating area.
- 2.Pulse width ≤300us , duty cycle ≤2%.

N-Channel

Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. On-Resistance v.s. Gate Voltage

Fig 4. Normalized On-Resistance v.s. Junction Temperature

N-Channel

Fig 9. Gate Charge Characteristics

Fig 10. Typical Capacitance Characteristics

Fig 11. Forward Characteristic of Reverse Diode

Fig 12. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

Fig 13. Switching Time Circuit

Fig 14. Switching Time Waveform

Fig 15. Gate Charge Circuit

Fig 16. Gate Charge Waveform

P-Channel

Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. On-Resistance v.s. Gate Voltage

Fig 4. Normalized On-Resistance v.s. Junction Temperature

P-Channel

Fig 9. Gate Charge Characteristics

Fig 10. Typical Capacitance Characteristics

Fig 11. Forward Characteristic of Reverse Diode

Fig 12. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

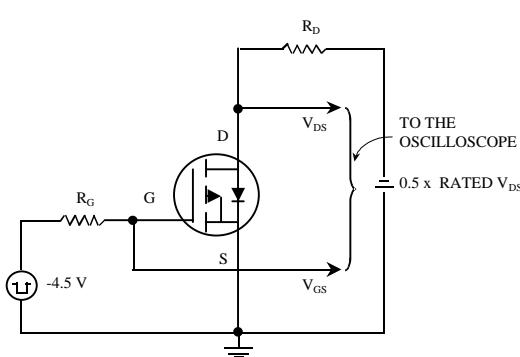


Fig 13. Switching Time Circuit

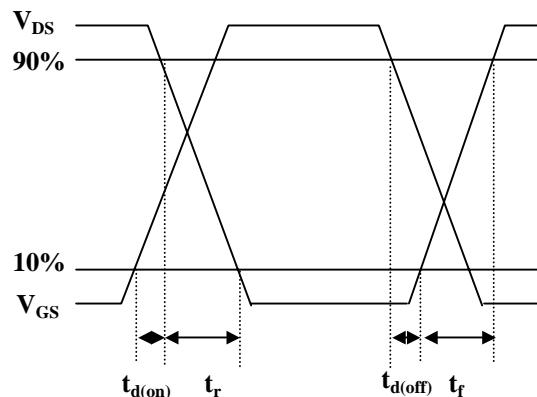


Fig 14. Switching Time Waveform

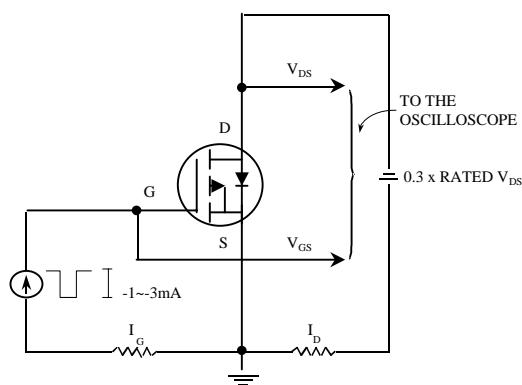


Fig 15. Gate Charge Circuit

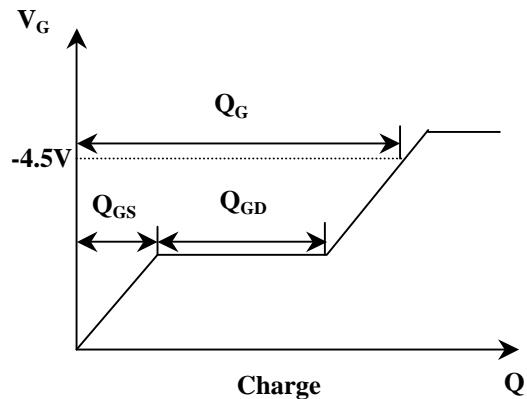


Fig 16. Gate Charge Waveform

Information furnished by Silicon Standard Corporation is believed to be accurate and reliable. However, Silicon Standard Corporation makes no guarantee or warranty, express or implied, as to the reliability, accuracy, timeliness or completeness of such information and assumes no responsibility for its use, or for infringement of any patent or other intellectual property rights of third parties that may result from its use. Silicon Standard reserves the right to make changes as it deems necessary to any products described herein for any reason, including without limitation enhancement in reliability, functionality or design. No license is granted, whether expressly or by implication, in relation to the use of any products described herein or to the use of any information provided herein, under any patent or other intellectual property rights of Silicon Standard Corporation or any third parties.