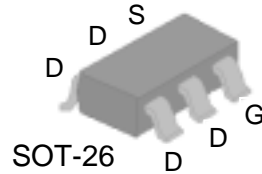


P-CHANNEL ENHANCEMENT-MODE POWER MOSFET

Simple drive requirement
 Small package outline
 Surface-mount device

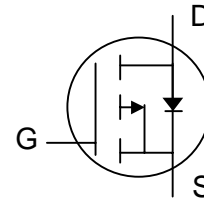


BV_{DSS} -20V
 $R_{DS(ON)}$ 65m Ω
 I_D -4.2A

Description

These power MOSFETs from Silicon Standard utilize advanced processing techniques to achieve the lowest possible on-resistance in an extremely efficient and cost-effective device.

The SOT-26 package is widely used for commercial and industrial surface-mount applications.



Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units |
|------------------------------|---------------------------------------|------------|---------------------|
| V_{DS} | Drain-Source Voltage | -20 | V |
| V_{GS} | Gate-Source Voltage | ± 12 | V |
| $I_D @ T_A=25^\circ\text{C}$ | Continuous Drain Current ³ | -4.2 | A |
| $I_D @ T_A=70^\circ\text{C}$ | Continuous Drain Current ³ | -3.4 | A |
| I_{DM} | Pulsed Drain Current ^{1,2} | -10 | A |
| $P_D @ T_A=25^\circ\text{C}$ | Total Power Dissipation | 1.56 | W |
| | Linear Derating Factor | 0.01 | W/ $^\circ\text{C}$ |
| T_{STG} | Storage Temperature Range | -55 to 150 | $^\circ\text{C}$ |
| T_J | Operating Junction Temperature Range | -55 to 150 | $^\circ\text{C}$ |

Thermal Data

| Symbol | Parameter | Value | Unit |
|---------------|--|---------|---------------------------|
| $R_{thj-amb}$ | Thermal Resistance Junction-ambient ³ | Max. 80 | $^\circ\text{C}/\text{W}$ |

Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|------------------------------|---|--|------|------|-----------|---------------------|
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS}=0V, I_D=-250\mu A$ | -20 | - | - | V |
| $\Delta BV_{DSS}/\Delta T_j$ | Breakdown Voltage Temperature Coefficient | Reference to $25^\circ\text{C}, I_D=-1\text{mA}$ | - | -0.1 | - | V/ $^\circ\text{C}$ |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance ² | $V_{GS}=-10V, I_D=-4.5A$ | - | - | 53 | m Ω |
| | | $V_{GS}=-4.5V, I_D=-4.2A$ | - | - | 65 | m Ω |
| | | $V_{GS}=-2.5V, I_D=-2.0A$ | - | - | 120 | m Ω |
| | | $V_{GS}=-1.8V, I_D=-1.0A$ | - | - | 250 | m Ω |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}=V_{GS}, I_D=-250\mu A$ | -0.5 | - | -1.2 | V |
| g_{fs} | Forward Transconductance | $V_{DS}=-5V, I_D=-2.8A$ | - | 9 | - | S |
| I_{DSS} | Drain-Source Leakage Current ($T_j=25^\circ\text{C}$) | $V_{DS}=-20V, V_{GS}=0V$ | - | - | -1 | μA |
| | Drain-Source Leakage Current ($T_j=55^\circ\text{C}$) | $V_{DS}=-16V, V_{GS}=0V$ | - | - | -10 | μA |
| I_{GSS} | Gate-Source Leakage | $V_{GS}=\pm 12V$ | - | - | ± 100 | nA |
| Q_g | Total Gate Charge ² | $I_D=-4.2A$ | - | 10.6 | 16 | nC |
| Q_{gs} | Gate-Source Charge | $V_{DS}=-16V$ | - | 2.32 | - | nC |
| Q_{gd} | Gate-Drain ("Miller") Charge | $V_{GS}=-4.5V$ | - | 3.68 | - | nC |
| $t_{d(on)}$ | Turn-on Delay Time ² | $V_{DS}=-15V$ | - | 5.9 | - | ns |
| t_r | Rise Time | $I_D=-4.2A$ | - | 3.6 | - | ns |
| $t_{d(off)}$ | Turn-off Delay Time | $R_G=6\Omega, V_{GS}=-10V$ | - | 32.4 | - | ns |
| t_f | Fall Time | $R_D=3.6\Omega$ | - | 2.6 | - | ns |
| C_{iss} | Input Capacitance | $V_{GS}=0V$ | - | 740 | 1200 | pF |
| C_{oss} | Output Capacitance | $V_{DS}=-15V$ | - | 167 | - | pF |
| C_{rss} | Reverse Transfer Capacitance | $f=1.0\text{MHz}$ | - | 126 | - | pF |

Source-Drain Diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|----------|---------------------------------|-------------------------|------|------|------|-------|
| V_{SD} | Forward On Voltage ² | $I_S=-1.2A, V_{GS}=0V$ | - | - | -1.2 | V |
| t_{rr} | Reverse Recovery Time | $I_S=-4.2A, V_{GS}=0V,$ | - | 27.7 | - | ns |
| Q_{rr} | Reverse Recovery Charge | $dI/dt=100A/\mu s$ | - | 22 | - | nC |

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- 3.Surface mounted on 1 in² copper pad of FR4 board ; 160 $^\circ\text{C}/\text{W}$ when mounted on min. copper pad.

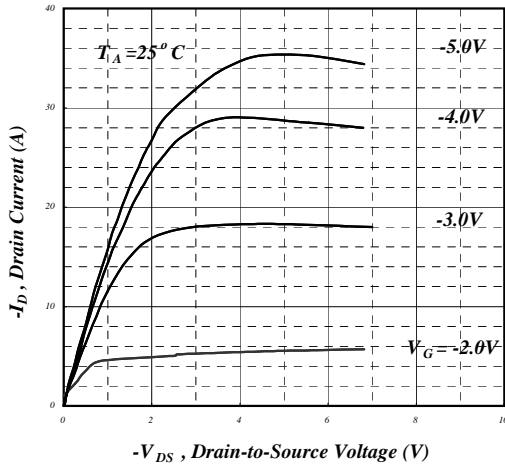


Fig 1. Typical Output Characteristics

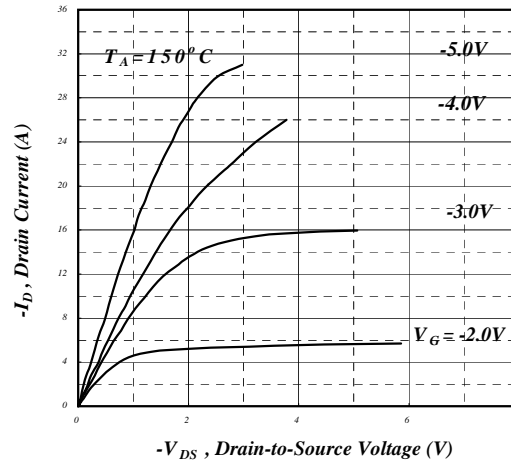


Fig 2. Typical Output Characteristics

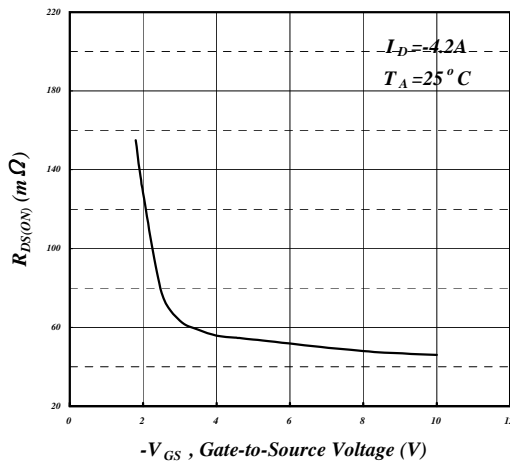


Fig 3. On-Resistance v.s. Gate Voltage

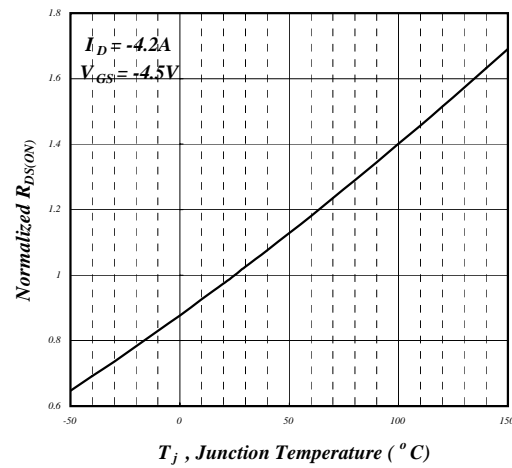


Fig 4. Normalized On-Resistance vs. Junction Temperature

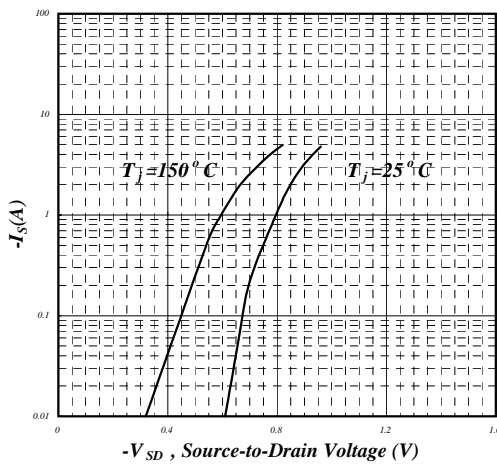


Fig 5. Forward Characteristic of Reverse Diode

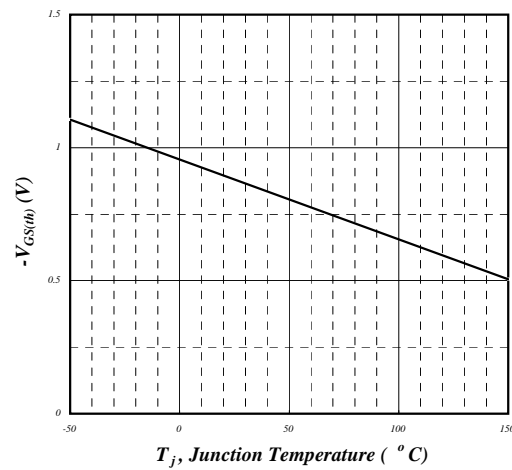


Fig 6. Gate Threshold Voltage vs. Junction Temperature

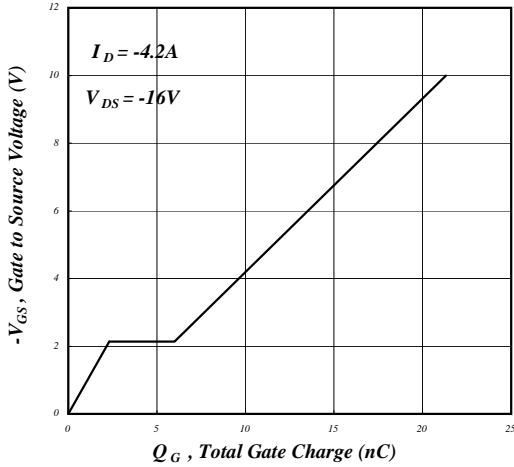


Fig 7. Gate Charge Characteristics

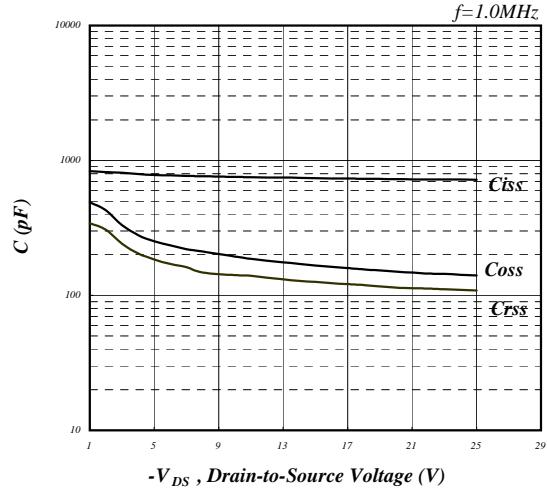


Fig 8. Typical Capacitance Characteristics

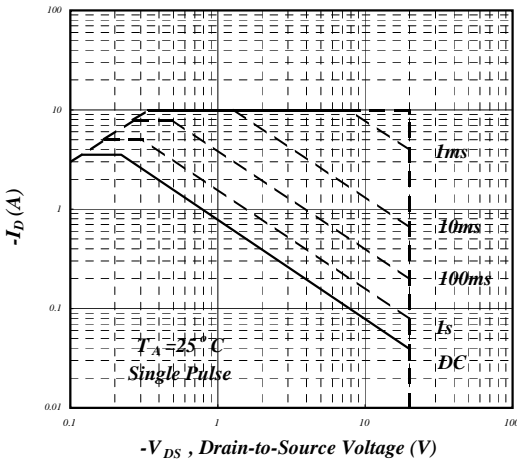


Fig 9. Maximum Safe Operating Area

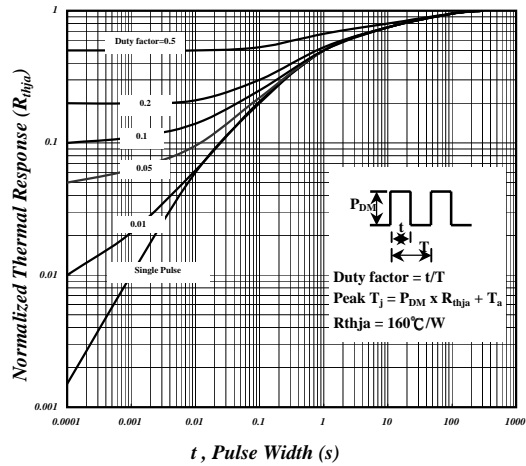


Fig 10. Effective Transient Thermal Impedance

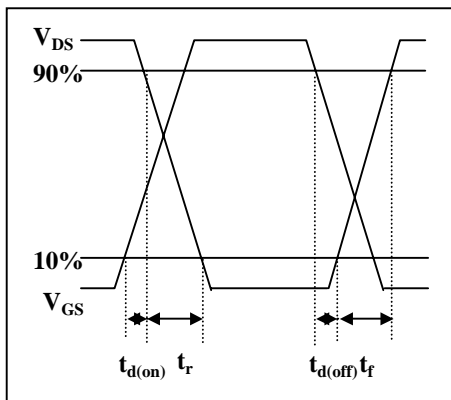


Fig 11. Switching Time Waveform

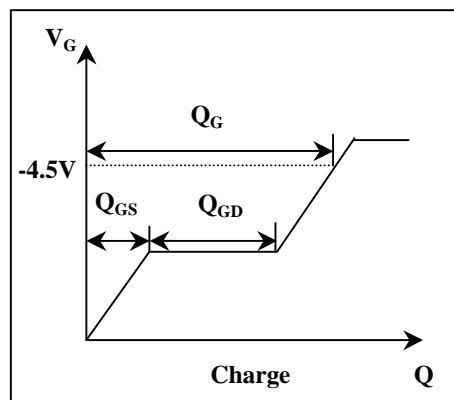


Fig 12. Gate Charge Waveform

Information furnished by Silicon Standard Corporation is believed to be accurate and reliable. However, Silicon Standard Corporation makes no guarantee or warranty, express or implied, as to the reliability, accuracy, timeliness or completeness of such information and assumes no responsibility for its use, or for infringement of any patent or other intellectual property rights of third parties that may result from its use. Silicon Standard reserves the right to make changes as it deems necessary to any products described herein for any reason, including without limitation enhancement in reliability, functionality or design. No license is granted, whether expressly or by implication, in relation to the use of any products described herein or to the use of any information provided herein, under any patent or other intellectual property rights of Silicon Standard Corporation or any third parties.