# SGS-THOMSON MICROELECTRONICS

# N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

| TYPE | V$_{DSS}$ | R$_{DS(on)}$ | I$_D$ |
|------|-----|------|----|
| STK2N80 | 800 V | 7 Ω | 2.1 A |

- AVALANCHE RUGGEDNESS TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW INPUT CAPACITANCE
- LOW GATE CHARGE
- LOW LEAKAGE CURRENT SPECIFIED AT MAXIMUM VOLTAGE
- "DIPS" EDGE TERMINATION TO SUSTAIN HIGH VOLTAGE
- APPLICATION ORIENTED CHARACTERIZATION

**APPLICATIONS**

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- CONSUMER AND INDUSTRIAL LIGHTING
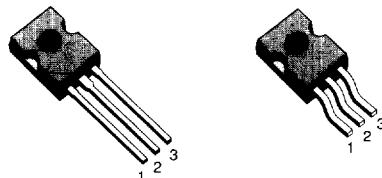


SOT-82

SOT-194 (option)

**INTERNAL SCHEMATIC DIAGRAM**
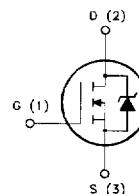


**ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| V$_{DS}$ | Drain-source Voltage (V$_{GS}$ = 0) | 800 | V |
| V$_{DGR}$ | Drain- gate Voltage (R$_{GS}$ = 20 kΩ) | 800 | V |
| V$_{GS}$ | Gate-source Voltage | ± 20 | V |
| I$_D$ | Drain Current (continuous) at T$_c$ = 25 °C | 2.1 | A |
| I$_D$ | Drain Current (continuous) at T$_c$ = 100 °C | 1.3 | A |
| I$_{DM}$(•) | Drain Current (pulsed) | 9.6 | A |
| P$_{tot}$ | Total Dissipation at T$_c$ = 25 °C | 70 | W |
| | Derating Factor | 0.56 | W/°C |
| T$_{stg}$ | Storage Temperature | -65 to 150 | °C |
| T$_j$ | Max. Operating Junction Temperature | 150 | °C |

(•) Pulse width limited by safe operating area

June 1992

# STK2N80

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{thj-case}$ | Thermal Resistance Junction-case | Max | 1.78 | °C/W |
| $R_{thj-amb}$ | Thermal Resistance Junction-ambient | Max | 80 | °C/W |
| $R_{thj-amb}$ | Thermal Resistance Case-sink | Typ | 0.7 | °C/W |
| $T_l$ | Maximum Lead Temperature For Soldering Purpose | | 275 | °C |

## AVALANCHE CHARACTERISTICS

| Symbol | Parameter | Max Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max, $\delta$ < 1%) | 2.1 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (starting $T_j$ = 25 °C, $I_D = I_{AR}$, $V_{DD}$ = 25 V) | 80 | mJ |
| $E_{AR}$ | Repetitive Avalanche Energy (pulse width limited by $T_j$ max, $\delta$ < 1%) | 2.8 | mJ |
| $I_{AR}$ | Avalanche Current, Repetitive or Not-Repetitive ($T_c$ = 100 °C, pulse width limited by $T_j$ max, $\delta$ < 1%) | 1.3 | A |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25 °C unless otherwise specified)

OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D$ = 250 µA   $V_{GS}$ = 0 | 800 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current ($V_{GS}$ = 0) | $V_{DS}$ = Max Rating<br>$V_{DS}$ = Max Rating x 0.8   $T_c$ = 125 °C | | | 250<br>1000 | µA<br>µA |
| $I_{GSS}$ | Gate-body Leakage Current ($V_{DS}$ = 0) | $V_{GS}$ = ± 20 V | | | ± 100 | nA |

ON (*)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}$   $I_D$ = 250 µA | 2 | | 4 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS}$ = 10V   $I_D$ = 1 A<br>$V_{GS}$ = 10V   $I_D$ = 1 A   $T_c$ = 100°C | | | 7<br>14 | Ω<br>Ω |
| $I_{D(on)}$ | On State Drain Current | $V_{DS} > I_{D(on)}$ x $R_{DS(on)max}$<br>$V_{GS}$ = 10 V | 2.1 | | | A |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (*) | Forward Transconductance | $V_{DS} > I_{D(on)}$ x $R_{DS(on)max}$    $I_D$ = 1 A | 1.2 | | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input Capacitance<br>Output Capacitance<br>Reverse Transfer Capacitance | $V_{DS}$ = 25 V   f = 1 MHz   $V_{GS}$ = 0 | | | 600<br>70<br>30 | pF<br>pF<br>pF |

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## ELECTRICAL CHARACTERISTICS (continued)

### SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------------|------|------|------|------|
| $t_{d(on)}$ | Turn-on Time | $V_{DD} = 400$ V $\quad I_D = 1.5$ A | | | 50 | ns |
| $t_r$ | Rise Time | $R_G = 50$ $\Omega$ $\quad V_{GS} = 10$ V | | | 57 | ns |
| | | (see test circuit, figure 3) | | | | |
| $(di/dt)_{on}$ | Turn-on Current Slope | $V_{DD} = 640$ V $\quad I_D = 2$ A | | 160 | | A/$\mu$s |
| | | $R_G = 50$ $\Omega$ $\quad V_{GS} = 10$ V | | | | |
| | | (see test circuit, figure 5) | | | | |
| $Q_g$ | Total Gate Charge | $V_{DD} = 640$ V $\quad I_D = 2$ A $\quad V_{GS} = 10$ V | | 31 | 40 | nC |

### SWITCHING OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------------|------|------|------|------|
| $t_{r(Voff)}$ | Off-voltage Rise Time | $V_{DD} = 640$ V $\quad I_D = 2$ A | | | 90 | ns |
| $t_f$ | Fall Time | $R_G = 50$ $\Omega$ $\quad V_{GS} = 10$ V | | | 32 | ns |
| $t_c$ | Cross-over Time | (see test circuit, figure 5) | | | 130 | ns |

### SOURCE DRAIN DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------------|------|------|------|------|
| $I_{SD}$ | Source-drain Current | | | | 2.1 | A |
| $I_{SDM}(\bullet)$ | Source-drain Current (pulsed) | | | | 9.6 | A |
| $V_{SD}$ (*) | Forward On Voltage | $I_{SD} = 2.1$ A $\quad V_{GS} = 0$ | | | 2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_{SD} = 2$ A $\quad di/dt = 100$ A/$\mu$s | | 920 | | ns |
| $Q_{rr}$ | Reverse Recovery Charge | $V_{DD} = 100$ V $\quad T_j = 150$ $^\circ$C (see test circuit, figure 5) | | 18.4 | | $\mu$C |
| $I_{RRM}$ | Reverse Recovery Current | | | 40 | | A |

(*) Pulsed: Pulse duration = 300 $\mu$s, duty cycle 1.5 %

(•) Pulse width limited by safe operating area

Safe Operating Area

Thermal Impedance

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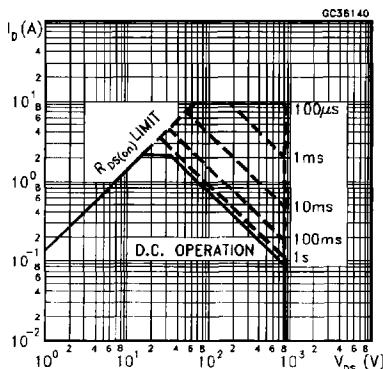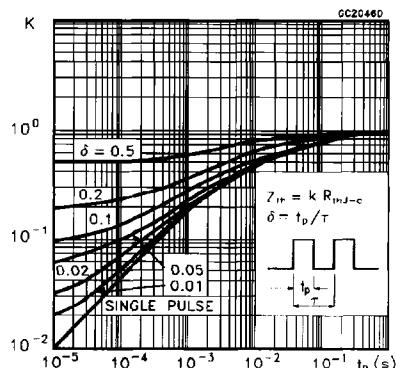
## Derating Curve
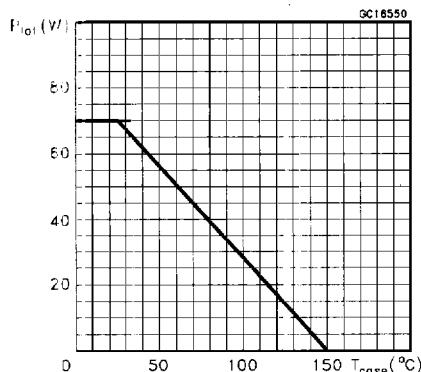


## Output Characteristics
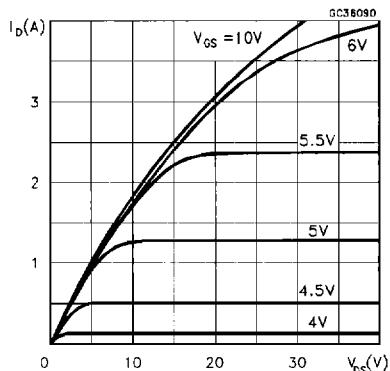


## Transfer Characteristics
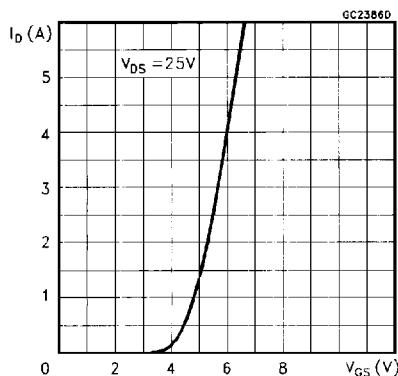


## Transconductance
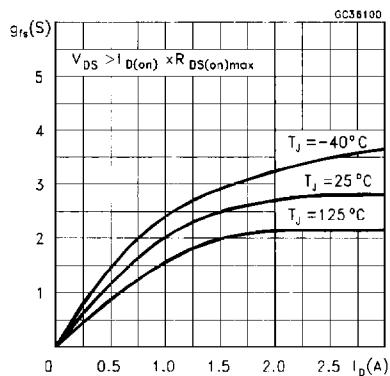


## Static Drain-source On Resistance
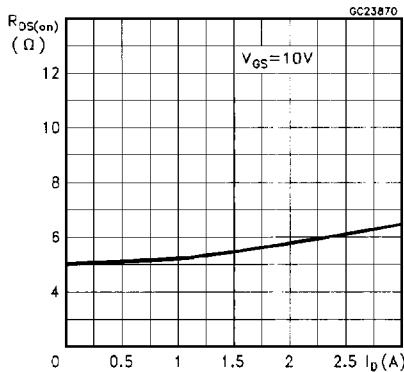


## Gate Charge vs Gate-source Voltage

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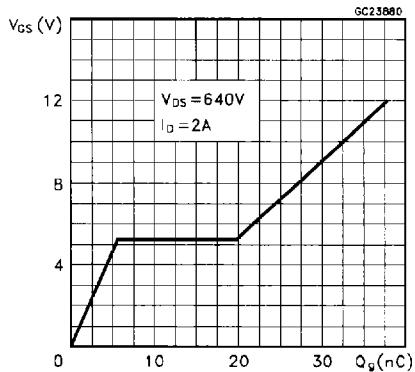
Capacitance Variations
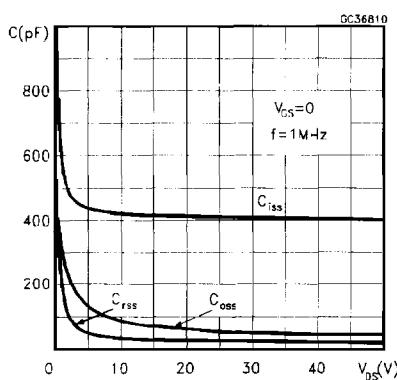


Normalized Gate Threshold Voltage vs Temperature
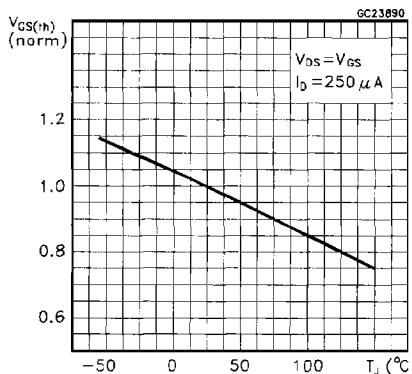


Normalized On Resistance vs Temperature
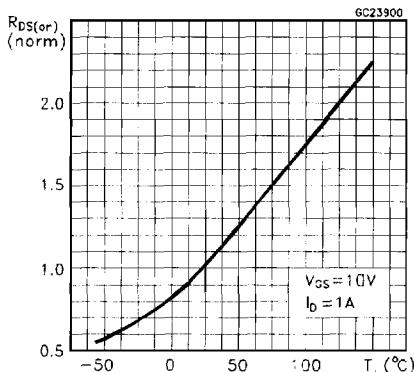


Turn-on Current Slope
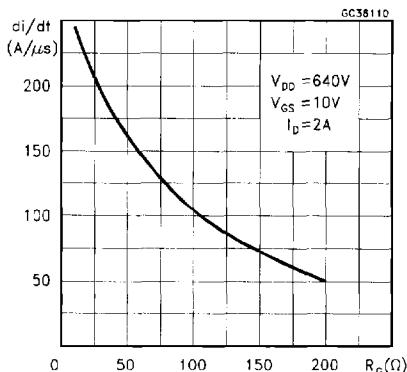


Turn-off Drain-source Voltage Slope
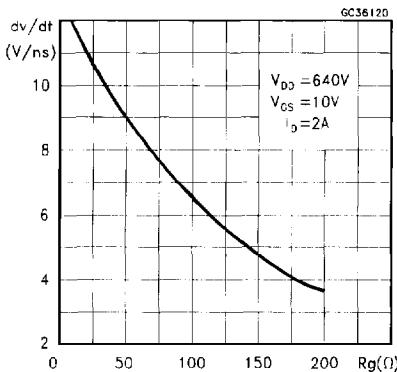


Cross-over Time
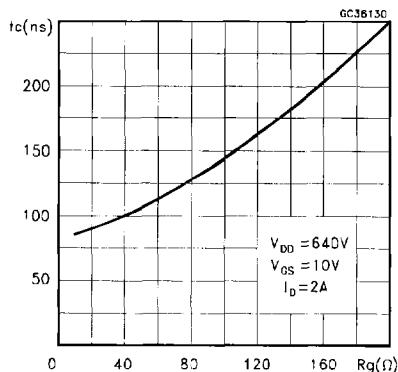
Switching Safe Operating Area
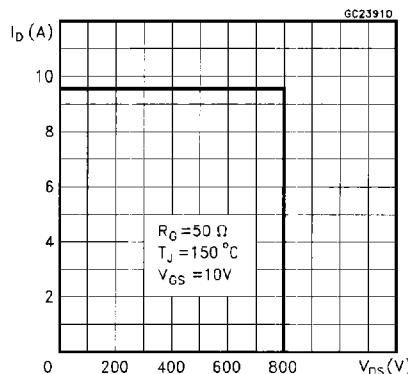


Accidental Overload Area
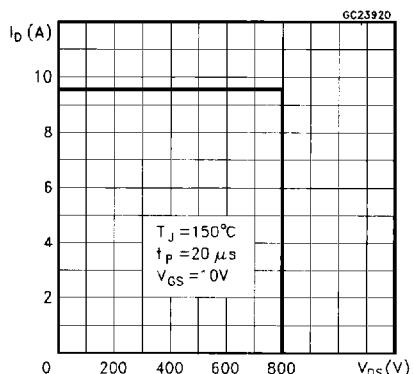


Source-drain Diode Forward Characteristics
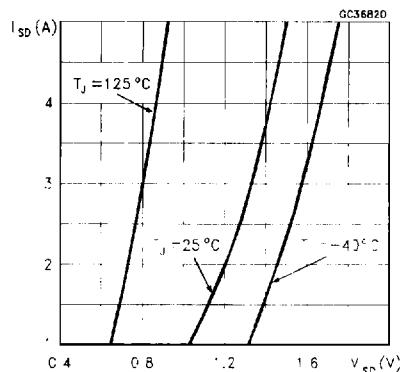


**Fig. 1:** Unclamped Inductive Load Test Circuits

**Fig. 2:** Unclamped Inductive Waveforms





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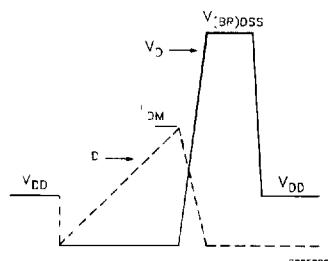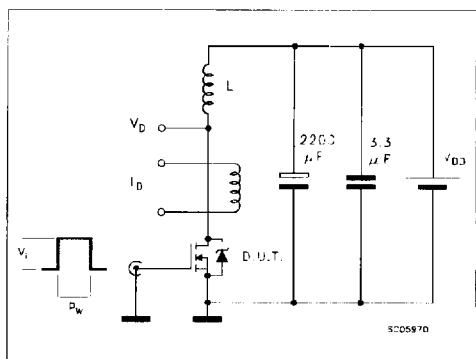
**Fig. 3:** Switching Times Test Circuits For Resistive Load
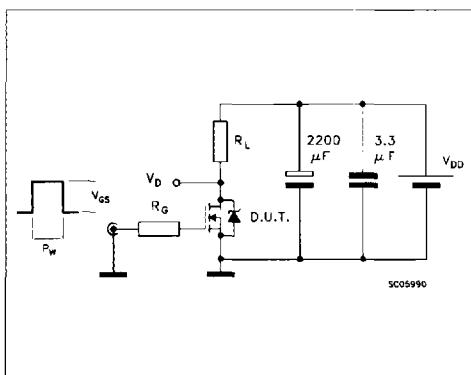


**Fig. 4:** Gate Charge Test Circuit
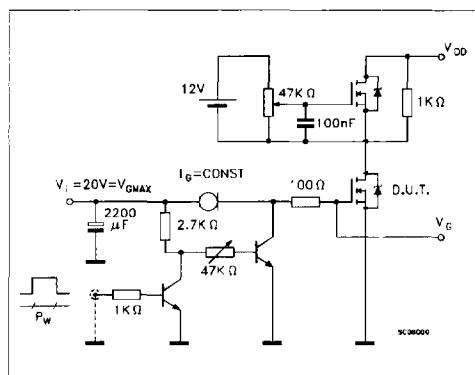


**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times

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