



Pin Definition:
 1. Source
 2. Source
 3. Source
 4. Gate
 5, 6, 7, 8. Drain

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (m Ω)	I_D (A)
-30	18 @ $V_{GS} = -10V$	-9.6
	30 @ $V_{GS} = -4.5V$	-7.5

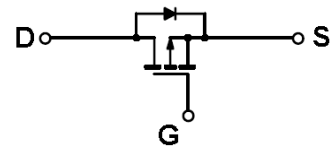
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switches
- Desktop PCs
- Notebook PCs

Block Diagram



P-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM4835CS RL	SOP-8	2.5Kpcs / 13" Ree

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current	I_D	-9.6	A
Pulsed Drain Current	I_{DM}	-50	A
Continuous Source Current (Diode Conduction) ^{a,b}	I_S	-2.1	A
Maximum Power Dissipation	P_D	Ta = 25°C	2.5
		Ta = 75°C	1.6
Operating Junction Temperature	T_J	+150	°C
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Foot (Drain) Thermal Resistance	$R_{\theta_{JF}}$	18	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta_{JA}}$	39	°C/W

Notes:

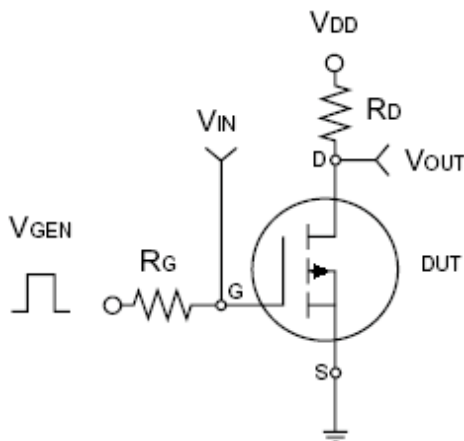
- a. Pulse width limited by the Maximum junction temperature
- b. Surface Mounted on FR4 Board, t ≤ 10 sec.

Electrical Specifications (Ta = 25°C unless otherwise noted)

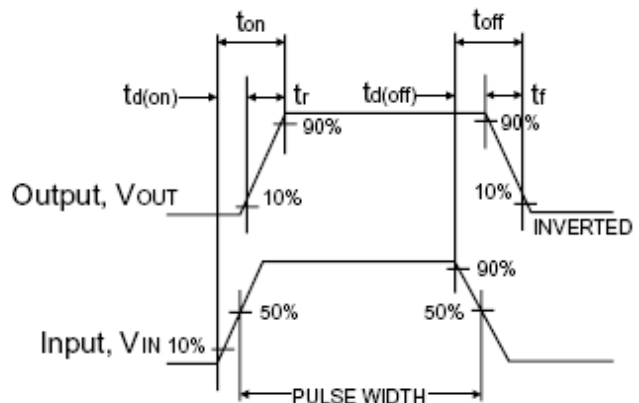
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-30	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-1	--	-3	V
Gate Body Leakage	$V_{GS} = \pm 25V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = -30V, V_{GS} = 0V$	I_{DSS}	--	--	-1.0	μA
On-State Drain Current ^a	$V_{DS} \leq -5V, V_{GS} = -10V$	$I_{D(ON)}$	-50	--	--	A
Drain-Source On-State Resistance ^a	$V_{GS} = -10V, I_D = -9.6A$	$R_{DS(ON)}$	--	14	18	m Ω
	$V_{GS} = -4.5V, I_D = -7.5A$		--	23	30	
Forward Transconductance ^a	$V_{DS} = -15V, I_D = -9.6A$	g_{fs}	--	30	--	S
Diode Forward Voltage	$I_S = -2.1A, V_{GS} = 0V$	V_{SD}	--	-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	$V_{DS} = -15V, I_D = -9.6A, V_{GS} = -5V$	Q_g	--	25	37	nC
Gate-Source Charge		Q_{gs}	--	6.5	--	
Gate-Drain Charge		Q_{gd}	--	12.5	--	
Input Capacitance	$V_{DS} = -15V, V_{GS} = 0V, f = 1.0MHz$	C_{iss}	--	2089	2347	pF
Output Capacitance		C_{oss}	--	597	--	
Reverse Transfer Capacitance		C_{rss}	--	495	624	
Switching^c						
Turn-On Delay Time	$V_{DD} = -15V, R_L = 15\Omega, I_D = -1A, V_{GEN} = -10V, R_G = 6\Omega$	$t_{d(on)}$	--	15	25	nS
Turn-On Rise Time		t_r	--	13	20	
Turn-Off Delay Time		$t_{d(off)}$	--	60	100	
Turn-Off Fall Time		t_f	--	45	70	

Notes:

- a. pulse test: PW $\leq 300\mu S$, duty cycle $\leq 2\%$
- b. For DESIGN AID ONLY, not subject to production testing.
- b. Switching time is essentially independent of operating temperature.

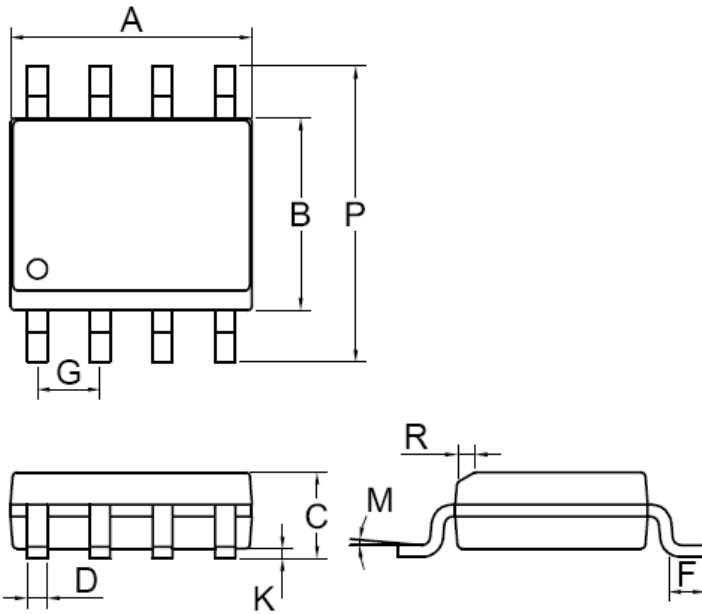


Switching Test Circuit



Switchin Waveforms

SOP-8 Mechanical Drawing



DIM	SOP-8 DIMENSION			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019



Preliminary

TSM4835
30V P-Channel MOSFET

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