

30V N-Channel MOSFET



SOP-8



Pin Definition:

- 1. Source
- 2. Source
- 3. Source
- 4. Gate
- 5, 6, 7, 8. Drain

PRODUCT SUMMARY

V _{DS} (V)	$R_{DS(on)}(m\Omega)$	I _D (A)
30	30 @ V _{GS} = 10V	8.5
	33 @ V _{GS} = 4.5V	8.5
	48 @ V _{GS} = 2.5V	5

Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

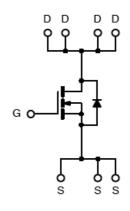
Application

- High-Side DC/DC Conversion
- Notebook
- Sever

Ordering Information

Part No.	Package	Packing
TSM4404CS RL	SOP-8	2.5Kpcs / 13" Reel

Block Diagram



N-Channel MOSFET

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V_{GS}	±12	V	
Continuous Drain Current		I _D	8.5	А	
Pulsed Drain Current		I _{DM}	60	Α	
Continuous Source Current (Diode Co	nduction) ^{a,b}	l _s 4.3		Α	
Maximum Power Dissipation	Ta = 25°C	- P _D	3.0	W	
	Ta = 75°C		2.1		
Operating Junction Temperature		TJ	+150	°C	
Operating Junction and Storage Temperature Range		T _J , T _{STG}	- 55 to +150	°C	

Thermal Performance

Parameter	Symbol	Limit	Unit		
Junction to Case Thermal Resistance	$R\Theta_{JF}$	24	°C/W		
Junction to Ambient Thermal Resistance (PCB mounted)	RO _{JA}	62.5	°C/W		

Notes:

- a. Pulse width limited by the Maximum junction temperature
- b. Surface Mounted on FR4 Board, t ≤ 10 sec.

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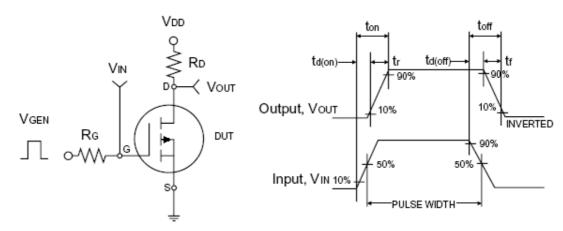


Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Тур	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250uA$	BV _{DSS}	30	1		V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	$V_{GS(TH)}$	0.7	1	1.4	V
Gate Body Leakage	$V_{GS} = \pm 12V, V_{DS} = 0V$	I _{GSS}		-	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 24V, V _{GS} =0V	I _{DSS}		-	1.0	μA
	$V_{GS} = 10V, I_D = 8.5A$	Б		24	30	mΩ
Drain-Source On-State Resistance ^a	$V_{GS} = 4.5V, I_D = 8.5A$	$R_{DS(ON)}$		27	33	
	$V_{GS} = 2.5V, I_D = 5A$			40	48	
Forward Transconductance ^a	V_{DS} = 5V, I_D =5A	g _{fs}		16		S
Diode Forward Voltage	I _S = 1A, V _{GS} =0V	V_{SD}		0.76	1.0	V
Dynamic ^b						
Total Gate Charge	\/ - 15\/ - 0.5 \	Q_g		9.7	12	
Gate-Source Charge	$I_{DS} = 15V, I_D = 8.5A,$ $I_{CS} = 4.5V$	Q_gs		1.63		nC
Gate-Drain Charge	V _{GS} - 4.5V	Q_{gd}		3.1		
Input Capacitance	\\ -45\\\\ -0\\	C _{iss}		857	1030	
Output Capacitance	$V_{DS} = 15V, V_{GS} = 0V,$ f = 1.0MHz	C _{oss}		97		pF
Reverse Transfer Capacitance	1 - 1.0IVITZ	C_{rss}		71		
Switching ^c						
Turn-On Delay Time	\\ -45\\ D -400	t _{d(on)}	-	3.3	5	
Turn-On Rise Time	$V_{DD} = 15V, R_L = 1.8\Omega,$	t _r		4.7	7	nC
Turn-Off Delay Time	$I_D = 1A, V_{GEN} = 10V,$ $R_G = 6\Omega$	t _{d(off)}		26	39	nS
Turn-Off Fall Time	17G - 022	t _f		4.1	6.2	

Notes:

- a. pulse test: PW ≤300µS, duty cycle ≤2%
- b. For DESIGN AID ONLY, not subject to production testing.b. Switching time is essentially independent of operating temperature.



Switching Test Circuit

Switchin Waveforms

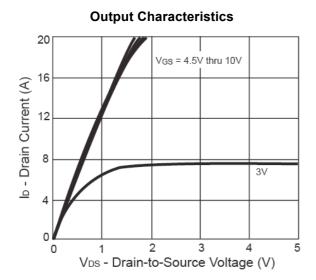
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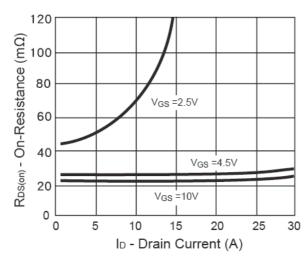
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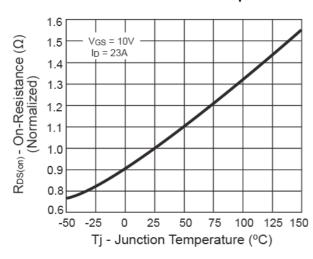
Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)



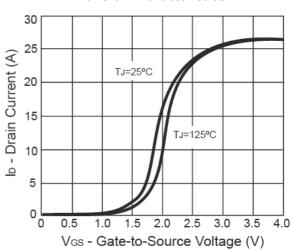
On-Resistance vs. Drain Current



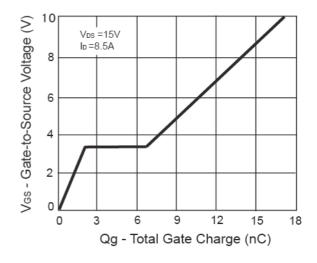
On-Resistance vs. Junction Temperature



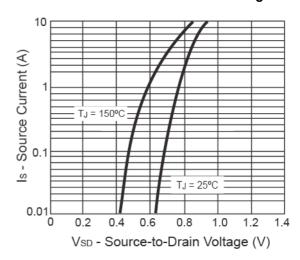
Transfer Characteristics



Gate Charge



Source-Drain Diode Forward Voltage



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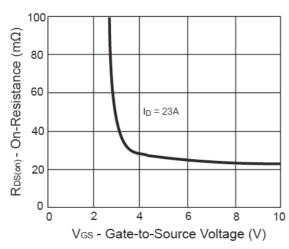


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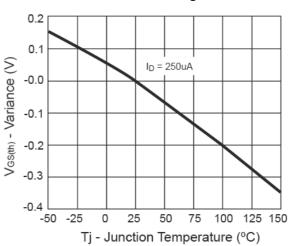


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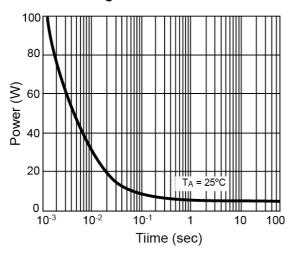
On-Resistance vs. Gate-Source Voltage



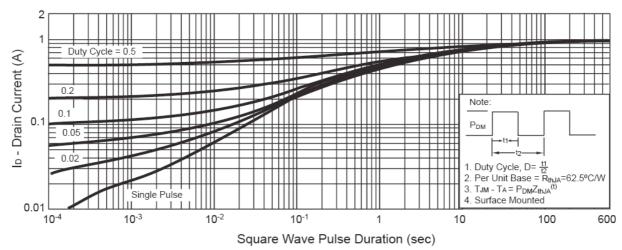
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



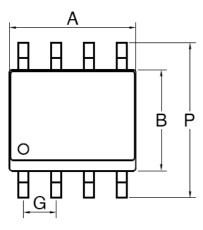
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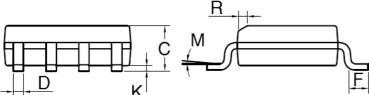
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SOP-8 Mechanical Drawing



SOP-8 DIMENSION					
DIM	MILLIMETERS		INCHES		
	MIN	MAX	MIN	MAX.	
Α	4.80	5.00	0.189	0.196	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27BSC		0.05	BSC	
K	0.10	0.25	0.004	0.009	
M	0°	7°	0°	7°	
Р	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	



Marking Diagram



Y = Year Code

M = Month Code

(A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)

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L = Lot Code

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TSM440430V N-Channel MOSFET

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