

# **Preliminary**

# **TSM4392**

## 30V N-Channel MOSFET



SOP-8



#### Pin Definition:

- 1. Source
- 2. Source
- 3. Source
- 4. Gate
- 5, 6, 7, 8. Drain

#### PRODUCT SUMMARY

V <sub>DS</sub> (V)	$R_{DS(on)}(m\Omega)$	I <sub>D</sub> (A)		
30	11.5 @ V <sub>GS</sub> = 10V	12.5		
	16.5 @ V <sub>GS</sub> = 4.5V	10		

#### **Features**

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

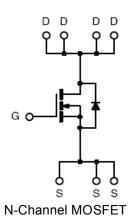
#### **Application**

- High-Side DC/DC Conversion
- Notebook
- Sever

## **Ordering Information**

Part No.	Package	Packing
TSM4392CS RL	SOP-8	2.5Kpcs / 13" Reel

#### **Block Diagram**



**Absolute Maximum Rating** (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	30	V	
Gate-Source Voltage		$V_{GS}$	±20	V	
Continuous Drain Current		I <sub>D</sub>	12.5	Α	
Pulsed Drain Current	sed Drain Current		50	Α	
Continuous Source Current (Diode Co	onduction) <sup>a,b</sup>	I <sub>S</sub>	2.7	Α	
Maximum Power Dissipation	Ta = 25°C	- P <sub>D</sub>	3.0	W	
	Ta = 75°C		1.9		
Operating Junction Temperature		TJ	+150	°C	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	- 55 to +150	°C	

#### **Thermal Performance**

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R\Theta_{JF}$	25	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	50	°C/W

#### Notes:

- a. Pulse width limited by the Maximum junction temperature
- b. Surface Mounted on FR4 Board, t ≤ 10 sec.

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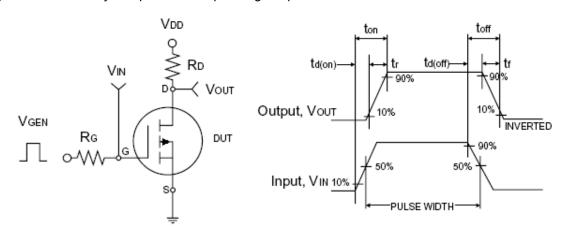


#### **Electrical Specifications** (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Тур	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250uA$	BV <sub>DSS</sub>	30			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	$V_{GS(TH)}$	1	1.8	3	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I <sub>GSS</sub>			±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 24V, V_{GS} = 0V$	I <sub>DSS</sub>			1.0	μA
On-State Drain Current <sup>a</sup>	V <sub>DS</sub> ≥ 5V, V <sub>GS</sub> = 10V	I <sub>D(ON)</sub>	30			Α
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 12.5A$	D		9	11.5	
Diditi-Source Oil-State Resistance	n-Source On-State Resistance $V_{GS} = 4.5V$ , $I_D = 10A$		13	16.5	mΩ	
Forward Transconductance <sup>a</sup>	$V_{DS} = 15V, I_{D} = 12.5A$	g <sub>fs</sub>		40		S
Diode Forward Voltage	$I_S = 2.7A$ , $V_{GS} = 0V$	$V_{SD}$		0.85	1.3	V
Dynamic <sup>b</sup>						
Total Gate Charge	V <sub>DS</sub> = 15V, I <sub>D</sub> = 12.5A,	$Q_g$		26		
Gate-Source Charge		$Q_{gs}$		6		nC
Gate-Drain Charge	V <sub>GS</sub> - 10V	$Q_{gd}$		5		
Input Capacitance	\\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	C <sub>iss</sub>		2134		
Output Capacitance	$V_{DS} = 15V, V_{GS} = 0V,$ f = 1.0MHz	Coss		343		pF
Reverse Transfer Capacitance	1 - 1.0IVINZ	C <sub>rss</sub>		134		
Switching <sup>c</sup>						
Turn-On Delay Time		$t_{d(on)}$		17		
Turn-On Rise Time	$V_{DD} = 15V, R_L = 15\Omega,$	t <sub>r</sub>		3.5		20
Turn-Off Delay Time	$I_D = 1A, V_{GEN} = 10V,$ $R_G = 6\Omega$	t <sub>d(off)</sub>		40		nS
Turn-Off Fall Time	11G - 022	t <sub>f</sub>		6		

#### Notes:

- a. pulse test: PW ≤300µS, duty cycle ≤2%
- b. For DESIGN AID ONLY, not subject to production testing.
- b. Switching time is essentially independent of operating temperature.



**Switching Test Circuit** 

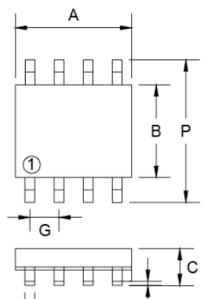
Switchin Waveforms



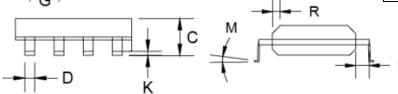




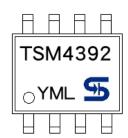
# **SOP-8 Mechanical Drawing**



SOP-8 DIMENSION					
DIM	MILLIMETERS		INCHES		
	MIN	MAX	MIN	MAX.	
Α	4.80	5.00	0.189	0.196	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	1.27BSC		BSC	
K	0.10	0.25	0.004	0.009	
М	0°	7°	0°	7°	
Р	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	



# **Marking Diagram**



Y = Year Code

**M** = Month Code

(A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug,

I=Sep, J=Oct, K=Nov, L=Dec)

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L = Lot Code



## **Preliminary**

# TSM4392 30V N-Channel MOSFET

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