Unit: mm

**TOSHIBA** 

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOS IV)

# **TPC8042**

Lithium-Ion Battery Applications Portable Equipment Applications Notebook PC Applications

- Small footprint due to a small and thin package
- Low drain-source ON-resistance:  $R_{DS}$  (ON) = 2.7 m $\Omega$  (typ.)
- High forward transfer admittance:  $|Y_{fs}| = 42 \text{ S} (typ.)$
- Low leakage current:  $IDSS = 10 \ \mu A \ (max) \ (VDS = 30 \ V)$
- Enhancement mode:  $V_{th} = 1.3$  to 2.5 V ( $V_{DS} = 10$  V,  $I_D = 1$  mA)

#### Absolute Maximum Ratings (Ta = 25°C)

Characte	ristics	Symbol	Rating	Unit
Drain-source voltage		V <sub>DSS</sub>	30	V
Drain-gate voltage (R	t <sub>GS</sub> = 20 kΩ)	V <sub>DGR</sub>	30	V
Gate-source voltage		V <sub>GSS</sub>	±20	V
Drain current	DC (Note 1)	I <sub>D</sub>	18	А
Drain current	Pulse (Note 1)	I <sub>DP</sub>	72	A
Drain power dissipati	on (t = 10 s) (Note 2a)	PD	1.9	W
Drain power dissipati	on (t = 10 s) (Note 2b)	PD	1.0	W
Single pulse avalancl	ne energy (Note 3)	E <sub>AS</sub>	84	mJ
Avalanche current		I <sub>AR</sub>	18	А
Repetitive avalanche (	energy Note 2a) (Note 4)	E <sub>AR</sub>	0.044	mJ
Channel temperature		T <sub>ch</sub>	150	°C
Storage temperature	range	T <sub>stg</sub>	-55 to 150	°C

Note: For Notes 1 to 4, refer to the next page.

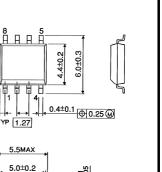
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in

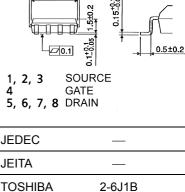
temperature, etc.) may cause this product to decrease in the

reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

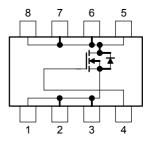




Weight: 0.08 g (typ.)

0.595TYP

#### **Circuit Configuration**

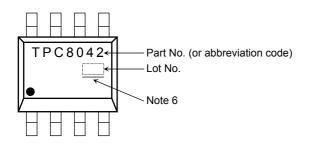


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#### **Thermal Characteristics**

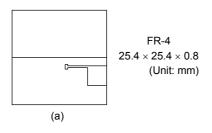
Characteristics	Symbol	Max	Unit
$\label{eq:thermal} \begin{array}{l} \mbox{Thermal resistance, channel to ambient} \\ (t=10 \mbox{ s}) & (\mbox{Note 2a}) \end{array}$	R <sub>th (ch-a)</sub>	65.8	°C/W
Thermal resistance, channel to ambient $(t = 10 \text{ s})$ (Note 2b)	R <sub>th (ch-a)</sub>	125	°C/W

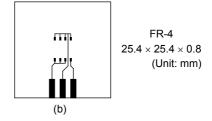
#### Marking (Note 5)



Note 1: Ensure that the channel temperature does not exceed 150°C.

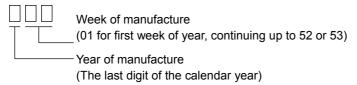
Note 2: (a) Device mounted on a glass-epoxy board (a)





(b) Device mounted on a glass-epoxy board (b)

- Note 3:  $V_{DD} = 24 V$ ,  $T_{ch} = 25^{\circ}C$  (initial), L = 0.2 mH,  $I_{AR} = 18 A$
- Note 4: Repetitive rating: pulse width limited by maximum channel temperature
- Note 5: on the lower left of the marking indicates Pin 1.
  - \* Weekly code: (Three digits)



Note 6: A line under a Lot No. identifies the indication of product Labels. Not underlined: [[Pb]]/INCLUDES > MCV Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

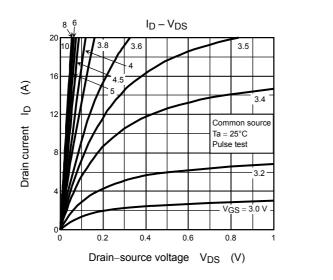
Electrical Characteristics (Ta = 25°C)

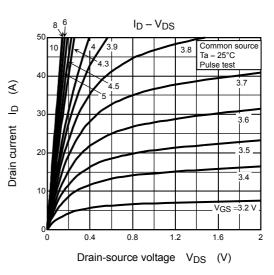
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cu	rrent	I <sub>GSS</sub>	$V_{GS}=\pm 20~V,~V_{DS}=0~V$		—	±100	nA
Drain cut-OFF cu	urrent	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$		_	10	μA
Drain agurag bra	e leakage current in cut-OFF current in-source breakdown voltage e threshold voltage in-source ON-resistance ward transfer admittance it capacitance erse transfer capacitance put capacitance put capacitance erse transfer capacitance put capacitance fail time Turn-on time Fail time Turn-off time al gate charge	V (BR) DSS	$I_{D} = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	30	_		V
Drain-source bre	akuown voltage	V (BR) DSX	$I_D = 10 \text{ mA}, V_{GS} = -20 \text{ V}$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	v		
Gate threshold v	oltage	V <sub>th</sub>	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1 \text{ mA}$	1.3	_	2.5	V
Drain course ON			$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 9 \text{ A}$	_	4.2	6.5	
Drain-source ON	-resistance	R <sub>DS (ON)</sub>	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 9 \text{ A}$	_	2.7	3.4	mΩ
Forward transfer	ward transfer admittance		$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 9 \text{ A}$	21	42	—	S
Input capacitance		C <sub>iss</sub>	$V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$	_	2900		pF
Reverse transfer capacitance		C <sub>rss</sub>		_	460		
Output capacitance		C <sub>oss</sub>			800		
Reverse transfer capacitance $C_{rss}$ $V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$ Output capacitance $C_{oss}$ Rise time $t_r$ $V_{GS} \frac{10 \text{ V}}{0 \text{ V}}$		18	_				
Curitoping time	Turn-on time	t <sub>on</sub>			$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		
Rise time $t_r$ $V_{GS}$ $V_{OV}$ $ 18$ Switching time $t_{on}$ $Turn-on timet_{on} 32Fall timet_fV_{DD} \approx 15 V 25$	25	_	ns				
	Turn-off time	t <sub>off</sub>			81	_	
Total gate charge (gate-source plus	otal gate charge gate-source plus gate-drain)		$V_{DD} \approx 24$ V, $V_{GS} = 10$ V, $I_D = 18$ A		56	_	nC
Gate-source charge 1		Q <sub>gs1</sub>		_	9	—	
Gate-drain ("mille	er") charge	Q <sub>gd</sub>			17	—	

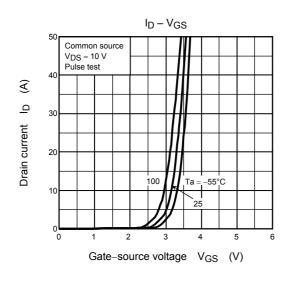
#### Source-Drain Ratings and Characteristics (Ta = 25°C)

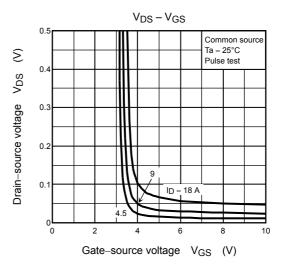
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit	
Drain reverse current	Pulse	(Note 1)	I <sub>DRP</sub>	—	_	_	72	А
Forward voltage (diode)			V <sub>DSF</sub>	$I_{DR} = 18 \text{ A}, V_{GS} = 0 \text{ V}$			-1.2	V

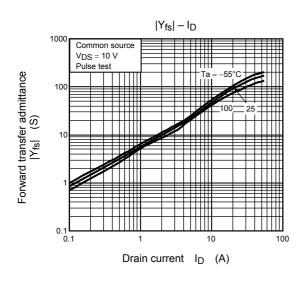
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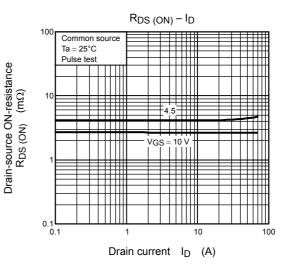


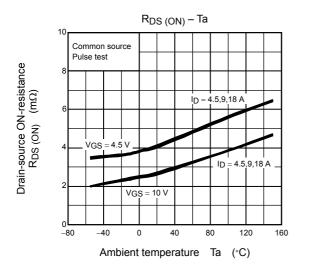


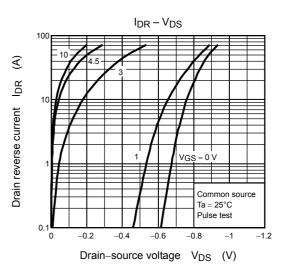


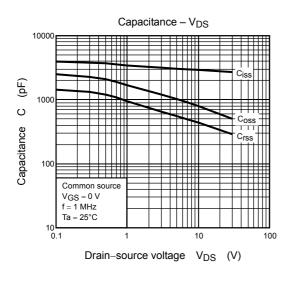


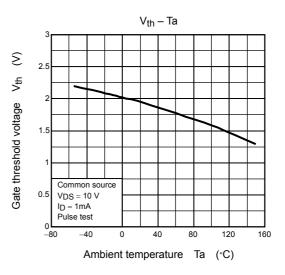


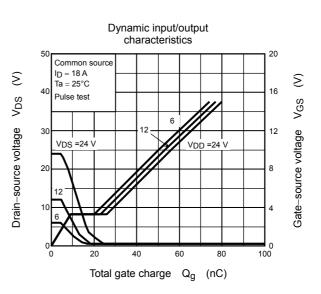


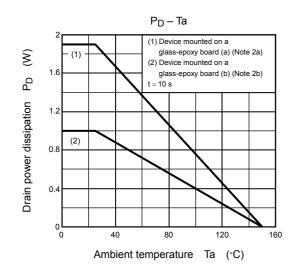


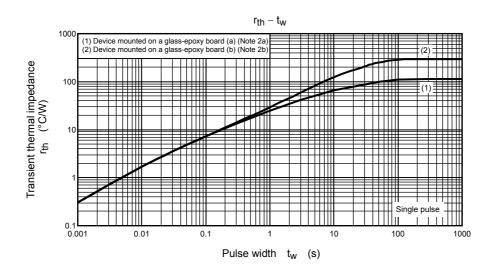


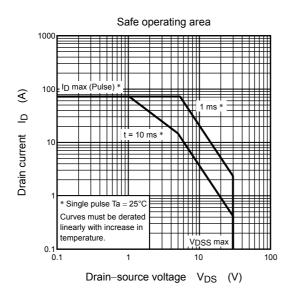












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