

# TK40P03M1

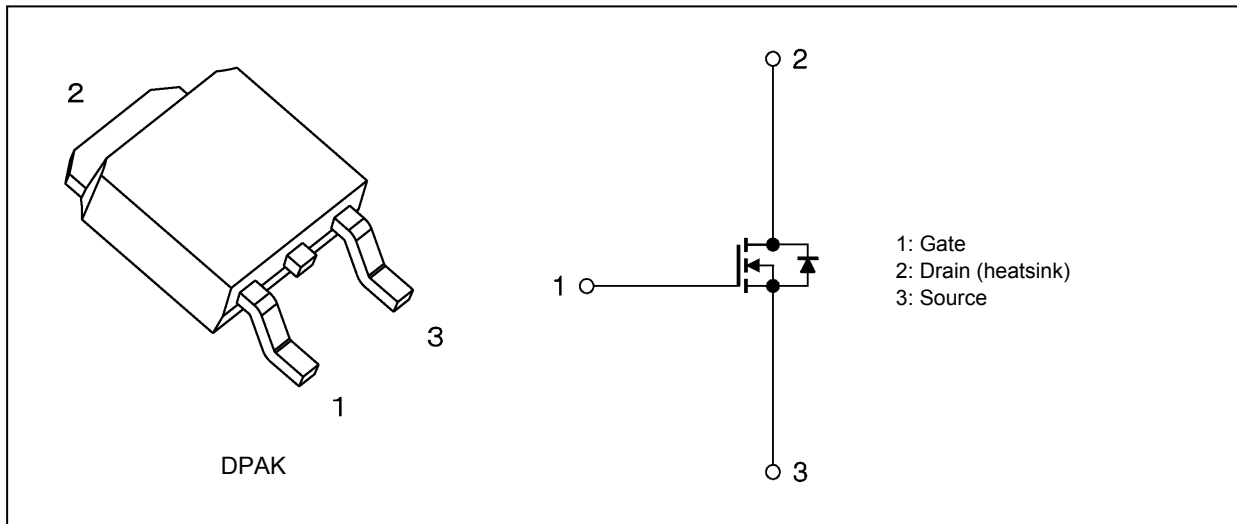
## 1. Applications

- DC-DC Converters
- Desktop PCs

## 2. Features

- (1) High-speed switching
- (2) Low gate charge:  $Q_{SW} = 5.7 \text{ nC (typ.)}$
- (3) Low drain-source on-resistance:  $R_{DS(ON)} = 8.3 \text{ m}\Omega \text{ (typ.) (} V_{GS} = 10 \text{ V)}$
- (4) Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A (max) (} V_{DS} = 30 \text{ V)}$
- (5) Enhancement mode:  $V_{th} = 1.3 \text{ to } 2.3 \text{ V (} V_{DS} = 10 \text{ V, } I_D = 0.1 \text{ mA)}$

## 3. Packaging and Internal Circuit



## 4. Absolute Maximum Ratings (Note) ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	30	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	
Drain current (DC)	$I_D$	40	A
Drain current (pulsed)	$I_{DP}$	120	
Power dissipation ( $T_c = 25^\circ\text{C}$ )	$P_D$	33	W
Single-pulse avalanche energy	$E_{AS}$	42	mJ
Avalanche current	$I_{AR}$	40	A
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	3.78	°C/W
Channel-to-ambient thermal resistance	$R_{th(ch-a)}$	125	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2:  $V_{DD} = 24\text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$  (initial),  $L = 20\ \mu\text{H}$ ,  $R_G = 25\ \Omega$ ,  $I_{AR} = 40\text{ A}$

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

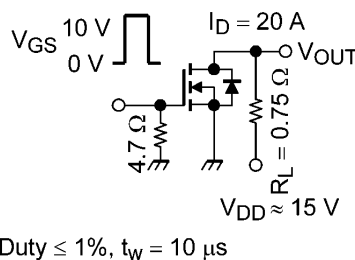
**6. Electrical Characteristics**

**6.1. Static Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 0.1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	30	—	—	V
	$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	15	—	—	
Gate threshold voltage	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 0.1\text{ mA}$	1.3	—	2.3	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	—	11.1	14.4	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	—	8.3	10.8	

**6.2. Dynamic Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	1150	—	$\text{pF}$
Reverse transfer capacitance	$C_{riss}$		—	85	—	
Output capacitance	$C_{oss}$		—	260	—	
Gate resistance	$r_g$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 5\text{ MHz}$	—	2.9	4.4	$\Omega$
Switching time (rise time)	$t_r$	See Figure 6.2.1.	—	15	—	ns
Switching time (turn-on time)	$t_{on}$		—	21	—	
Switching time (fall time)	$t_f$		—	14	—	
Switching time (turn-off time)	$t_{off}$		—	54	—	



**Fig. 6.2.1 Switching Time Test Circuit**

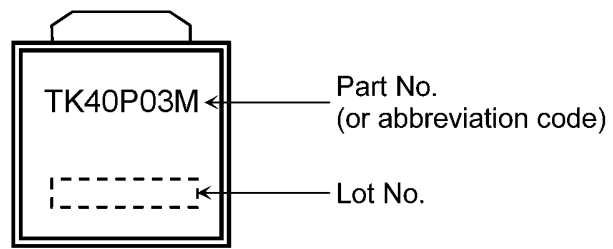
**6.3. Gate Charge Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} \approx 24\text{ V}, V_{GS} = 10\text{ V}, I_D = 40\text{ A}$	—	17.5	—	nC
		$V_{DD} \approx 24\text{ V}, V_{GS} = 5\text{ V}, I_D = 40\text{ A}$	—	9.4	—	
Gate-source charge 1	$Q_{gs1}$	$V_{DD} = 24\text{ V}, V_{GS} = 10\text{ V}, I_D = 40\text{ A}$	—	4.1	—	
Gate-drain charge	$Q_{gd}$		—	3.5	—	
Gate switch charge	$Q_{sw}$		—	5.7	—	

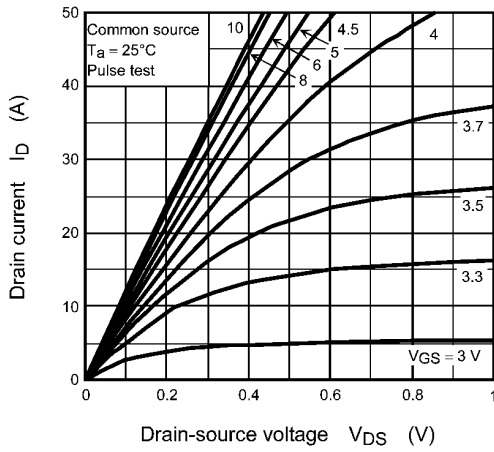
**6.4. Source-Drain Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed)	(Note 3) $I_{DRP}$	—	—	—	120	A
Diode forward voltage	$V_{DSF}$	$I_{DR} = 40\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.2	V

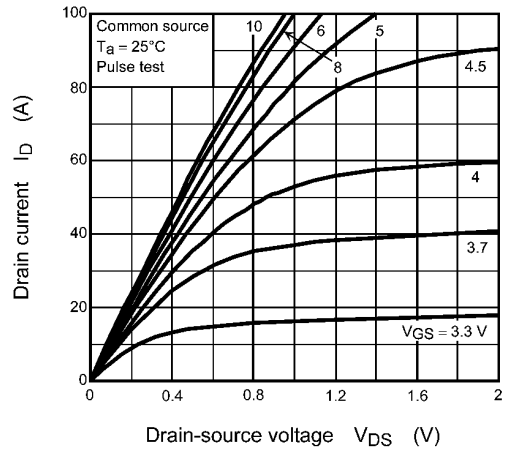
Note 3: Ensure that the channel temperature does not exceed  $150^\circ\text{C}$ .

**7. Marking****Fig. 7.1 Marking**

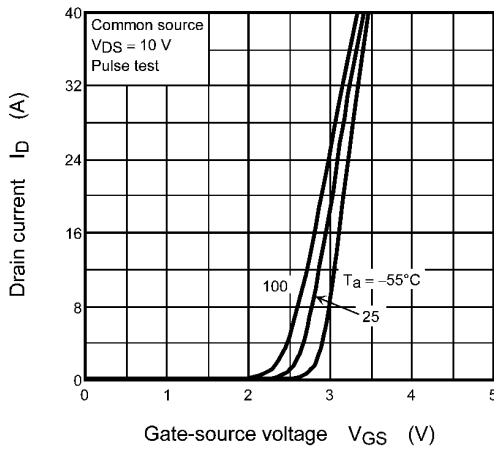
**8. Characteristics Curves (Note)**



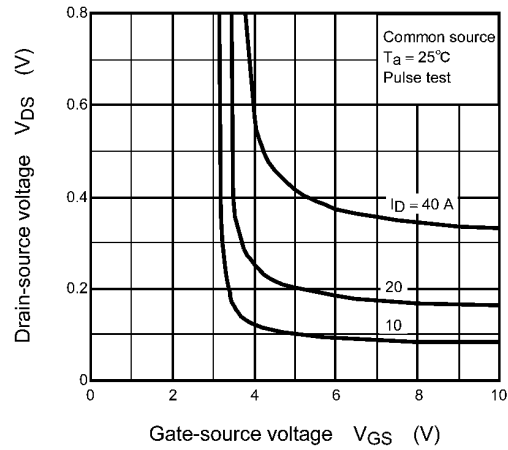
**Fig. 8.1  $I_D - V_{DS}$**



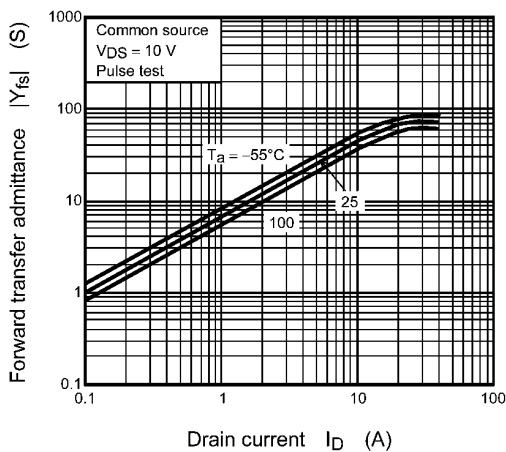
**Fig. 8.2  $I_D - V_{DS}$**



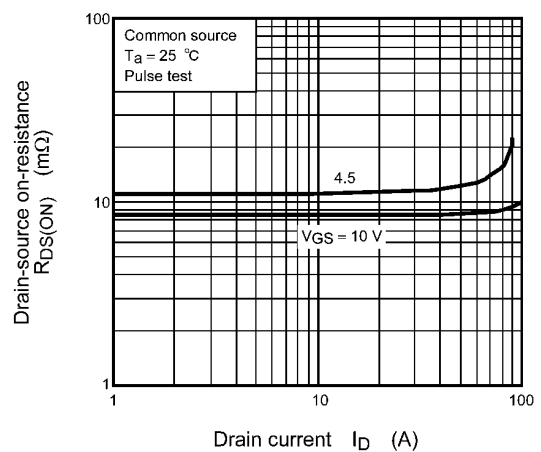
**Fig. 8.3  $I_D - V_{GS}$**



**Fig. 8.4  $V_{DS} - V_{GS}$**



**Fig. 8.5  $|Y_{fs}| - I_D$**



**Fig. 8.6  $R_{DS(ON)} - I_D$**

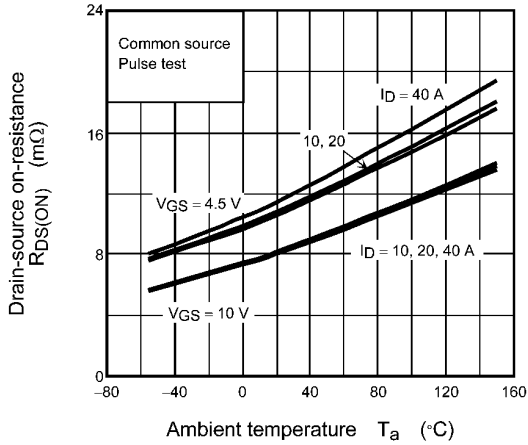


Fig. 8.7  $R_{DS(ON)} - T_a$

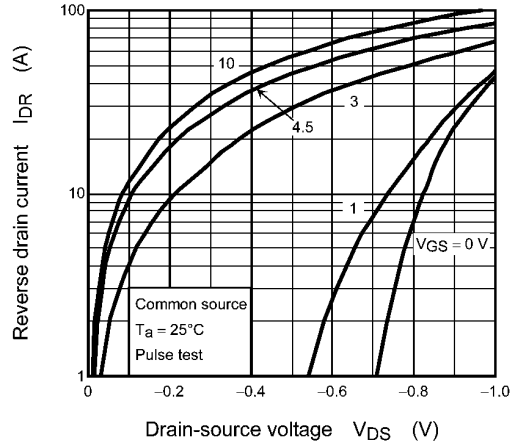


Fig. 8.8  $I_{DR} - V_{DS}$

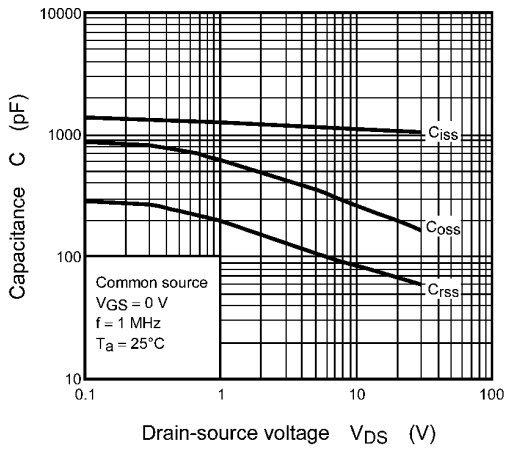


Fig. 8.9 Capacitance -  $V_{DS}$

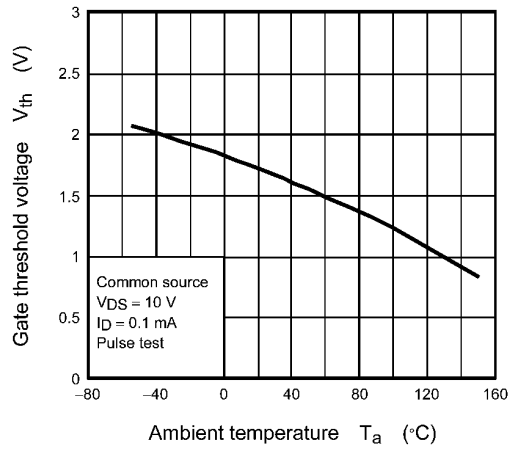


Fig. 8.10  $V_{th} - T_a$

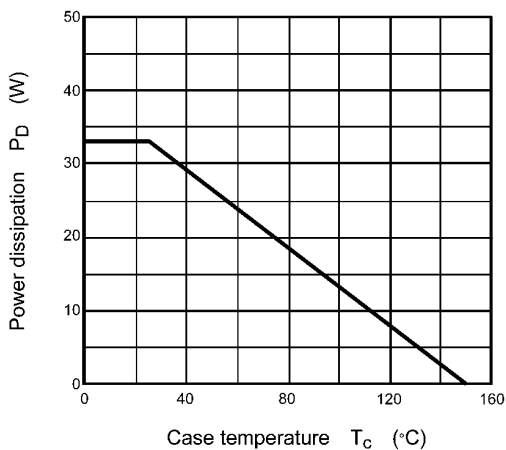


Fig. 8.11  $P_D - T_C$   
(Guaranteed Maximum)

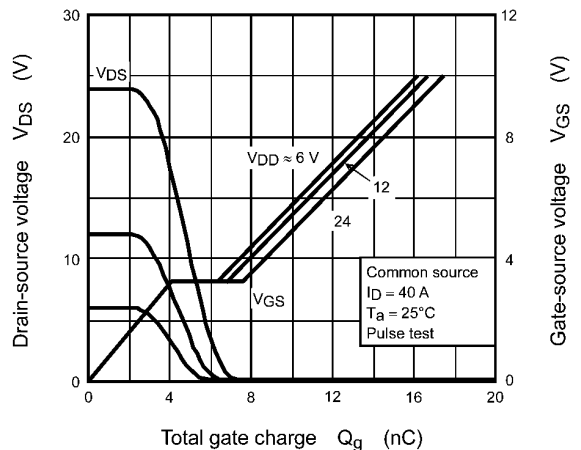
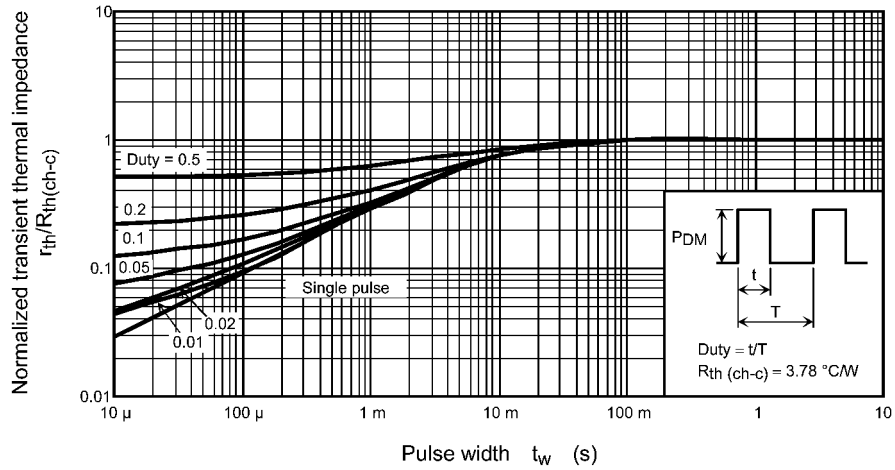
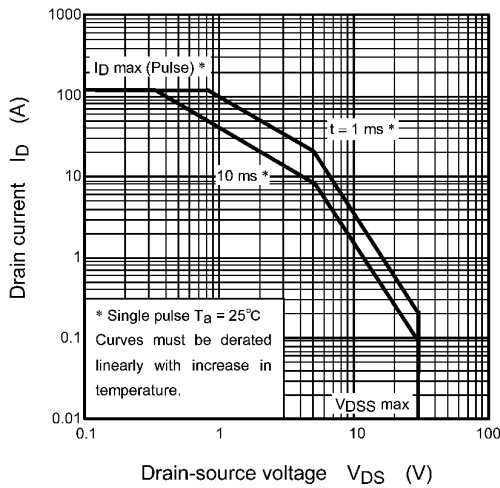


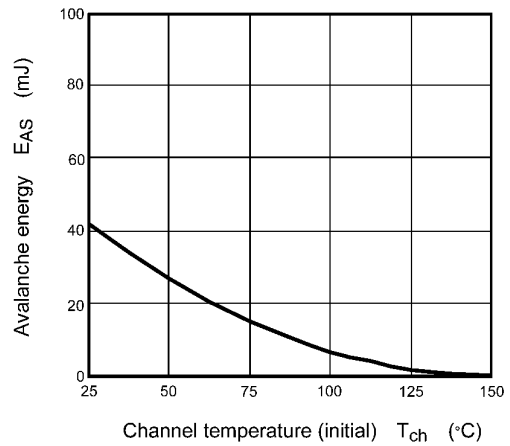
Fig. 8.12 Dynamic Input/Output Characteristics



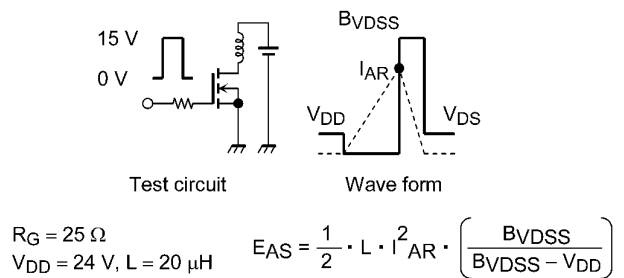
**Fig. 8.13**  $r_{th}/R_{th(ch-c)} - t_w$   
(Guaranteed Maximum)



**Fig. 8.14** Safe Operating Area  
(Guaranteed Maximum)



**Fig. 8.15**  $E_{AS} - T_{ch}$   
(Guaranteed Maximum)

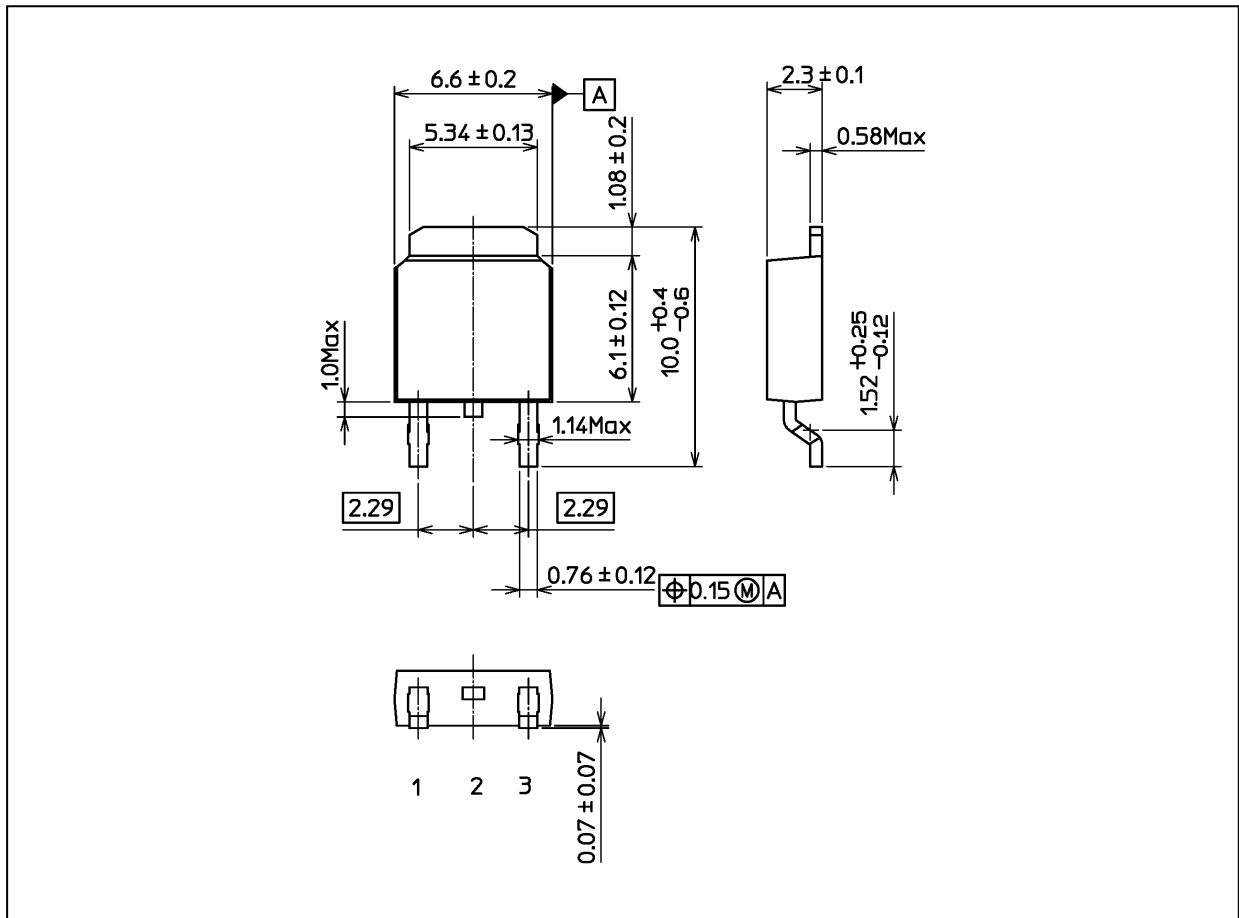


**Fig. 8.16** Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.36 g (typ.)

Package Name(s)
TOSHIBA: 2-7K1S
Nickname: DPAK



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