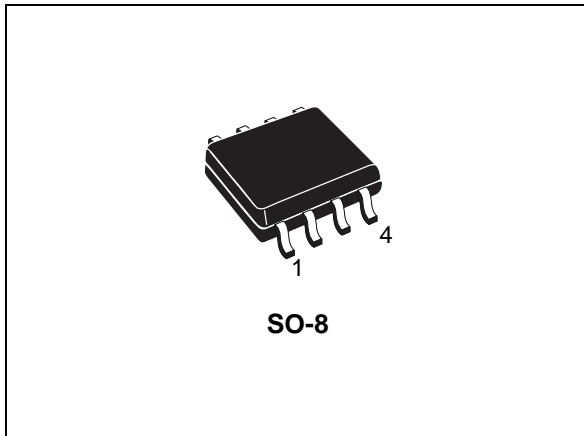


## P-channel 40 V, 0.013 $\Omega$ typ., 10 A, STripFET™ VI DeepGATE™ Power MOSFET in a SO-8 package

Datasheet - preliminary data



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STS10P4LLF6	40 V	0.017 $\Omega$	10A

- R<sub>DS(on)</sub>\* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the 6<sup>th</sup> generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R<sub>DS(on)</sub> in all packages.

Figure 1. Internal schematic diagram

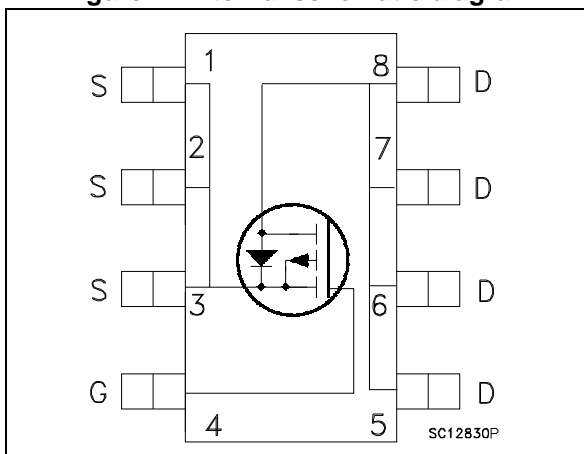


Table 1. Device summary

Order code	Marking	Packages	Packaging
STS10P4LLF6	10K4L	SO-8	Tape and reel

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed.

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate- source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_{amb} = 25^\circ\text{C}$	10	A
$I_D^{(1)}$	Drain current (continuous) at $T_{amb} = 100^\circ\text{C}$	5.6	A
$I_{DM}^{(2)}$	Drain current (pulsed)	40	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{amb} = 25^\circ\text{C}$	2.7	W
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature	150	$^\circ\text{C}$

1. This value is rated according to  $R_{thj-amb}$
2. Pulse width limited by safe operating area

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb	47	$^\circ\text{C/W}$

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz. Cu.,  $t \leq 10$  sec

*Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed.*

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A$	40			V V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 40\ V$			1	$\mu A$
		$V_{DS} = 30V, T_C = 125\text{°C}$			10	
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\ V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10V, I_D = 3\ A$		0.013	0.017	$\Omega$
		$V_{GS} = 4.5V, I_D = 3\ A$		0.018	0.0235	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 32\ V, f = 1\ MHz, V_{GS} = 0$	-	2900	-	pF
$C_{oss}$	Output capacitance		-	400	-	pF
$C_{rss}$	Reverse transfer capacitance		-	150	-	pF
$Q_g$	Total gate charge	$V_{DD} = 32\ V, I_D = 10\ A, V_{GS} = 4.5\ V$	-	30	-	nC
$Q_{gs}$	Gate-source charge		-	TBD	-	nC
$Q_{gd}$	Gate-drain charge		-	TBD	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 32\ V, I_D = 5\ A, R_G = 4.7\ \Omega, V_{GS} = 10\ V$ <i>Figure 2</i>	-	TBD	-	ns
$t_r$	Rise time		-	TBD	-	
$t_{d(off)}$	Turn-off delay time		-	TBD	-	
$t_f$	Fall time		-	TBD	-	

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		40	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3A, V_{GS} = 0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5 A, di/dt = 100 A/\mu s$ $V_{DD} = 10 V, T_j = 150 ^\circ C$	-	TBD		ns
$Q_{rr}$	Reverse recovery charge		-	TBD		nC
$I_{RRM}$	Reverse recovery current		-	TBD		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5%

*Note:* For the P-channel MOSFET actual polarity of voltages and current has to be reversed

### 3 Test circuits

Figure 2. Switching times test circuit for resistive load

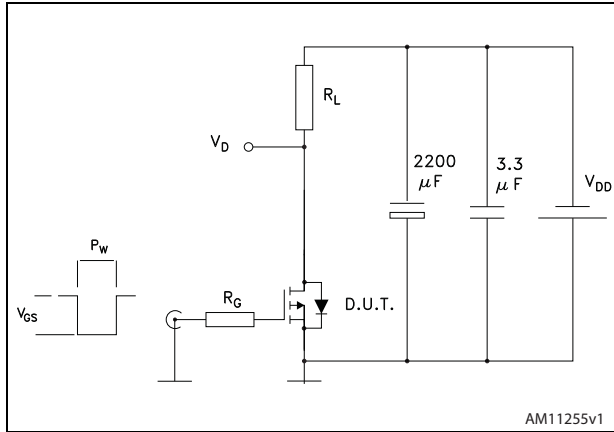


Figure 3. Gate charge test circuit

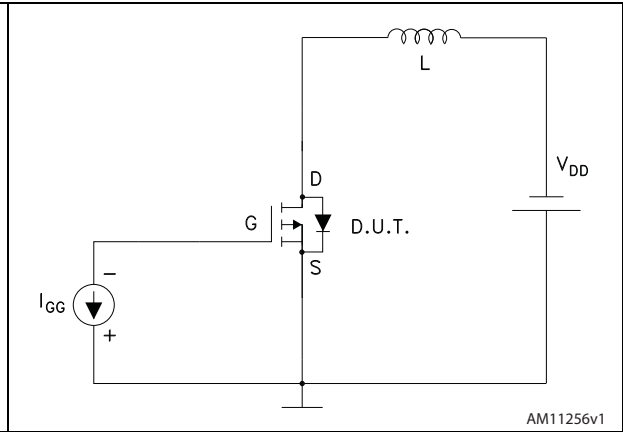
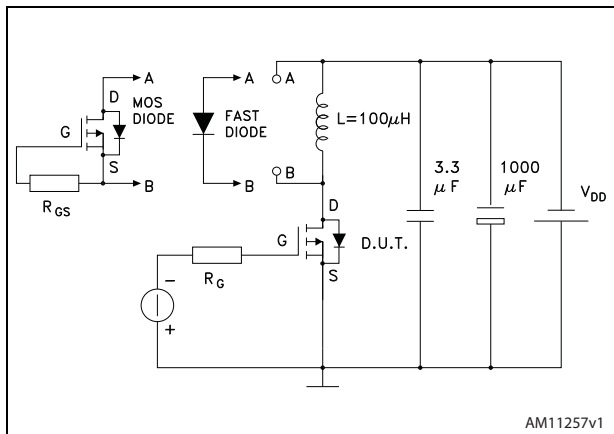


Figure 4. Test circuit for diode recovery behavior



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 5. SO-8 drawing

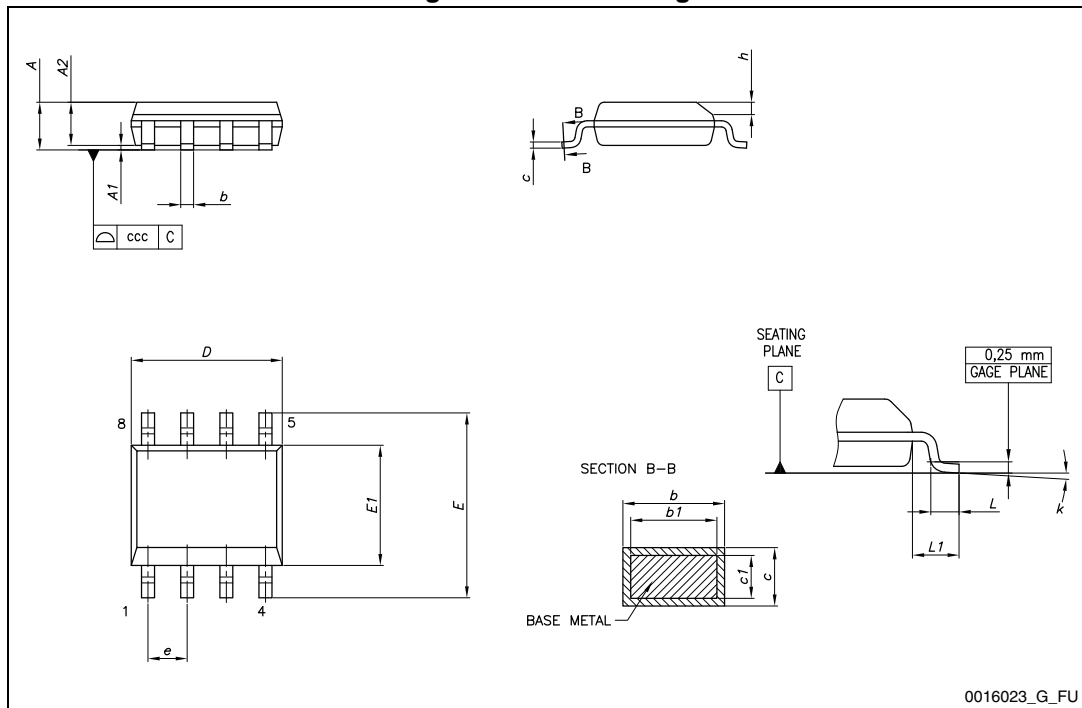
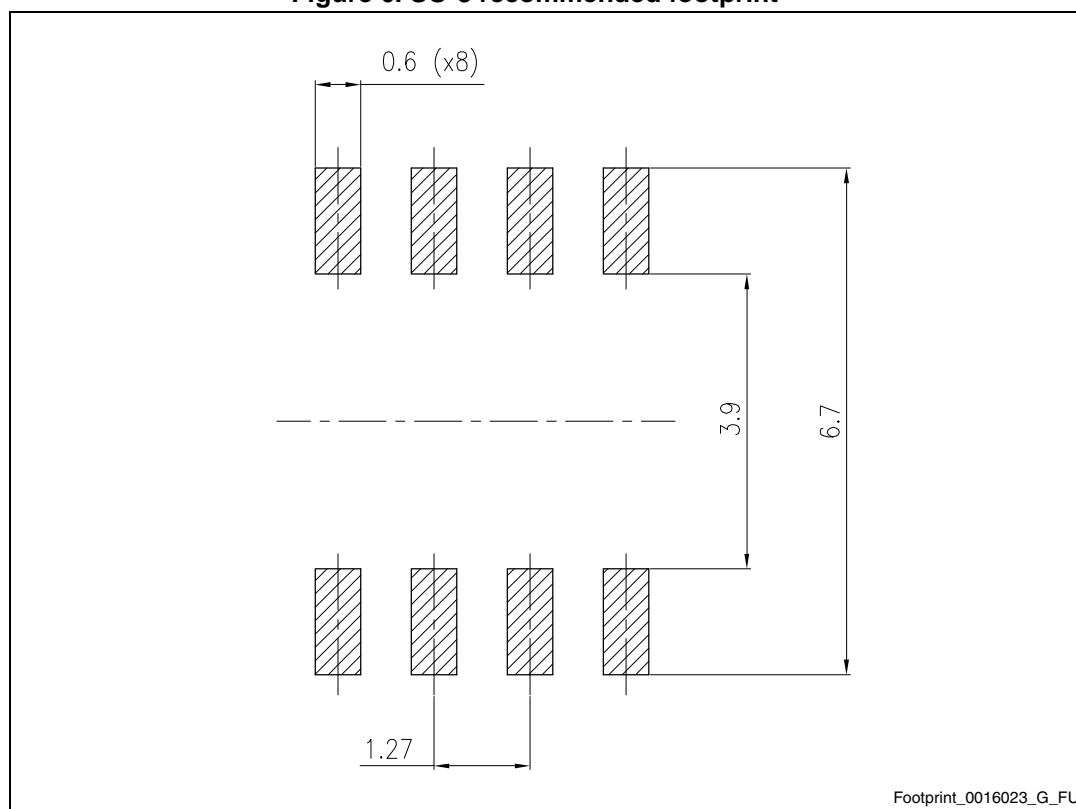


Table 8. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 6. SO-8 recommended footprint<sup>(a)</sup>



a. All dimensions are in millimeters.



## 5 Packaging mechanical data

Figure 7. SO-8 tape and reel dimensions

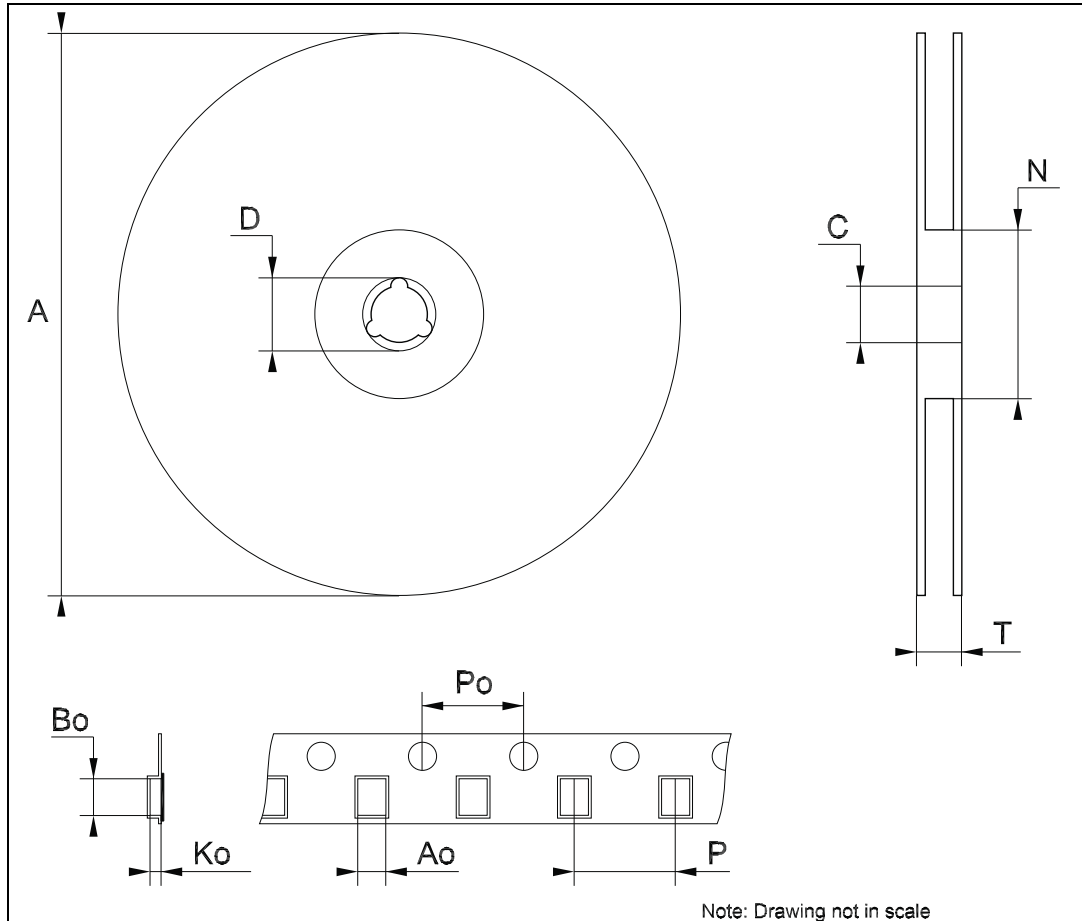


Table 9. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

## 6 Revision history

Table 10. Revision history

Date	Revision	Changes
20-Jan-2014	1	First revision.

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