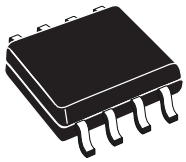
# STS5DP3LLH6

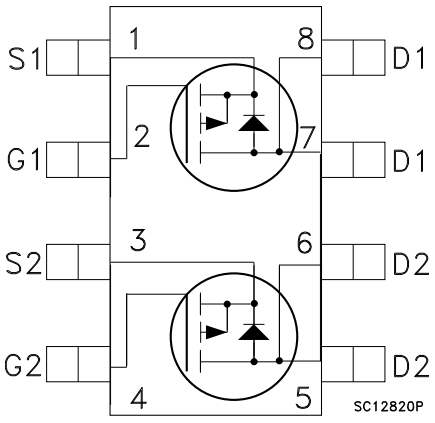
## DUAL P-Channel 30 V, 0.04 Ω typ., 5 A STripFET™ VI DeepGATE™ Power MOSFET in a SO-8 package

**Datasheet - preliminary data**



**SO-8**

**Figure 1. Internal schematic diagram**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STS5DP3LLH6 | 30 V | 0.06 Ω at 10 V | 5 A |

- $R_{DS(on)}$* Qg industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power losses

## Applications

- Switching applications

## Description

This device is a DUAL P-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STS5DP3LLH6 | 5K3L | SO-8 | Tape and reel |

*Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed.*

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 30 | V |
| $V_{GS}$ | Gate-source voltage | ± 20 | V |
| $I_D$ | Drain current (continuous) at $T_{pcb}$ = 25 °C | 5 | A |
| $I_D$ | Drain current (continuous) at $T_{pcb}$ = 100 °C | 3.2 | A |
| $I_{DM}$ (1) (2) | Drain current (pulsed) | 20 | A |
| $P_{TOT}$ | Total dissipation at $T_{pcb}$ = 25 °C | 2.7 | W |
| $T_J$ | Operating junction temperature | 150 | °C |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |

1. This value is rated according to Rthj-pcb
2. Pulse width limited by safe operating area

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}amb}$ (1) | Thermal resistance junction-amb | 47 | °C/W |

1. When mounted on 1 inch² FR-4 board, 2 oz. Cu., t ≤ 10 sec

*Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.*

# 2 Electrical characteristics

($T_{CASE}$ = 25 °C unless otherwise specified)

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ($V_{GS}$ = 0) | $I_D$ = 250 µA | 30 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 30 V,<br>$V_{DS}$ = 30 V, $T_J$ = 125 °C | | | 1 | µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ±20 V | | | 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | | | | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 2.5 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 2.5 A | | 0.04<br>0.07 | 0.06<br>0.09 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 24 V, f=1 MHz<br>$V_{GS}$ = 0 | - | 690 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 120 | - | |
| $C_{rss}$ | Reverse transfer capacitance | | - | 60 | - | |
| $Q_g$ | Total gate charge | $V_{DD}$ = 24 V, $I_D$ = 5 A<br>$V_{GS}$ = 4.5 V | - | 8 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | TBD | - | |
| $Q_{gd}$ | Gate-drain charge | | - | TBD | - | |

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$= 24 V, $I_D$ = 5 A,<br>$R_G$ = 4.7 Ω, $V_{GS}$ = 10 V | - | TBD | - | ns |
| $t_r$ | Rise time | | - | TBD | - | |
| $t_{d(off)}$ | Turn-off delay time | | - | TBD | - | |
| $t_f$ | Fall time | | - | TBD | - | |

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | - | 5 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | - | 20 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$ = 5 A, $V_{GS}$ = 0 | - | - | TBD | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 5 A, di/dt = 100 A/µs, $V_{DD}$= 16 V, $T_J$ = 150 °C | - | - | TBD | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | - | TBD | nC |
| $I_{RRM}$ | Reverse recovery current | | - | - | TBD | A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

*Note: For the P-channel MOSFET the actual polarity of the voltages and the current must be reversed.*

# 3 Test circuits

**Figure 2. Switching times test circuit for resistive load**

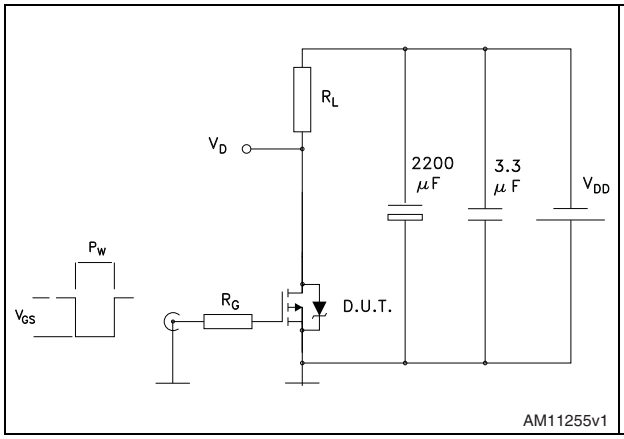



**Figure 3. Gate charge test circuit**

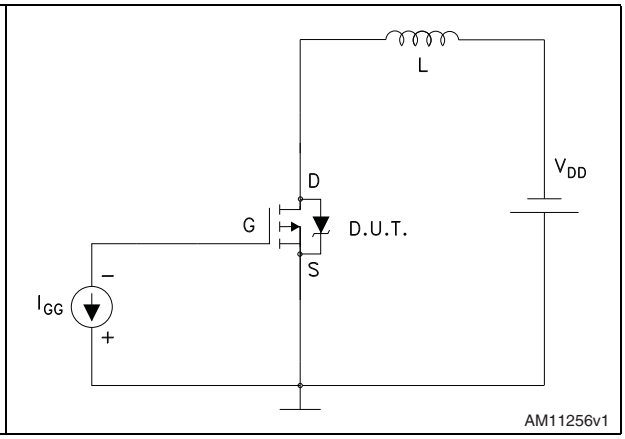
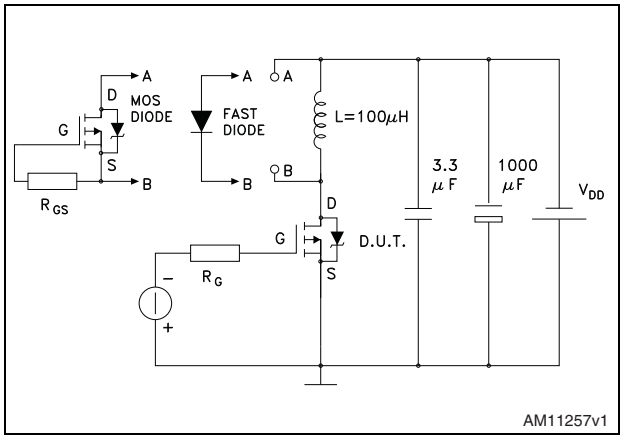



**Figure 4. Test circuit for inductive load switching and diode recovery times**



# 4 Package mechanical data

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**Figure 5. SO-8 drawings**

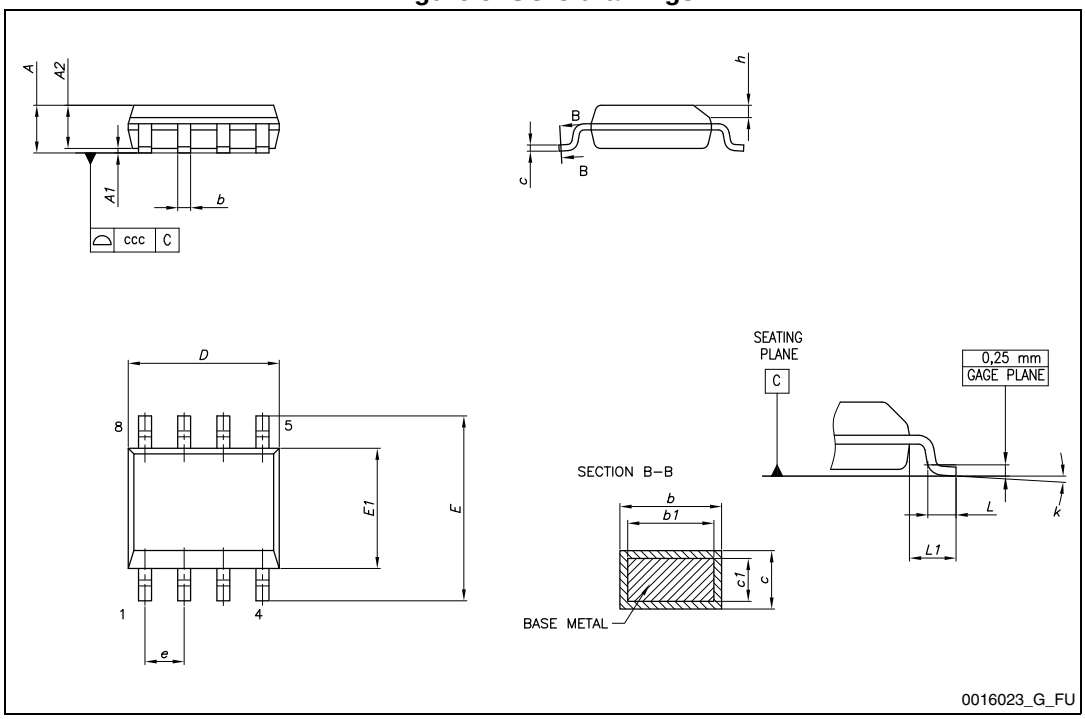
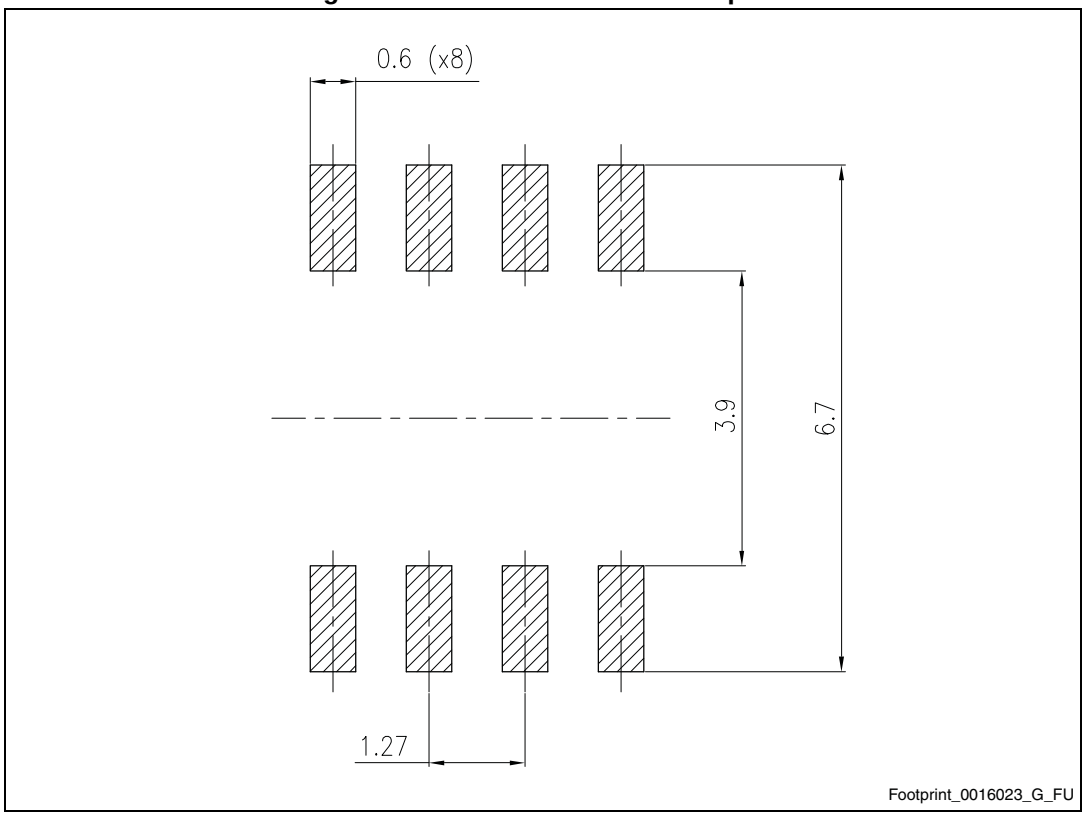


Table 8. SO-8 mechanical data

| Dim | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.75 |
| A1 | 0.10 | | 0.25 |
| A2 | 1.25 | | |
| b | 0.31 | | 0.51 |
| b1 | 0.28 | | 0.48 |
| c | 0.10 | | 0.25 |
| c1 | 0.10 | | 0.23 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| L1 | | 1.04 | |
| L2 | | 0.25 | |
| k | 0° | | 8° |
| ccc | | | 0.10 |

**Figure 6. SO-8 recommended footprint**



# 5 Packaging mechanical data

**Figure 7. SO-8 tape and reel dimensions**

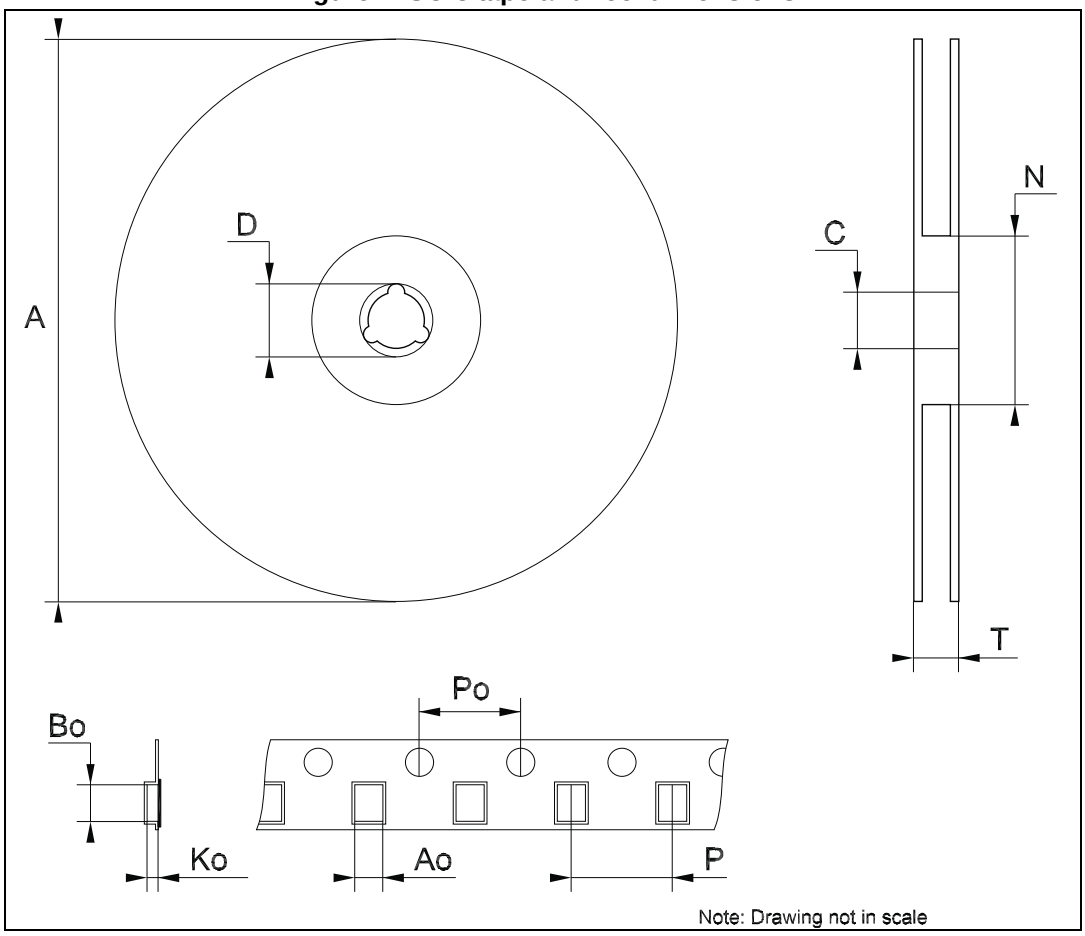


**Table 9. SO-8 tape and reel mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 330 |
| C | 12.8 | | 13.2 |
| D | 20.2 | | |
| N | 60 | | |
| T | | | 22.4 |
| Ao | 8.1 | | 8.5 |
| Bo | 5.5 | | 5.9 |
| Ko | 2.1 | | 2.3 |
| Po | 3.9 | | 4.1 |
| P | 7.9 | | 8.1 |

# 6 Revision history

Table 10. Revision history

| Date | Revision | Changes |
|---|---|---|
| 30-Jan-2014 | 1 | First revision. |

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