### STP160N3LL



# N-channel 30 V, 0.0024 Ω typ., 160 A STripFET<sup>TM</sup> VI DeepGATE<sup>TM</sup> Power MOSFET in a TO-220 package

Datasheet - preliminary data

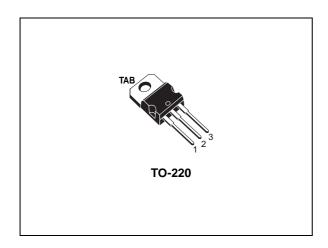
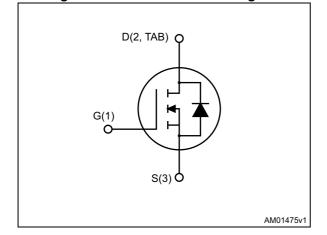


Figure 1. Internal schematic diagram



#### **Features**

Order code	$V_{DS}$	R <sub>DS(on)</sub> max	I <sub>D</sub>
STP160N3LL	30 V	$0.0032~\Omega$	160 A

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- · High avalanche ruggedness
- Low gate drive power losses

### **Applications**

• Switching applications

#### **Description**

This device is an N-channel Power MOSFET developed using the  $6^{th}$  generation of STripFET<sup>TM</sup> DeepGATE<sup>TM</sup> technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R<sub>DS(on)</sub> in all packages.

**Table 1. Device summary** 

Order code	Marking	Package	Packaging
STP160N3LL	160N3LL	TO-220	Tube

Contents STP160N3LL

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STP160N3LL Electrical ratings

# 1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage	30	V
V <sub>GS</sub>	Gate-source voltage	± 20	V
I <sub>D</sub>	Continuous drain current at T <sub>C</sub> = 25 °C (silicon limited)	160	А
I <sub>D</sub>	Continuous drain current at T <sub>C</sub> = 25 °C (package limited)	120	А
I <sub>D</sub>	Continuous drain current at T <sub>C</sub> = 100 °C	112	А
I <sub>DM</sub> <sup>(1)</sup>	Pulsed drain current	480	Α
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	136	W
	Derating factor	0.9	W/°C
E <sub>AS</sub> (2)	Single pulse avalanche energy	150	mJ
T <sub>stg</sub>	Storage temperature	-55 to 175	°C
T <sub>j</sub>	Max. operating junction temperature	175	°C

<sup>1.</sup> Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case max	1.1	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max	62.5	°C/W

<sup>2.</sup> Starting  $T_j = 25$ °C,  $I_{AV} = 40$  A

Electrical characteristics STP160N3LL

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified).

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
I <sub>DSS</sub>	Zero gate voltage drain current	$V_{GS} = 0$ , $V_{DS} = 30 \text{ V}$ $V_{GS} = 0$ , $V_{DS} = 30 \text{ V}$ , $T_C = 125 \text{ °C}$			1 10	μA μA
I <sub>GSS</sub>	Gate body leakage current	$V_{DS} = 0, V_{GS} = \pm 20 \text{ V}$			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1		2.5	V
Read	Static drain-source on-	$V_{GS} = 10 \text{ V}, I_D = 60 \text{ A}$		0.0024	0.0032	Ω
R <sub>DS(on)</sub>	resistance	$V_{GS} = 4.5 \text{ V}, I_D = 60 \text{ A}$		0.0032	0.0042	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Тур.	Max.	Unit
C <sub>iss</sub>	Input capacitance		-	3100	-	pF
C <sub>oss</sub>	Output capacitance	$V_{DS} = 25 \text{ V, f=1 MHz,}$	-	400	-	pF
C <sub>rss</sub>	Reverse transfer capacitance	V <sub>GS</sub> = 0	-	380	-	pF
Qg	Total gate charge	$V_{DD} = 15 \text{ V}, I_{D} = 120 \text{ A}$ $V_{GS} = 4.5 \text{ V}$ Figure 3	-	42	-	nC
$Q_{gs}$	Gate-source charge		-	9	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	18	-	nC
R <sub>G</sub>	Gate input resistance	f = 1 MHz, gate DC Bias = 0, test signal level = 20 mV, $I_D = 0$	-	1	-	Ω

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time		-	19	-	ns
t <sub>r</sub>	Rise time	$V_{DD} = 15 \text{ V}, I_D = 60 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 5 \text{ V}$	-	91	-	ns
t <sub>d(off)</sub>	Turn-off delay time	$R_G = 4.7 \Omega$ , $V_{GS} = 5 V$ Figure 2	-	24.5	-	ns
t <sub>f</sub>	Fall time		-	23.4	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current		-		120	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		-		480	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	I <sub>SD</sub> = 60 A, V <sub>GS</sub> = 0	-		1.1	V
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 120 A,	-	28.6		ns
Q <sub>rr</sub>	Reverse recovery charge	$di/dt = 100 \text{ A/}\mu\text{s},$	-	22.8		nC
I <sub>RRM</sub>	Reverse recovery current	V <sub>DD</sub> = 24 V Figure 4	-	1.6		Α

<sup>1.</sup> Pulse width limited by safe operating area

<sup>2.</sup> Pulsed: pulse duration =  $300 \mu s$ , duty cycle 1.5%

Test circuits STP160N3LL

### 3 Test circuits

Figure 2. Switching times test circuit for resistive load

Figure 3. Gate charge test circuit

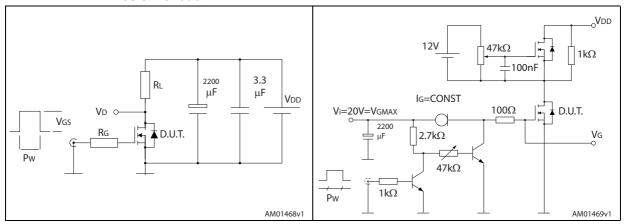


Figure 4. Test circuit for inductive load switching and diode recovery times

Figure 5. Unclamped inductive load test circuit

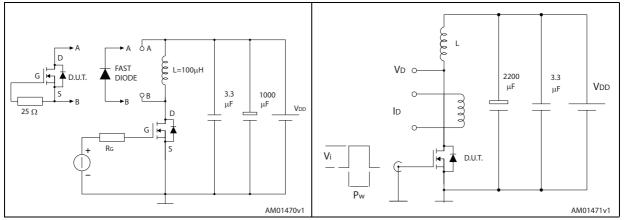
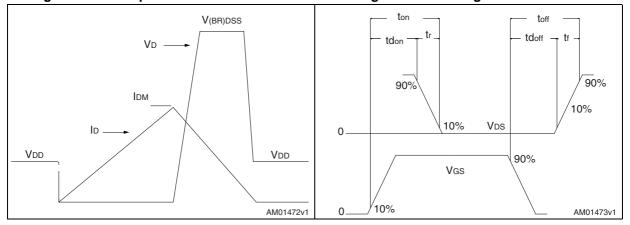


Figure 6. Unclamped inductive waveform

Figure 7. Switching time waveform



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# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: <a href="https://www.st.com">www.st.com</a>. ECOPACK<sup>®</sup> is an ST trademark.



Table 8. TO-220 type A mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
А	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
С	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
е	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

øΡ Ε H1 D <u>D1</u> L20 L30 b1(X3) -- b (X3) \_e1\_\_\_ 0015988\_typeA\_Rev\_T

Figure 8. TO-220 type A drawing

Revision history STP160N3LL

# 5 Revision history

**Table 9. Document revision history** 

Date	Revision	Changes
31-Jul-2013	1	First release.

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