STP32N55M5, STW32N55M5

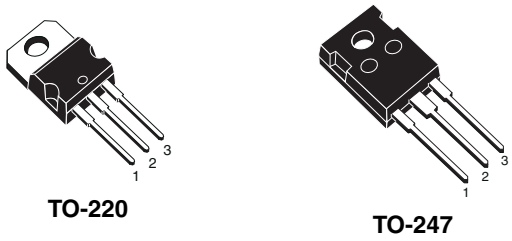
N-channel 550 V, 0.074 Ω, 29 A, MDmesh™ V Power MOSFET in TO-220 and TO-247

Preliminary data

Features

Order codes	V_{DSS} @T_{Jmax}	$R_{DS(on)}$ max	I_D
STP32N55M5 STW32N55M5	550 V	< 0.100 Ω	29 A

- Worldwide best $R_{DS(on)}$*area
- Higher V_{DSS} rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



TO-220 **TO-247**

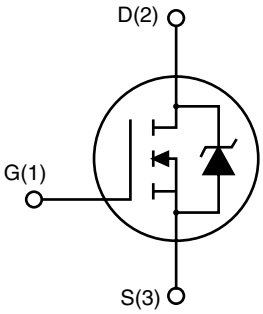
Applications

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram



AM01475v1

Table 1. Device summary

Order codes	Marking	Package	Packaging
STP32N55M5	32N55M5	TO-220	Tube
STW32N55M5		TO-247	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
		TO-220, TO-247	
V_{GS}	Gate-source voltage	25	V
I_D	Drain current (continuous) at T_C = 25 °C	29	A
I_D	Drain current (continuous) at T_C = 100 °C	18.5	A
I_{DM} (1)	Drain current (pulsed)	116	A
P_{TOT}	Total dissipation at T_C = 25 °C	190	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	7	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50 V)	500	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 50	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 29$ A, di/dt ≤ 400 A/µs, $V_{Peak} < V_{(BR)DSS}$, V_{DD} = 400 V.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.66		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	50	°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA	550			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 14.5 A		0.074	0.100	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	TBD TBD TBD	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 440 V	-	TBD	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	TBD	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	TBD	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 440 V, I_D = 14.5 A, V_{GS} = 10 V (see *Figure 3*)	-	TBD TBD TBD	-	nC nC nC

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(off)}$ t_r t_c t_f	Turn-off delay time Rise time Cross time Fall time	V_{DD} = 400 V, I_D = 19 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 2*, *Figure 7*)	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		29 116	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 29 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 29 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 4*)	-	TBD TBD TBD		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 29 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 4*)	-	TBD TBD TBD		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

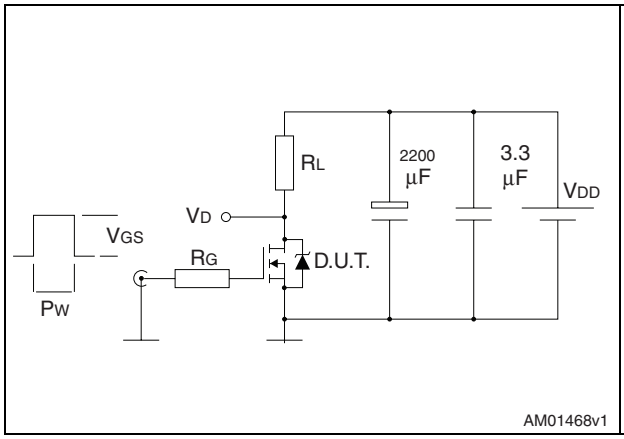


Figure 3. Gate charge test circuit

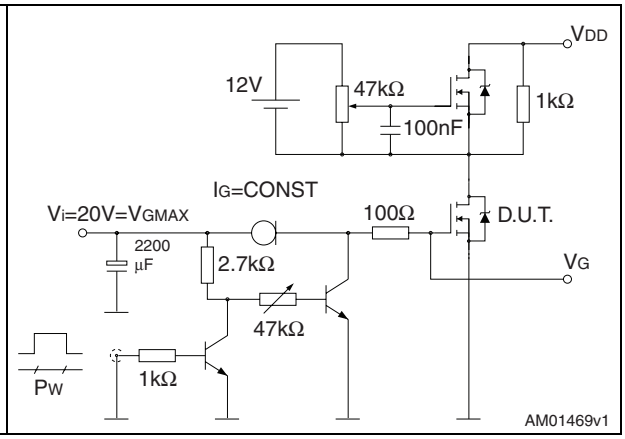


Figure 4. Test circuit for inductive load switching and diode recovery times

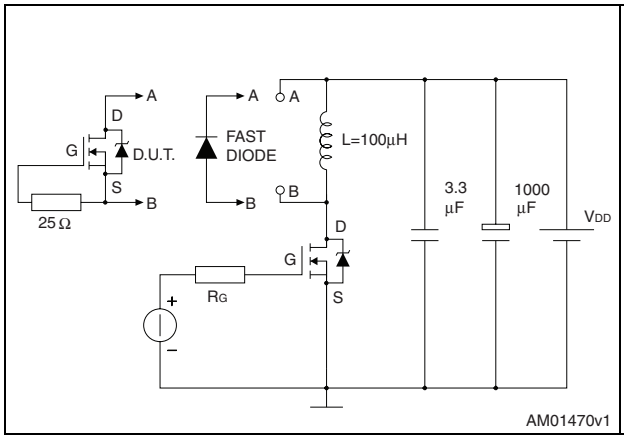


Figure 5. Unclamped inductive load test circuit

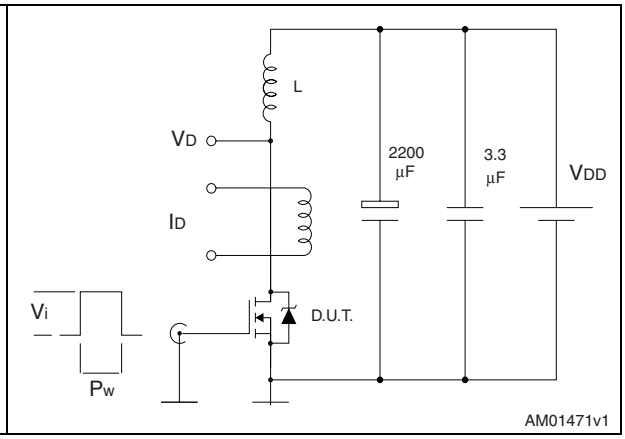


Figure 6. Unclamped inductive waveform

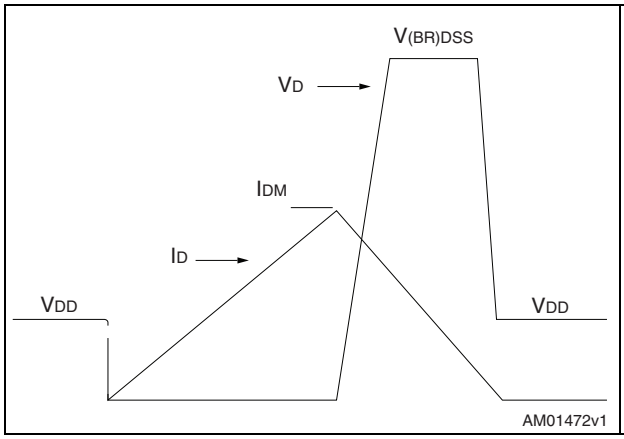
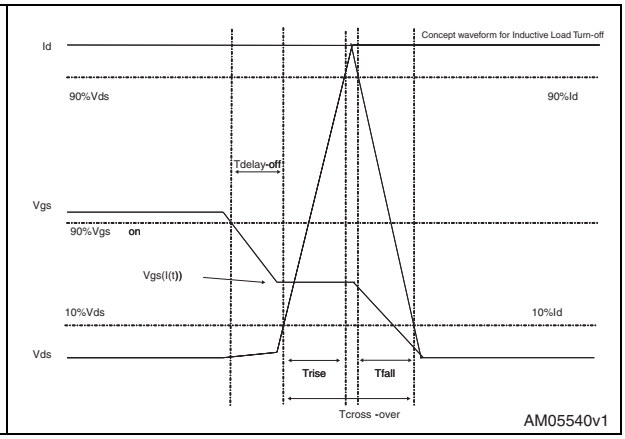


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 8. TO-220 type A drawing

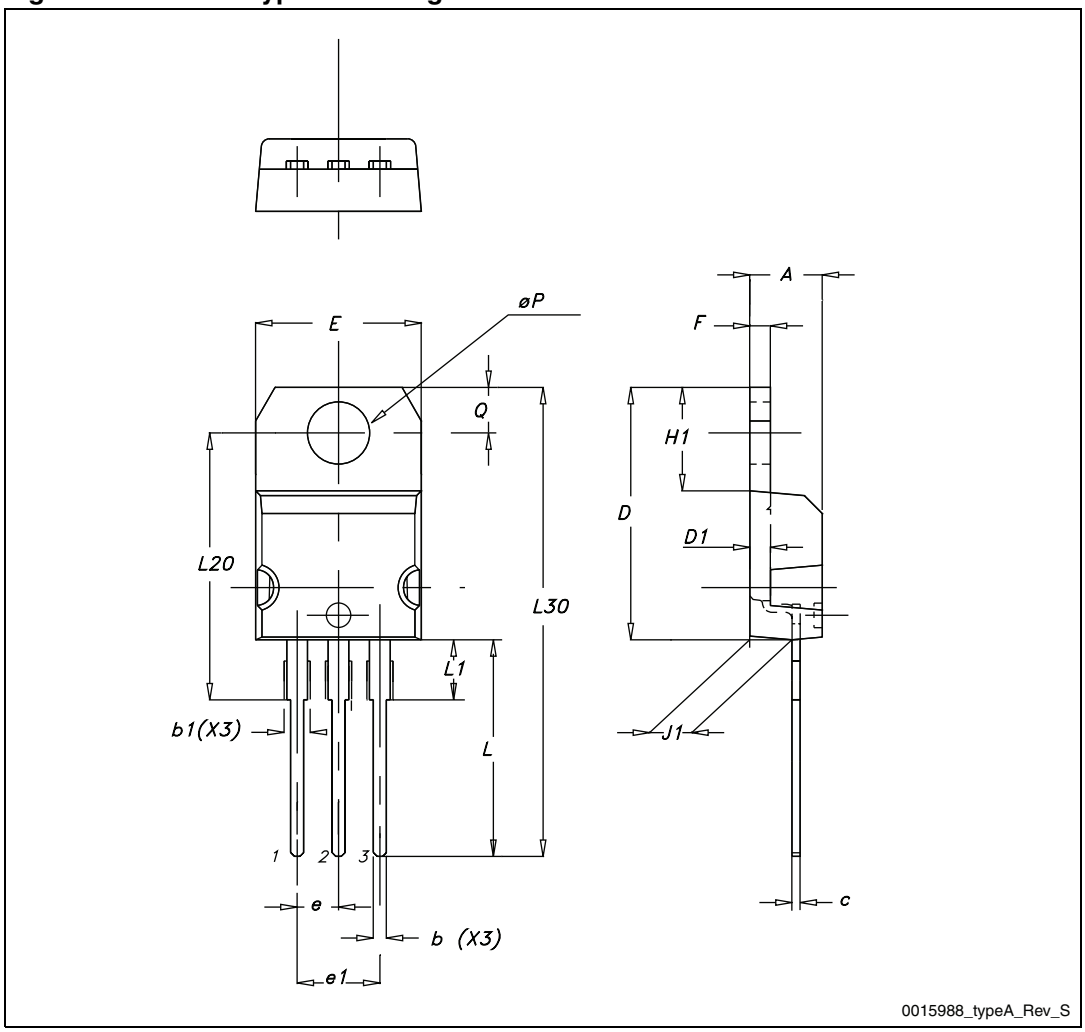
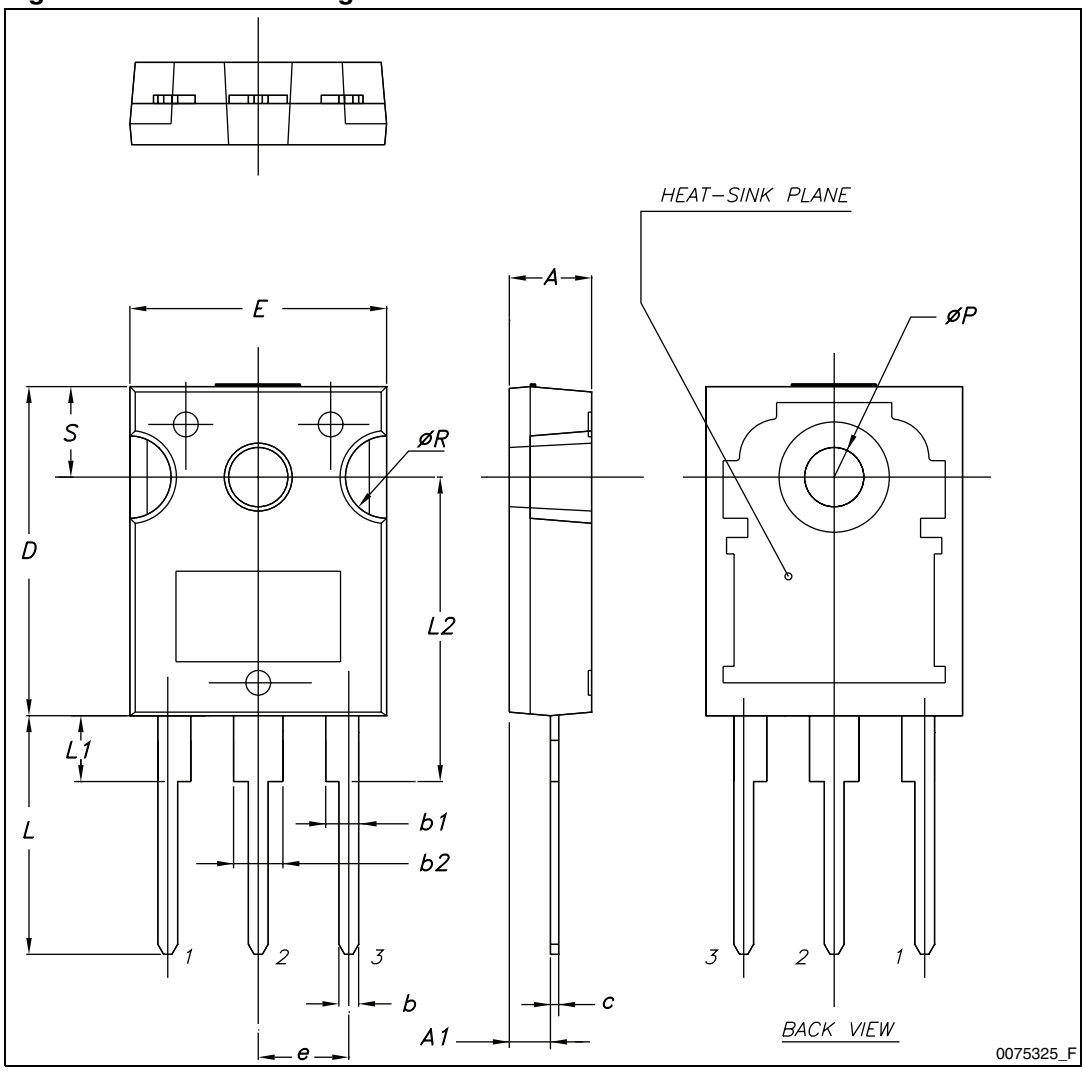


Table 9. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S		5.50	

Figure 9. TO-247 drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
26-Jul-2011	1	First release.

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