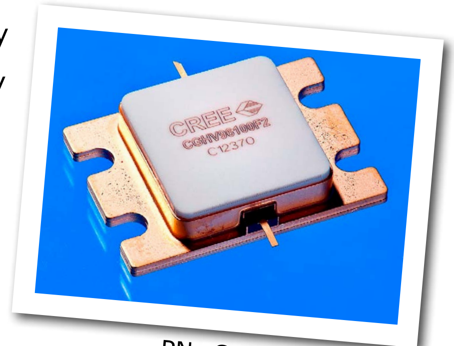
CGHV96100F2

100 W, 7.9 - 9.6 GHz, 50-ohm, Input/Output Matched GaN HEMT

Cree's CGHV96100F2 is a gallium nitride (GaN) High Electron Mobility Transistor (HEMT) on Silicon Carbide (SiC) substrates. This GaN Internally Matched (IM) FET offers excellent power added efficiency in comparison to other technologies. GaN has superior properties compared to silicon or gallium arsenide, including higher breakdown voltage, higher saturated electron drift velocity and higher thermal conductivity. GaN HEMTs also offer greater power density and wider bandwidths compared to GaAs transistors. This IM FET is available in a metal/ceramic flanged package for optimal electrical and thermal performance.



PN: CGHV96100F2
Package Type: 440210

Typical Performance Over 8.4-9.6 GHz (T_C = 25°C)

Parameter	8.4 GHz	8.8 GHz	9.0 GHz	9.2 GHz	9.4 GHz	9.6 GHz	Units
Linear Gain	12.7	12.4	12.7	13.1	13.1	12.4	dB
Output Power	151	147	150	152	140	131	W
Power Gain	10.8	10.6	10.7	10.7	10.5	10.2	dB
Power Added Efficiency	44	42	44	43	45	45	%

Note: Measured in CGHV96100F2-TB (838179) under 100 μS pulse width, 10% duty, Pin 41.0 dBm (12.6 W)

Features

- 8.4 - 9.6 GHz Operation
- 145 W P_{OUT} typical
- 10 dB Power Gain
- 45 % Typical PAE
- 50 Ohm Internally Matched
- <0.3 dB Power Droop

Applications

- Marine Radar
- Weather Monitoring
- Air Traffic Control
- Maritime Vessel Traffic Control
- Port Security

Rev 1.0 – November 2013

Absolute Maximum Ratings (not simultaneous)

Parameter	Symbol	Rating	Units	Conditions
Drain-source Voltage	V_{DSS}	100	Volts	25˚C
Gate-source Voltage	V_{GS}	-10, +2	Volts	25˚C
Power Dissipation	P_{DISS}	115.2 / 222.0	Watts	(CW / Pulse)
Storage Temperature	T_{STG}	-65, +150	˚C	
Operating Junction Temperature	T_J	225	˚C	
Maximum Drain Current[1]	I_{DMAX}	12	Amps	
Maximum Forward Gate Current	I_{GMAX}	28.8	mA	25˚C
Soldering Temperature[2]	T_S	245	˚C	
Screw Torque	τ	40	in-oz	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.63	˚C/W	Pulse Width = 100 µs, Duty Cycle = 10%, P_{DISS} = 222.0 W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.06	˚C/W	CW, 85˚C, P_{DISS} = 115.2 W
Case Operating Temperature[3]	T_C	-40, +150	˚C	

Note:

[1] Current limit for long term reliable operation.

[2] Refer to the Application Note on soldering at http://www.cree.com/rf/tools-and-support/document-library

[3] See also, the Power Dissipation De-rating Curve on Page 9.

Electrical Characteristics (Frequency = 9.6 GHz unless otherwise stated; T_C = 25˚C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(TH)}$	-3.8	-3.0	-2.3	V	V_{DS} = 10 V, I_D = 28.8 mA
Gate Quiscent Voltage	$V_{GS(Q)}$	–	-2.7	–	V	V_{DS} = 40 V, I_D = 1000 mA
Saturated Drain Current[2]	I_{DS}	21.0	26.0	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BD}	100	–	–	V	V_{GS} = -8 V, I_D = 28.8 mA
RF Characteristics[3]						
Small Signal Gain	S21	10.5	12.4	–	dB	V_{DD} = 40 V, I_{DQ} = 1000 mA, P_{IN} = -20 dBm
Input Return Loss 1	S11	–	−5.2	-2.8	dB	V_{DD} = 40 V, I_{DQ} = 1000 mA, P_{IN} = -20 dBm, 8.4 - 9.4 GHz
Input Return Loss 2	S11	–	–	-3.3	dB	V_{DD} = 40 V, I_{DQ} = 1000 mA, P_{IN} = -20 dBm, 9.4 - 9.6 GHz
Output Return Loss	S22	–	−12.3	-6.0	dB	V_{DD} = 40 V, I_{DQ} = 1000 mA, P_{IN} = -20 dBm
Power Output[3,4]	P_{OUT}	100	131.0	–	W	V_{DD} = 40 V, I_{DQ} = 1000 mA, P_{IN} = 41 dBm
Power Added Efficiency[3,4]	PAE	30	45	–	%	V_{DD} = 40 V, I_{DQ} = 1000 mA, P_{IN} = 41 dBm
Power Gain[3,4]	P_G	–	10.2	–	dB	V_{DD} = 40 V, I_{DQ} = 1000 mA, P_{IN} = 41 dBm
Output Mismatch Stress	VSWR	–	–	5:1	Ψ	No damage at all phase angles, V_{DD} = 40 V, I_{DQ} = 1000 mA,

Notes:

[1] Measured on-wafer prior to packaging.

[2] Scaled from PCM data.

[3] Measured in CGHV96100F2-TB (838179) under 100 µS pulse width, 10% duty

[4] Fixture loss de-embedded using the following offsets: Frequency = 9.6 GHz. Input = 0.5 dB and Output = 0.5 dB.

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CGHV96100F2 Typical Performance

Figure 1. - Small Signal Gain and Return Loss vs Frequency of CGHV96100F2 measured in CGHV96100F2-TB
V_{DS} = 40 V, I_{DQ} = 1000mA

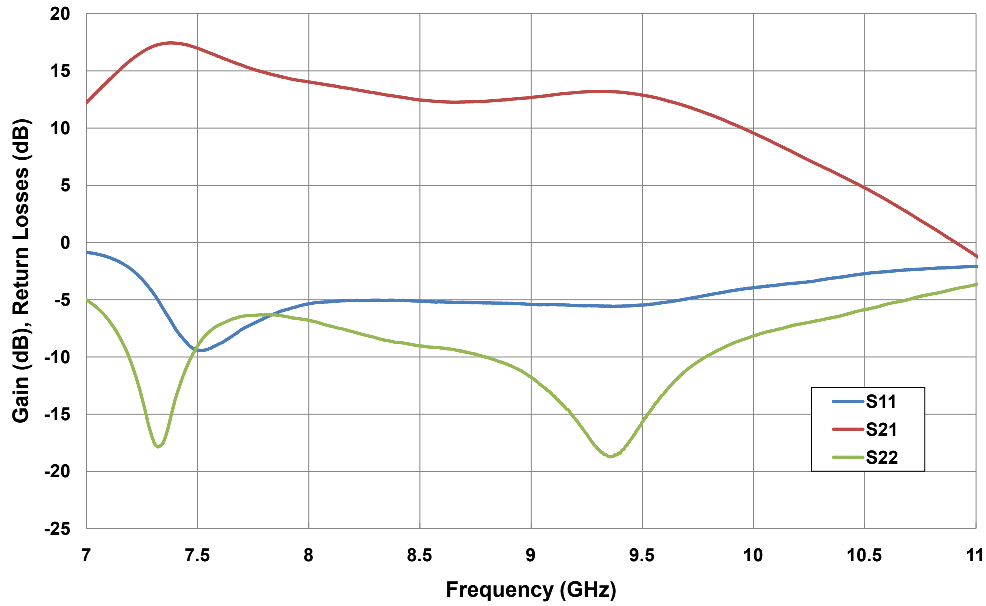

Figure 2. - Power Gain vs. Frequency and Input Power
V_{DD} = 40 V, Pulse Width = 100 µsec, Duty Cycle = 10%

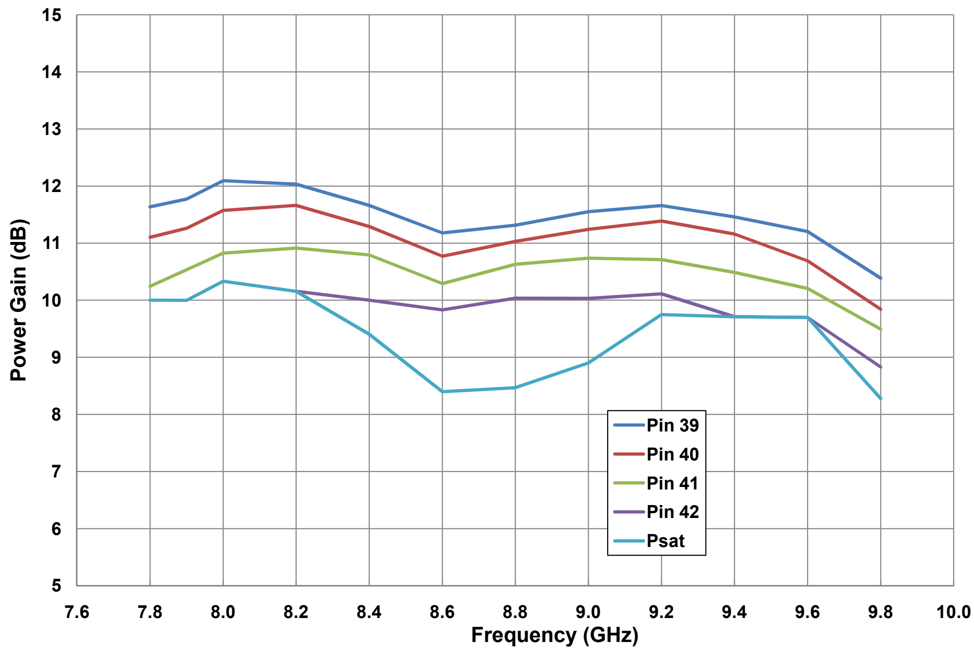

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Figure 3. - Output Power vs. Input Power
V_{DD} = 40 V, Pulse Width = 100 µsec, Duty Cycle = 10%

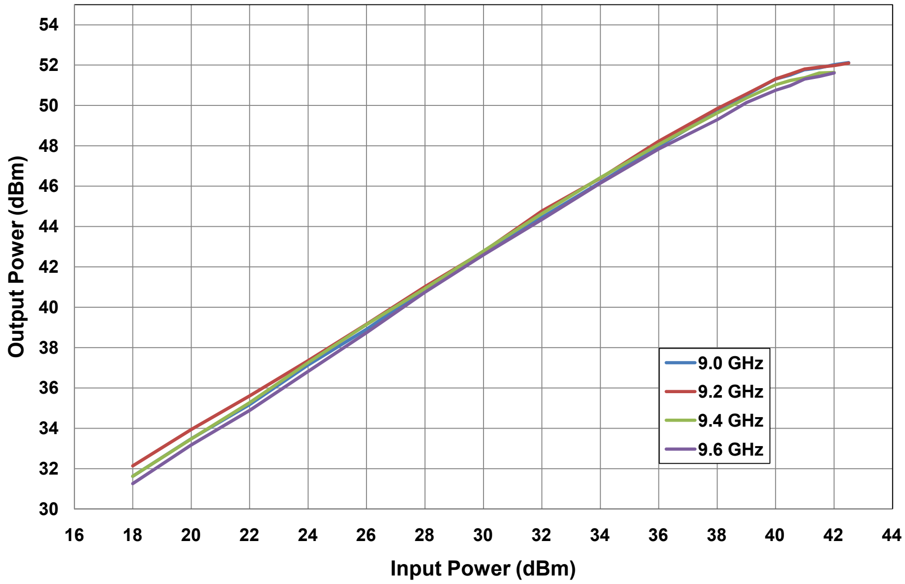

Figure 4. - Power Gain vs. Frequency and Input Power
V_{DD} = 40 V, Pulse Width = 100 µsec, Duty Cycle = 10%

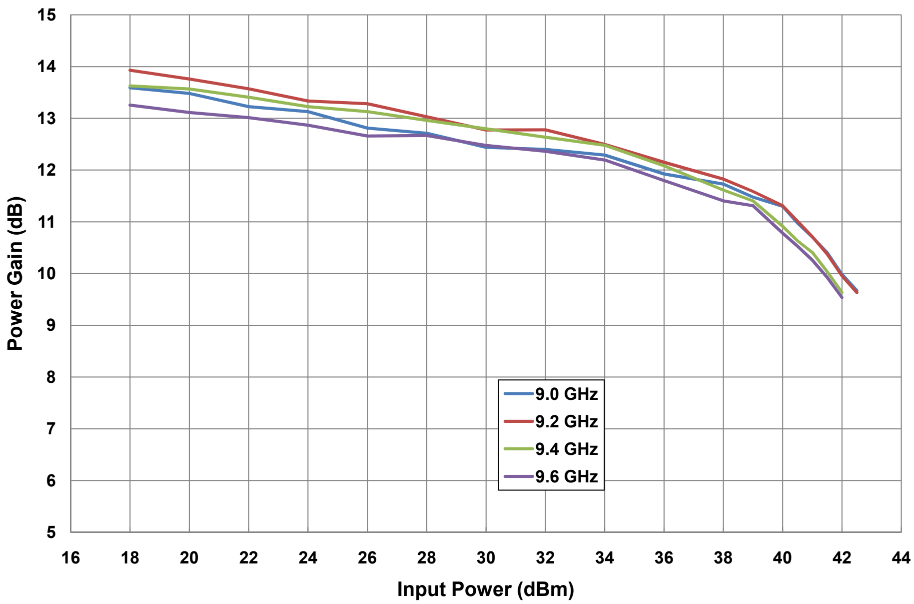

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Figure 5. - Power Added Efficiency vs. Input Power
V_{DD} = 40 V, Pulse Width = 100 μsec, Duty Cycle = 10%

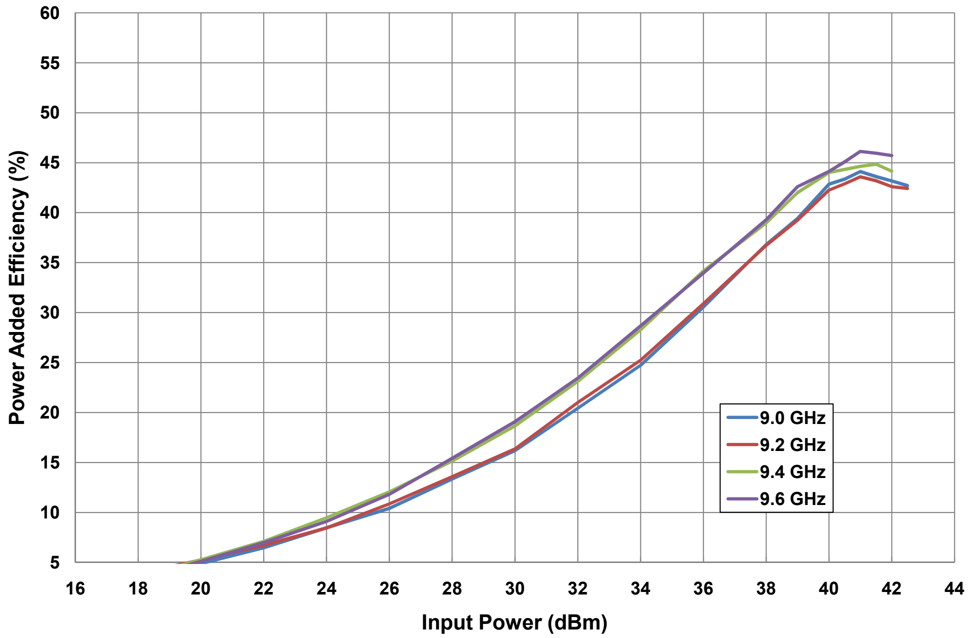

Figure 6. - Output Power vs. Time
V_{DD} = 40 V, P_{IN} = 41 dBm, Duty Cycle = 10%

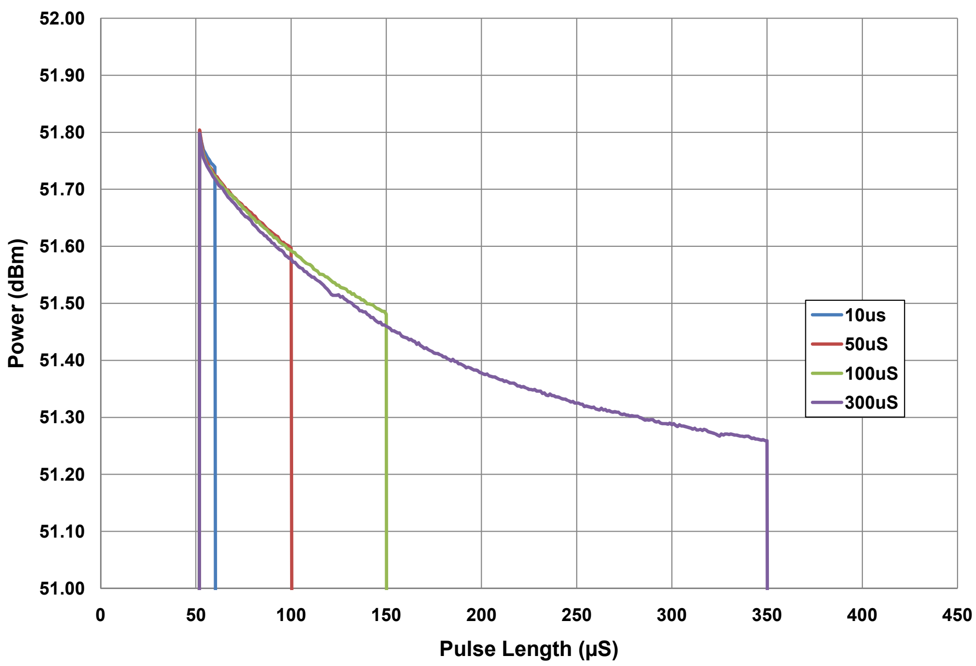

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Figure 7. - Output Power vs. Input Power & Frequency
V_{DD} = 40 V, Pulse Width = 100 µsec, Duty Cycle = 10%

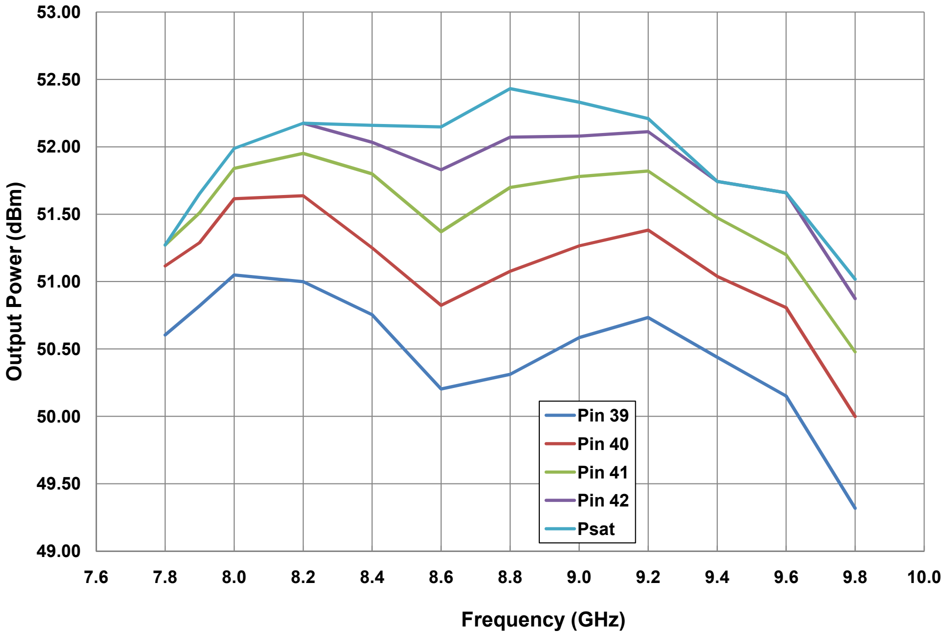
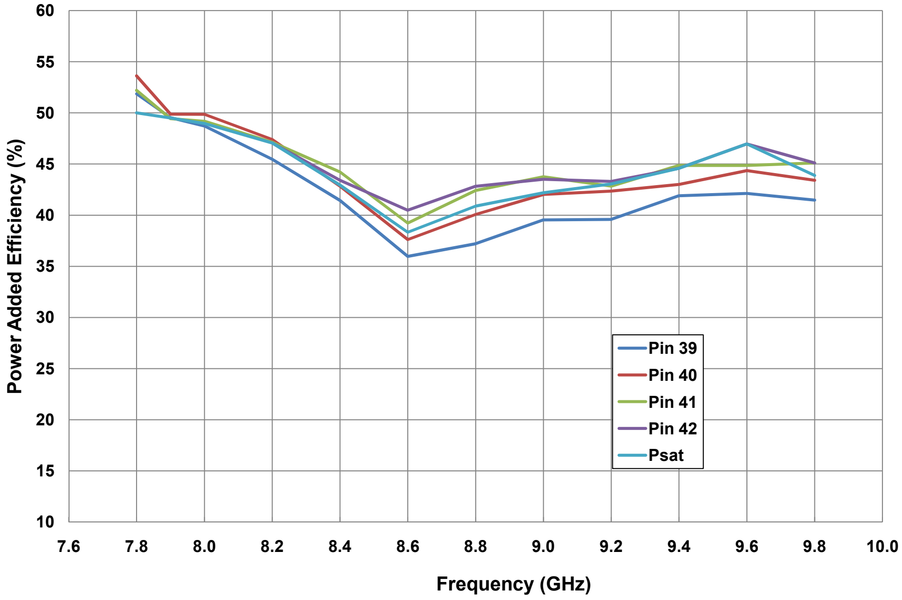


Figure 8. - Power Added Efficiency vs. Input Power & Frequency
V_{DD} = 40 V, Pulse Width = 100 µsec, Duty Cycle = 10%



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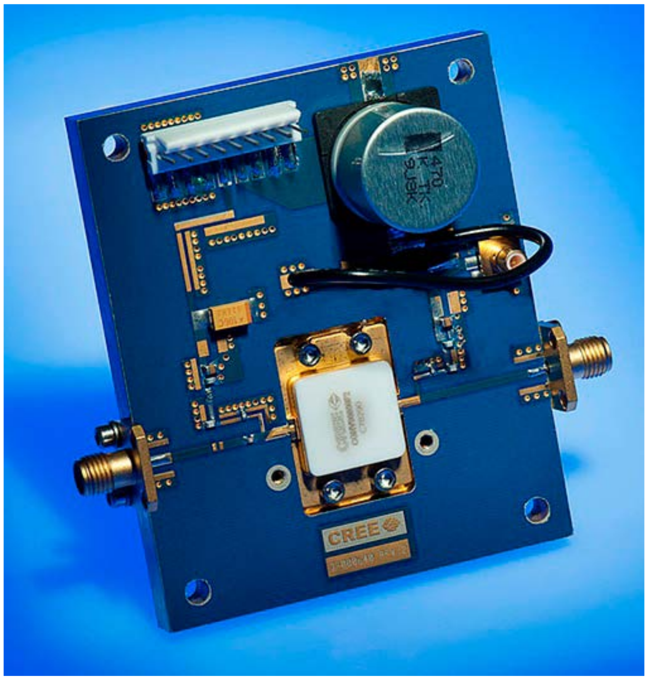
CGHV96100F2-TB Demonstration Amplifier Circuit Bill of Materials

Designator	Description	Qty
R1	RES, 47 OHM +/-1%, 1/16 W, 0603, SMD	1
C1, C11	CAP, 1.6 pF +/-0.05 pF, 0603, ATC 600L	2
C2, C12	CAP, 1.0 pF +/-0.05 pF, 0603, ATC 600L	2
C3, C13	CAP, 10 pF +/-5%, 0603, ATC	2
C4, C14	CAP, 470 pF +/-5%, 100 V, 0603	2
C5, C15	CAP, 33,000 pF, 0805, 100 V, X7R	2
C6	CAP, 10 uF, 16 V, TANTALUM	1
C18	CAP, 470 uF +/-20%, ELECTROLYTIC	1
J1,J2	CONNECTOR, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20MIL	2
J3	CONNECTOR, HEADER, RT>PLZ .1CEN LK 9POS	1
J4	CONNECTOR, SMB, STRAIGHT JACK	1
-	PCB, TEST FIXTURE, TACONICS RF35P, 20 MIL THK, 440210 PKG	1
-	2-56 SOC HD SCREW 1/4 SS	4
-	#2 SPLIT LOCKWASHER SS	4
Q1	CGHV96100F2	1

CGHV96100F2-TB Demonstration Amplifier Circuit



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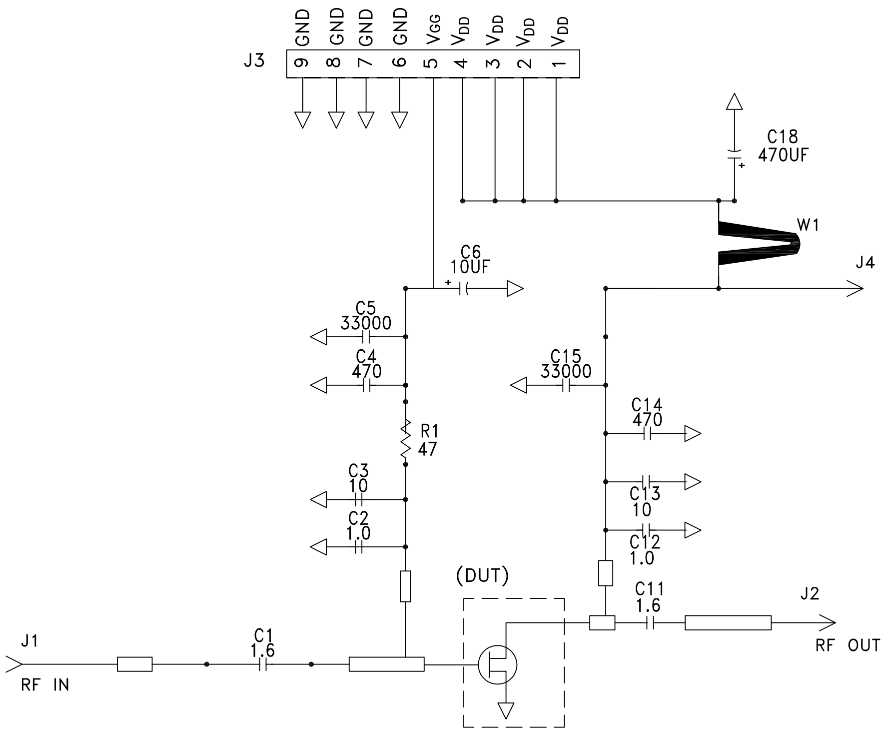
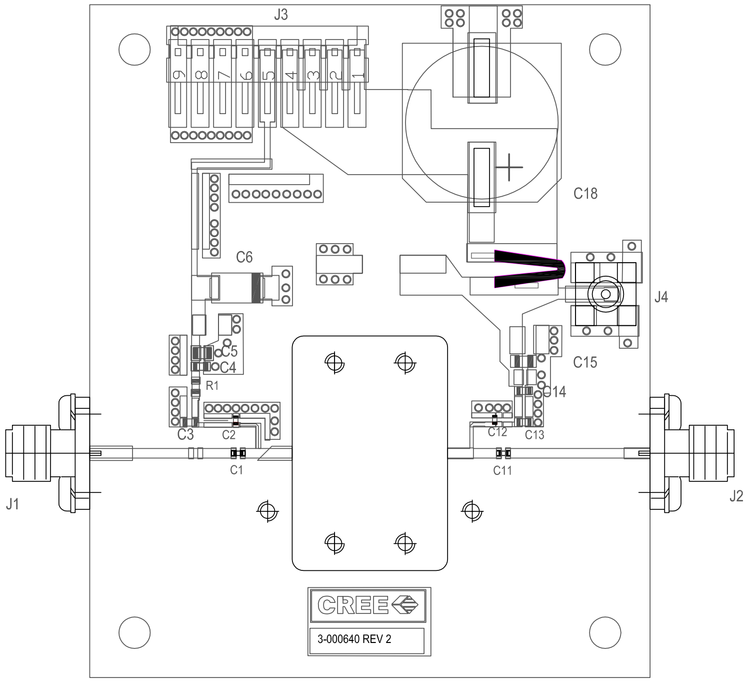
CGHV96100F2-TB Demonstration Amplifier Circuit Schematic



CGHV96100F2-TB Demonstration Amplifier Circuit Outline



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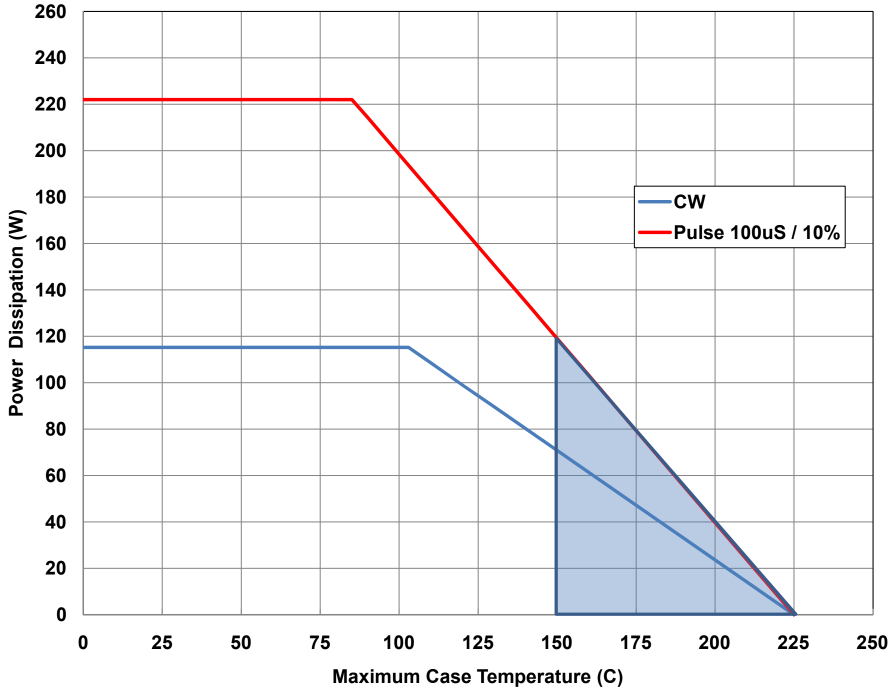
CGHV96100F2 Power Dissipation De-rating Curve



Note. Shaded area exceeds Maximum Case Operating Temperature (See Page 2)

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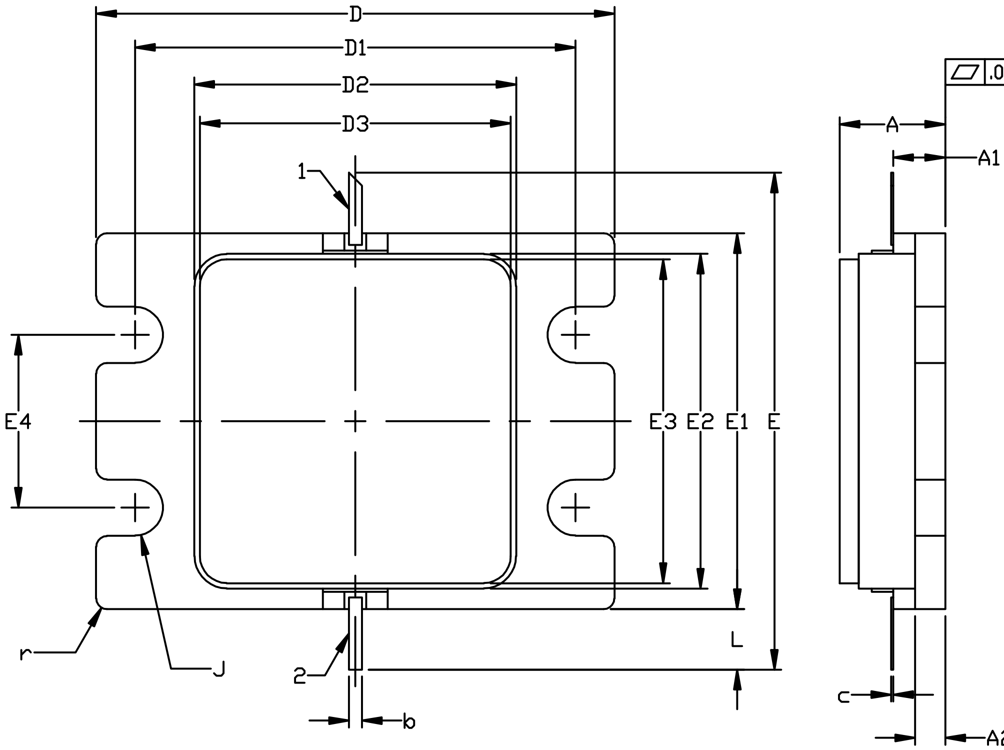
Product Dimensions CGHV96100F2 (Package Type — 440210)

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. INTERPRET DRAWING IN ACCORDANCE WITH ANSI Y14.5M-2009
2. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF .020 BEYOND EDGE OF LID
3. LID MAY BE MISALIGNED TO THE BODY OF PACKAGE BY A MAXIMUM OF .008 IN ANY DIRECTION
4. ALL PLATED SURFACES ARE GOLD OVER NICKEL



1. GATE
2. DRAIN

DIM	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.188	0.198	4.78	5.03	
A1	0.088	0.100	2.24	2.54	2x
A2	0.049	0.061	1.24	1.55	
b	0.022	0.026	0.56	0.66	2x
c	0.002	0.006	0.05	0.15	
D	0.935	0.955	23.75	24.26	
D1	0.797	0.809	20.24	20.55	2x
D2	0.581	0.593	14.76	15.06	
D3	0.563	0.571	14.30	14.50	
E	0.906		23.01		REF
E1	0.679	0.691	17.25	17.55	
E2	0.604	0.616	15.34	15.65	
E3	0.586	0.594	14.88	15.09	
E4	0.309	0.321	7.85	8.15	2x
J	ø0.097	ø0.107	ø2.46	ø2.72	4x
L	0.090	0.130	2.29	3.30	2x
r	0.02 TYP		0.51 TYP		12x

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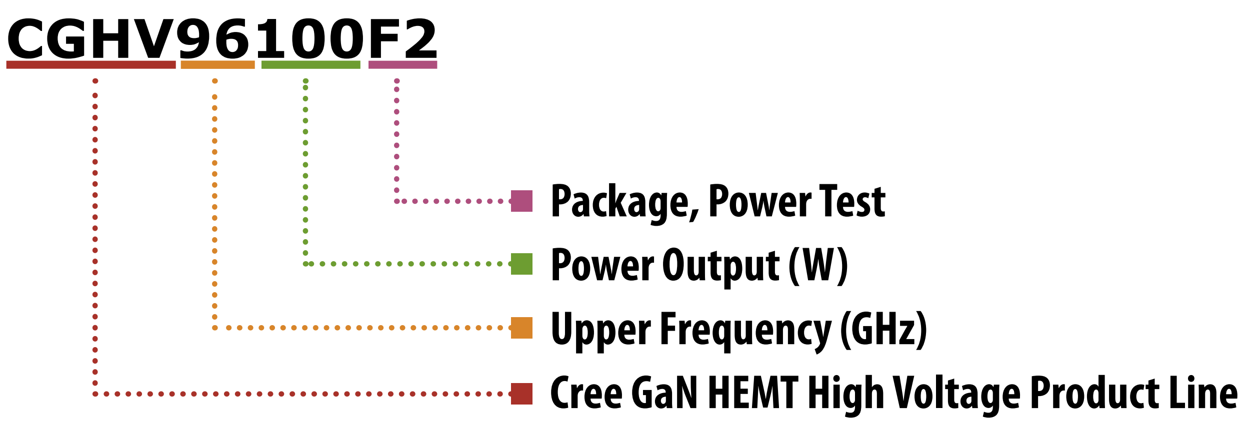
Part Number System



Parameter	Value	Units
Upper Frequency[1]	9.6	GHz
Power Output	100	W
Package	Flange	-

Table 1.

Note[1]: Alpha characters used in frequency code indicate a value greater than 9.9 GHz. See Table 2 for value.

Character Code	Code Value
A	0
B	1
C	2
D	3
E	4
F	5
G	6
H	7
J	8
K	9
Examples:	1A = 10.0 GHz 2H = 27.0 GHz

Table 2.

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