The documentation and process conversion measures necessary to comply with this revision shall be completed by 26 May 2015.

INCH–POUND

MIL–PRF–19500/598C
w/AMENDMENT 2
26 February 2015
SUPERSEDING
MIL–PRF–19500/598C
w/AMENDMENT 1
8 May 2014

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, QUAD, FIELD EFFECT, P-CHANNEL AND N-CHANNEL, SILICON,
14-PIN DUAL INLINE PACKAGE, TYPE 2N7336,
QUALITY LEVELS JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL–PRF–19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for quad N-channel and P-channel, enhancement- mode, MOSFET, power transistor, with avalanche energy ratings (E_{AS} and E_{AR}) and maximum avalanche current (I_{AR}). Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each device type as specified in MIL–PRF–19500.

1.2 Physical dimensions. The device package style is as follows: 14 pin dual-in line package (MO–036AB) in accordance with figure 1.

1.3 Maximum ratings. Unless otherwise specified T_A = +25°C.

P_T (1) T_C = +25°C (free air)		V_{GS}	I_{D1} (2) (3) T_C = +25°C		I_{D2} (2) T_C = +100°C		I_S		E_{AS}	E_{AR}	T_{op} and T_{STG}
W	W	V dc	A dc		A dc		A dc		mJ	mJ	°C
(1 die)	(4 die)		N-channel	P-channel	N-channel	P-channel	N-channel	P-channel			
1.4	2.5	±20	1.0	–.75	.6	–.5	1.0	–.75	75	.14	–55 to +150

I_{AR}		I_{DM} (4)		Max $r_{DS(on)}$ (5) V_{GS} = 10 V dc, $I_D = I_{D2}$				$R_{\theta JA1}$ max (1 die)	$R_{\theta JA2}$ max (4 die)	$R_{\theta JC}$ max
				T_J = +25°C		T_J = +150°C				
A		A (pk)		Ω		Ω		°C/W	°C/W	°C/W
N-channel	P-channel	N-channel	P-channel	N-channel	P-channel	N-channel	P-channel			
1.0	–.75	4.0	–3.0	0.7	1.4	1.4	2.5	90	50	17

See footnotes on next page.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

1.3 Maximum ratings – Continued.

(1) Derate linearly 0.011 W/°C for T_C > +25°C.
(2) The following formula derives the maximum theoretical I_D limit. I_D is also limited by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) x (R_{DS(on)} at T_{JM})}}$$

(3) See figure 2, maximum drain current graph.
(4) I_{DM} = 4 x I_{D1} as calculated in note 2.
(5) Pulsed (see 4.5.1).

1.4 Primary electrical characteristics. Unless otherwise specified, T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 V I_D = 1 mA dc	$V_{GS(th)1}$ $V_{DS} \geq V_{GS}$ I_D = 0.25 mA	Max I_{DSS1} V_{GS} = 0 V	Max $r_{DS(on)1}$ (1) V_{GS} = 10 V dc, $I_D = I_{D2}$	
			V_{DS} = 80 percent of rated V_{DS}	T_J = +25°C	
	V dc	V dc	µA dc	Ω	
		Min Max		N-channel	P-channel
2N7336	100	2.0 4.0	25	0.7	1.4

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL–PRF–19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

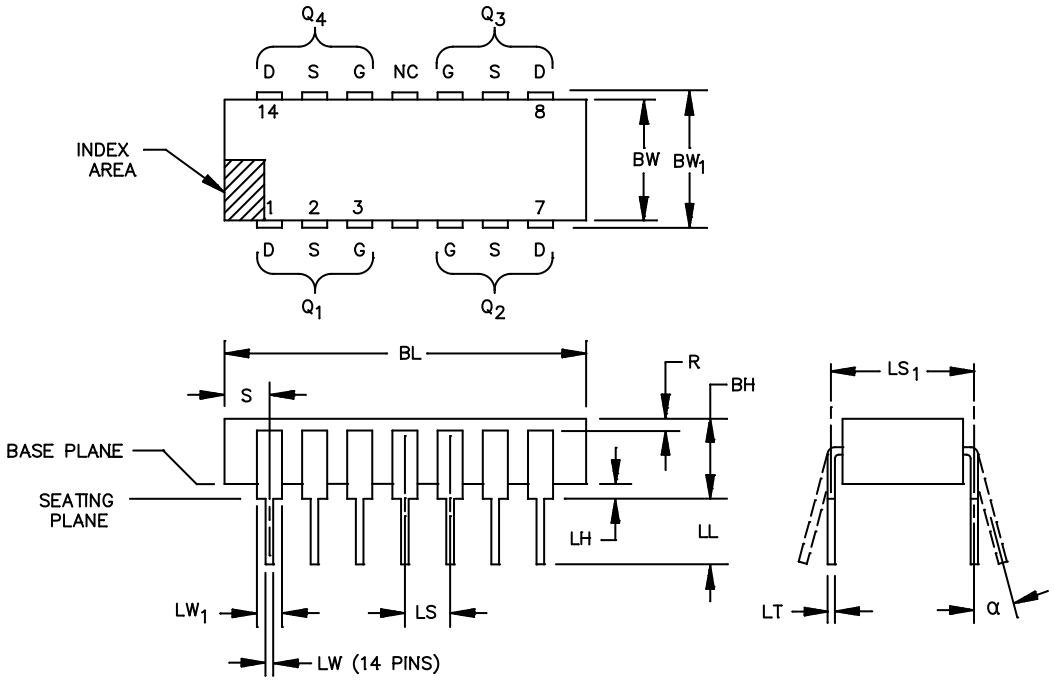
1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet is "7336".

1.5.3 Suffix symbols. Suffix symbols are not applicable for this specification sheet.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QML–19500.



Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.105	.175	2.67	4.45	4
BL	.690	.770	17.53	19.56	
BW	.280	.310	7.11	7.87	
BW_1	.290	.325	7.37	8.26	5
LH	.025	.055	0.64	1.40	4, 6
LL	.125	.175	3.18	4.45	4
LT	.008	.012	0.203	0.305	

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
LS	.100 TP		2.54 TP		7
LS_1	.300 TP		7.62 TP		7
LW_1	.038	.060	0.97	1.52	
LW	.015	.021	0.381	0.533	6
R	.010		0.25		
S	.030	.095	0.76	2.41	
α	0°	15°	0°	15°	8

NOTES:
1. Dimensions are in inches. Millimeters are for general information only.
2. Pin-out: G = gate, S = source, D = drain, and NC = not connected.
3. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1. The manufacturer's identification shall not be used as a pin 1 identification mark.
4. This dimension shall be measured with the device seated in seating plane gauge JEDEC Outline No. GS–3.
5. Lead center when α is 0°. BW_1 shall be measured at the centerline of the leads.
6. Outlines on which the seating plane is coincident with the base plane (LH = 0), terminals lead standoffs are not required, and LW_1 may equal LW along any part of the lead above the seating/base plane.
7. Leads within .005 inch (0.13 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed. Twelve spaces.
8. α applies to spread leads prior to installation.
9. Dimensioning and tolerancing in accordance with ASME Y14.5.

FIGURE 1. Physical dimensions and configuration (MO–036AB).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL–PRF–19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL–STD–750 – Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL–PRF–19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL–PRF–19500.

I_{AS} Rated avalanche current, nonrepetitive.
nC nano coulomb.

3.4 Interface and physical dimensions. The interface requirements and physical dimensions shall be as specified in MIL–PRF–19500 and on figure 1 (MO-036AB) herein.

3.4.1 Lead finish. Unless otherwise specified, the lead finish shall be solderable as defined in MIL–STD–750, MIL–PRF–19500, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Pin out. The pin out of the device types shall be as shown on figure 1.

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.5.1 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.5.2 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of electrostatic charge. The following handling practices shall be followed:

a. Devices shall be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100\ k\Omega$, whenever bias voltage is to be applied drain to source.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Marking. Marking shall be in accordance with MIL–PRF–19500.

3.8 Workmanship. Devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I, II and III).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL–PRF–19500, and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification that did not request the performance of table III tests, the tests specified in table III herein shall be performed by the first inspection lot of this revision to maintain qualification.

4.3 Screening (quality levels JANS, JANTX and JANTXV only). Screening shall be in accordance with table E–IV of MIL–PRF–19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurement (1) (2)	
	Quality level JANS	Quality levels JANTX and JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3) (4)	Method 3470 of MIL–STD–750, (see 4.3.2) optional	Method 3470 of MIL–STD–750, (see 4.3.2) optional
3c (3)	Method 3161 of MIL–STD–750, (see 4.3.3)	Method 3161 of MIL–STD–750, (see 4.3.3)
9	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, see table I subgroup 2 herein	See table I, subgroup 2 herein
10	Method 1042 of MIL–STD–750, test condition B	Method 1042 of MIL–STD–750, test condition B
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(th)1}$ Subgroup 2 of table I herein; ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 μA dc or ±100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(th)1}$ Subgroup 2 of table I herein
12	Method 1042 of MIL–STD–750, test condition A, t = 240 hours.	Method 1042 of MIL–STD–750, test condition A
13	Subgroups 2 and 3 of table I herein; ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ±20 percent of initial value $\Delta V_{GS(th)1}$ = ±20 percent of initial value.	Subgroup 2 of table I herein; ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ±20 percent of initial value $\Delta V_{GS(th)1}$ = ±20 percent of initial value.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS}, and $V_{GS(th)1}$ shall be invoked.
(3) Shall be performed anytime before screen 9.
(4) This test method in no way implies a repetitive single pulse avalanche energy rating. This test need not be performed in group A when performed as a screen.

4.3.1 Gate stress test. Apply V_{GS} = +30 V minimum for t = 250 µs minimum.

4.3.2 Single pulse avalanche energy (E_{AS}). The single pulse avalanche energy capability shall be determined in accordance with method 3470 of MIL–STD–750. The following details shall apply:

a. Peak current, I_{AS} — I_{D1}.

b. Peak gate voltage, V_{GS} — 10 V.

c. Gate to source resistor, R_{GS} — $25 \leq R_{GS} \leq 200\Omega$.

d. Initial case temperature — +25°C +10, –5°C.

e. Inductance — $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR}-V_{DD}}{V_{BR}}\right]$ mH minimum.

f. Number of pulses to be applied — 1 pulse minimum.

g. Supply voltage (V_{DD}) — 25 V minimum.

4.3.3 Thermal impedance (ΔV_{SD} measurements). The ΔV_{SD} measurements shall be performed in accordance with method 3161 of MIL–STD–750. The ΔV_{SD} conditions (I_H and V_H) and maximum limit shall be derived by each vendor from the thermal response curves (see figure 3). The ΔV_{SD} measurement and conditions for each device in the qualification lot shall be submitted (read and record) in the qualification report. The chosen ΔV_{SD} shall be considered final after the manufacturer has had the opportunity to test five consecutive lots. The following parameter measurements shall apply:

a. I_M measuring current — 10 mA.

b. I_H drain heating current — 0.15 A minimum.

c. t_H heating time — 100 ms.

d. V_H drain-source heating voltage — 15 V minimum.

e. t_{MD} measurement time delay — 30 to 60 µs.

f. t_{SW} sample window time — 10 µs maximum.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL–PRF–19500, and as specified herein. Alternate flow is allowed for quality conformance inspection in accordance with appendix E of MIL–PRF–19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E–V of MIL–PRF–19500, and table I herein. End-point electrical measurements shall be in accordance with the applicable steps of table II herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E–VIA (JANS) and table E–VIB (JAN, JANTX, and JANTXV) of MIL–PRF–19500, and herein.

4.4.2.1 Quality level JANS (table E–VIA of MIL–PRF–19500).

Subgroup	Method	Conditions
B3	1051	Condition G.
B3	2077	As specified.
B5	1042	Condition A (reverse bias), V_{DS} = 80 percent of rated, T_A = +175°C, t = 120 hours.
B5	1042	Condition B (gate stress), V_{GS} = 80 percent of rated, T_A = +175°C, t = 24 hours.
B6	3161	See 4.5.2.

4.4.2.2 Quality levels JAN, JANTX, and JANTXV (table E–VIB of MIL–PRF–19500).

Subgroup	Method	Conditions
B2	1051	Condition G.
B3	1042	Condition A, V_{DS} = 80 percent of rated, T_A = +150°C, t = 160 hours.
		Condition B, V_{GS} = 80 percent of rated, T_A = +150°C, t = 24 hours.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E–VII of MIL–PRF–19500 and as follows herein.

Subgroup	Method	Conditions
C2	2036	Condition E, the sampling plan applies to the number of leads tested. A minimum of three devices shall be tested.
C5	3161	See 4.5.2.
C6	1042	Condition A, V_{DS} = 80 percent of rated, T_A = +150°C, t = 340 hours. Electrical measurements in accordance with table I, subgroup 2 herein.
		Condition B, V_{GS} = 80 percent of rated, T_A = +150°C, t = 24 hours.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E–IX of MIL–PRF–19500, and as specified in table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse response measurements. Conditions for pulse response measurement shall be as specified in section 4 of MIL–STD–750.

4.5.2 Thermal resistance. Thermal resistance measurements shall be performed in accordance with method 3161 of MIL–STD–750. $R_{\theta JA1}$ maximum = 90°C/W. $R_{\theta JA1}$ shall be performed on each die. The following details shall apply:

a.	I_M measuring current	10 mA.
b.	I_H drain heating current	0.15 A minimum.
c.	t_H heating time	Steady-state (see method 3161 of MIL–STD–750 for definition).
d.	V_H drain-source heating voltage	15 V minimum.
e.	t_{MD} measurement time delay	30 to 60 μs.
f.	t_{SW} sample window time	10 μs maximum.

TABLE I. Group A inspection.

Inspection 1/	MIL–STD–750		Symbol	Limit		Unit
	Method	Conditions		Max	Min	
Subgroup 1						
Vizsual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$		10	°C/W
Breakdown voltage, drain to source	3407	Bias condition C, V_{GS} = 0V, I_D = 1 mA dc	$V_{(BR)DSS}$	100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 0.25 mA	$V_{GS(th)1}$	2.0	4.0	V dc
Gate current (forward)	3411	Bias condition C, V_{GS} = +20V dc, V_{DS} = 0 V dc	I_{GSSF1}		+100	nA dc
Gate current (reverse)	3411	Bias condition C, V_{GS} = - 20 V dc, V_{DS} = 0 V dc	I_{GSSR1}		–100	nA dc
Drain current	3413	Bias condition C, V_{GS} = 0 V dc, V_{DS} = 80 percent of rated V_{DS}	I_{DSS1}		25	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 10 V dc, condition A, pulsed (see 4.5.1), I_D = rated I_{D2}, (see 1.3)	$r_{DS(on)1}$			
N-channel					0.7	Ω
P-channel					1.4	Ω
Forward voltage	4011	Condition A, V_{GS} = 0 V dc, I_D = rated I_{D1}, pulsed (see 4.5.1)	V_{SD}			
N-channel					1.5	V dc
P-channel					5.5	V dc
Subgroup 3						
High temperature operation:		$T_C = T_J$ = +125°C				
Gate current	3411	Bias condition C, V_{GS} = +20V dc and –20 V dc, V_{DS} = 0 V dc,	I_{GSS2}		±200	nA dc
Drain current	3413	Bias condition C, V_{GS} = 0 V dc, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		0.25	mA dc

See footnote at end of table.

TABLE I. Group A inspection – Continued.

Inspection 1/	MIL–STD–750		Symbol	Limit		Unit
	Method	Conditions		Max	Min	
Subgroup 3 – continued						
Static drain to source on-state resistance	3421	Bias condition A, V_{GS} = 10 V dc, I_D = rated I_{D2}, pulsed (see 4.5.1)	$r_{DS(on)2}$			
N-channel					1.4	Ω
P-channel					2.3	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 0.25 mA	$V_{GS(th)2}$	1.0		V dc
Low temperature operation:		$T_C = T_J$ = –55°C				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 0.25 mA	$V_{GS(th)3}$		5.0	V dc
Subgroup 4						
Switching time test	3472	I_D = rated I_{D1}; V_{GS} = 10 V dc, R_G = 7.5 Ω; V_{DD} = 50 percent of $V_{(BR)DSS}$				
Turn-on delay time			$t_{d(on)}$			
N-channel					20	ns
P-channel					30	ns
Rise time			t_r			ns
N-channel					25	ns
P-channel					60	ns
Turn-off delay time			$t_{d(off)}$			
N-channel					40	ns
P-channel					70	ns
Fall time			t_f			
N-channel					40	ns
P-channel					80	ns

See footnote at end of table.

TABLE I. Group A inspection – Continued.

Inspection 1/	MIL–STD–750		Symbol	Limit		Unit
	Method	Conditions		Max	Min	
Subgroup 5						
Single pulse unclamped inductive switching 3/	3470	See 4.3.2, n = 116, c = 0	E_{AS}			
Electrical measurements		See subgroup 2 of this table				
Safe operating area test for power MOSFETs	3474	V_{DS} = 80 percent of rated $V_{(BR)DSS}$, t_p = 10 ms, (see figure 4)				
N-channel		I_D = 0.25 A				
P-channel		I_D = 0.5 A				
Electrical measurements		See subgroup 2 of this table and table II, step 7				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B				
On-state gate charge			$Q_{g(on)}$		15	nC
Gate to source charge			Q_{gs}			
N-channel					7.5	nC
P-channel					7.0	nC
Gate to drain charge			Q_{gd}			nC
N-channel					7.5	nC
P-channel					8.0	nC
Reverse recovery time	3473	Condition A, $d_i/d_t \leq -100$ A/µs, $V_{DD} \leq 30$ V, $I_D = I_{D1}$, (see 1.3)	t_{rr}		200	ns

1/ For sampling plan, see MIL–PRF–19500.
2/ This test is required for the following end-point measurement only (not intended for screen 9, 11, or 13): JANS, table E–VIA of MIL–PRF–19500, group B, subgroups 3 and 4; JAN, JANTX, and JANTXV, table E–VIA of MIL–PRF–19500, group B, subgroups 2 and 3; and table E–VII of MIL–PRF–19500, group C, subgroup 6, and table E–IX of MIL–PRF–19500, group E, subgroup 1.
3/ This test need not be performed in group A if performed in screening.

TABLE II. Group A, B, C, and E electrical end-point measurements. 1/ 2/ 3/ 4/ 5/

Step	Inspection	MIL–STD–750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1	Breakdown voltage drain to source	3407	Bias condition C; V_{GS} = 0 V, I_D = 1.0 mA dc	$V_{(BR)DSS}$	100		V dc
2	Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 0.25 mA dc.	$V_{GS(th)1}$	2.0	4.0	V dc
3	Gate current	3411	Bias condition C; V_{GS} = ±20 V dc	I_{GSS1}		±100	nA dc
4	Drain current	3413	Bias condition C; V_{GS} = 0 V dc, V_{DS} = 80 percent of rated V_{DS}	I_{DSSS1}		25	µA dc
5	Static drain to source on-state resistance N-channel P-channel	3421	Bias condition A; V_{GS} = 10 V dc, pulsed (see 4.5.1); $I_D = I_{D2}$	$r_{DS(on)1}$		 0.7 1.4	Ω
6	Forward voltage N-channel P-channel	4011	Condition A; pulsed (see 4.5.1) V_G = 0 V; $I_D = I_{D1}$	V_{SD}		 1.5 5.5	V
7	Thermal response	3161	See 4.3.3	ΔV_{SD}			

1/ The electrical measurements for group B, quality level JANS, shall be as follows:
- a. In addition to the measurements specified for subgroup 3 of table E–VIA of MIL–PRF–19500, the measurements of steps 1, 2, 3, 4, 5, 6 and 7 shall also be taken.
- b. In addition to the measurements specified for subgroup 5 of table E–VIA of MIL–PRF–19500, the accelerated steady state gate stress of steps 1, 2, 3, 4, 5 and 6 shall also be taken.
- c. In addition to the measurements specified for subgroup 5 of table E–VIA of MIL–PRF–19500, the accelerated steady state reverse bias of steps 1, 2, 3, 4, 5 and 6 shall also be taken. No more than 15 percent of the sample shall be permitted to have a $\Delta V_{BR(DSS)}$ shift of more than 10 percent and Δ_{IDSS} greater than 50 µA.

2/ The electrical measurements for group B, quality levels JAN, JANTX and JANTXV shall be as follows:
- a. In addition to the measurements specified for subgroup 2 of table E–VIB of MIL–PRF–19500, the measurements of steps 1, 2, 3, 4, 5, 6 and 7 shall also be taken.
- b. In addition to the measurements specified for subgroup 3 of table E–VIB of MIL–PRF–19500, the accelerated steady state gate stress of steps 1, 2, 3, 4, 5 and 6 shall also be taken.
- c. In addition to the measurements specified for subgroup 3 of table E–VIB of MIL–PRF–19500, the accelerated steady state reverse bias of steps 1, 2, 3, 4, 5 and 6 shall also be taken.

3/ The electrical measurements for group C, shall be as follows:
- a. In addition to the measurements specified for subgroup 2 of table E–VII of MIL–PRF–19500, the measurements of steps 1, 2, 3, 4, 5, 6 and 7 shall also be taken.
- b. In addition to the measurements specified for subgroup 3 of table E–VII of MIL–PRF–19500, the measurements of step 1, 2, 3, 4, 5 and 6 shall also be taken.
- c. In addition to the measurements specified for subgroup 6 of table E–VII of MIL–PRF–19500, the steady state gate stress measurements of step 1, 2, 3, 4, 5 and 6 shall also be taken.
- d. In addition to the measurements specified for subgroup 6 of table E–VII of MIL–PRF–19500, the steady state reverse bias measurements of step 1, 2, 3, 4, 5 and 6 shall also be taken.

TABLE II. Group A, B, C, and E electrical end-point measurements – Continued.

4/ The electrical measurements for group E, all quality levels, shall be as follows:
   a. In addition to the measurements specified for subgroup 1 of table E–IX of MIL–PRF–19500, the measurements of steps 1, 2, 3, 4, 5, 6 and 7 shall also be taken.
   b. In addition to the measurements specified for subgroup 2 of table E–IX of MIL–PRF–19500, the measurements of steps 1, 2, 3, 4, 5 and 6 shall also be taken.

5/ Devices which exceed the table I (group A) limits for this test shall not be acceptable.

TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL–STD–750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Condition G, 500 cycles.	
Hermetic seal Fine leak Gross leak	1071		
End-point electrical measurements		See table I, subgroup 2 and table II, step 7.	
Subgroup 2 1/			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		See table I, subgroup 2.	
Steady-state gate bias	1042	Condition B, 1,000 hours.	
End-point electrical measurements		See table I, subgroup 2 and table II, step 7.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL–PRF–19500.	
Subgroup 6			11 devices
Electrostatic discharge sensitivity	1020		
Subgroup 11	3476		22 devices c = 0
Test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors			

1/ A separate sample for each test may be selected pulled.

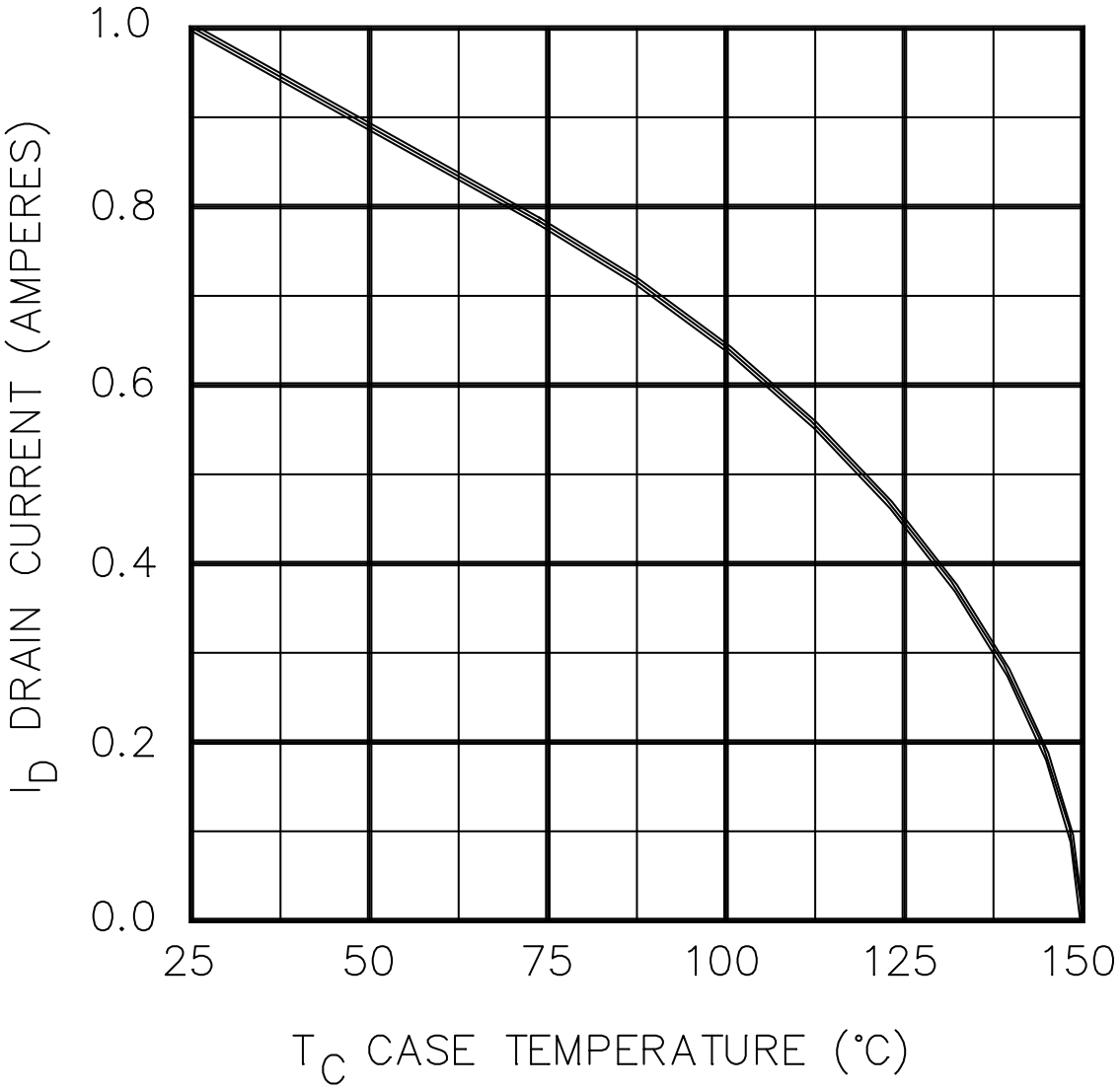
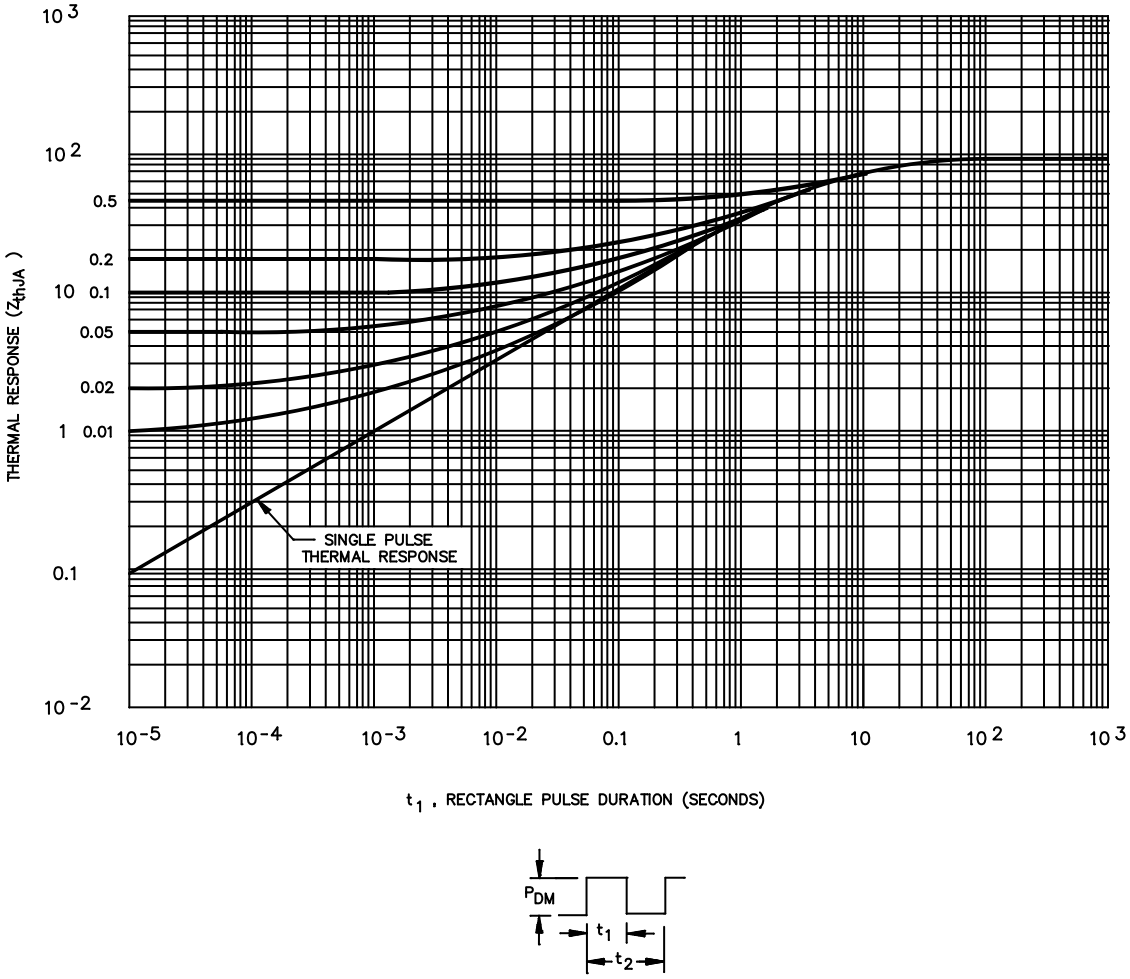


FIGURE 2. Maximum drain current versus case temperature graph.



NOTES:

1. Curves are from bottom to top are: Single pulse, D = 0.01, D = 0.02, D = 0.05, D = 0.1, and D = 0.5.
2. Pulse duration magnitude = P_{DM}.
3 Duty factor D = t_1 / t_2.
4 Peak $T_J = P_{DM} \times Z_{thJA} + T_C$.

FIGURE 3. Thermal response curves.

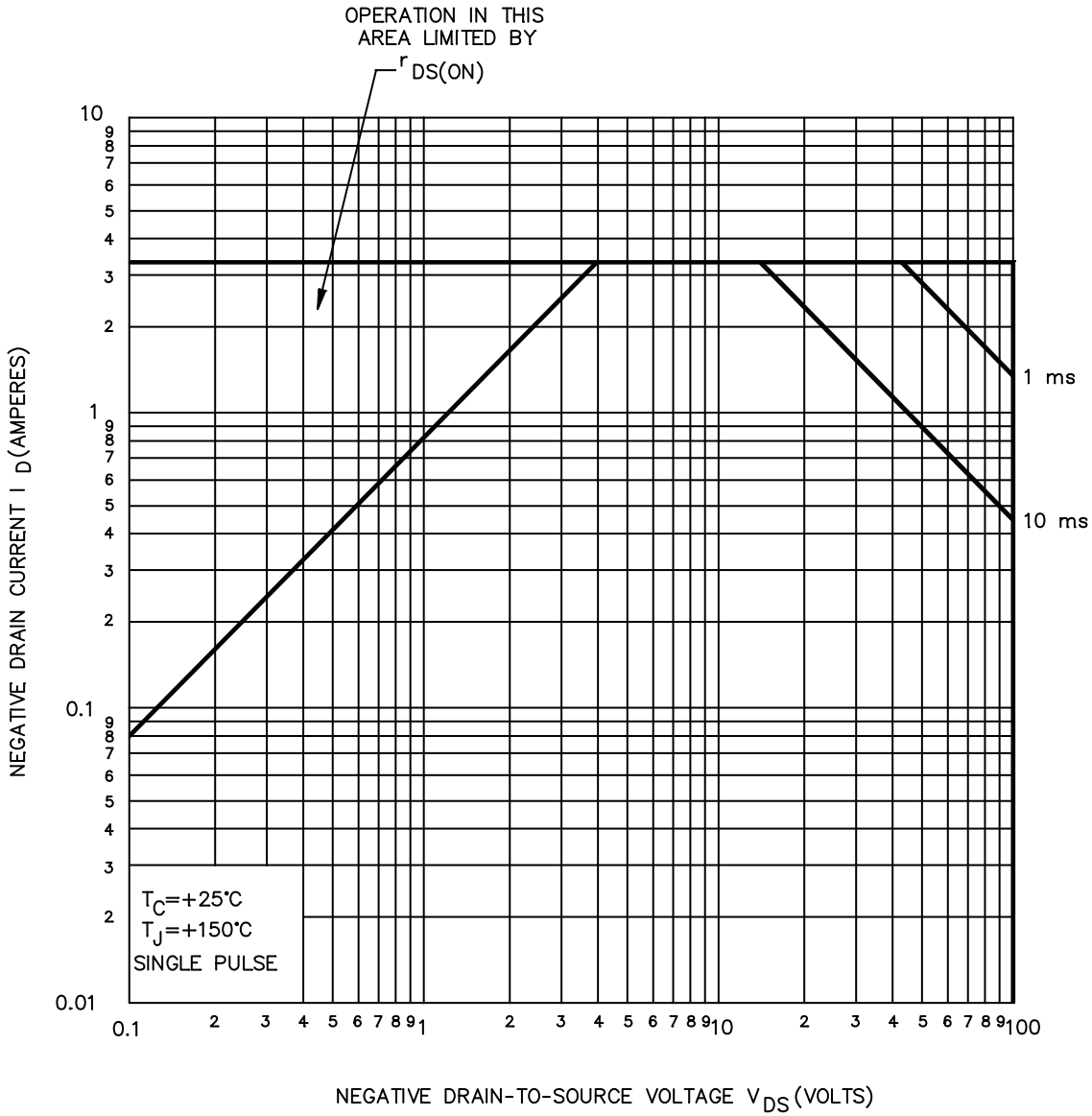


FIGURE 4. Maximum safe operating area.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL–PRF–19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

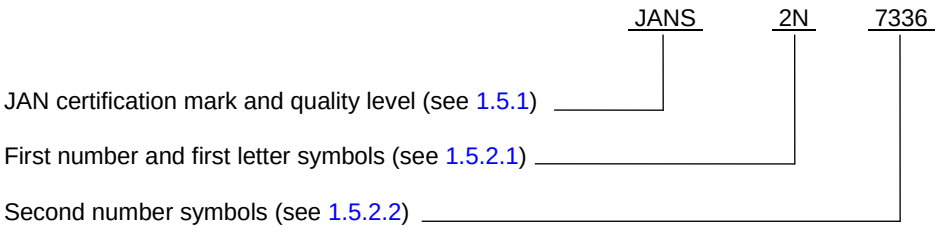
b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5, 6.4 and 6.5.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



6.5 List of PINs. The following is a list of possible PINs available for encapsulated devices covered by this specification sheet.

JAN2N7336
JANTX2N7336
JANTXV2N7336
JANS2N7336

6.6 Substitution information. Devices covered by this specification are substitutable for the manufacturers' and users' PIN. This information in no way implies that manufacturers' part numbers are suitable as a substitute for the military PIN.

Military PIN	Manufacturers' CAGE code	Manufacturers' and users' PIN
2N7336	59993	IRFG6110

6.7 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at "Semiconductor@.dla.mil" or by facsimile (614) 693–1642 or DSN 850–6939.

6.8 Changes from previous issue. The margins of this specification are marked with vertical lines to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
Army – CR
Navy – EC
Air Force – 85
NASA – NA
DLA – CC

Review activities:
Army – MI, SM
Navy – AS, MC
Air Force – 19, 99

Preparing activity:
DLA – CC

(Project 5961–2015–020)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.