The documentation and process conversion measures necessary to comply with this revision shall be completed by 1 February 2015.

INCH-POUND

MIL-PRF-19500/564J
1 November 2014
SUPERSEDING
MIL-PRF-19500/564H
2 June 2009

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, FIELD EFFECT, P-CHANNEL, SILICON,
TYPES 2N6849, 2N6849U, 2N6851 AND 2N6851U,
JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for a P-channel, enhancement-mode, MOSFET, power transistor for use in particular power-switching applications.. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each encapsulated device type as specified in MIL-PRF-19500. Two levels of product assurance (JANHC and JANKC) are provided for each unencapsulated device type.

* 1.2 Package outlines. The device package outlines are as follows: TO-205AF (formerly TO-39) in accordance with figure 1, surface mount version, "U" suffix (leadless chip carrier, LCC), see figure 2 for dimensions. The dimensions and topography for JANHC and JANKC unencapsulated die are as follows: "A" version die in accordance with figure 3 and "B" version die in accordance with figure 4.

* 1.3 Maximum ratings. Unless otherwise specified, T_C = +25°C.

Type	P_T (1) T_C = +25°C	P_T T_A = +25°C	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) T_C = +25°C	I_{D2} (3) (4) T_C = +100°C	I_S	I_{DM} (5)	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A (pk)	°C
2N6849, 2N6849U	25	0.8	5.0	-100	-100	±20	-6.5	-4.1	-6.5	-25	-55 to +150
2N6851, 2N6851U	25	0.8	5.0	-200	-200	±20	-4.0	-2.4	-4.0	-16	-55 to +150

(1) Derate linearly by 0.2 W/°C for T_C > +25°C.
(2) See figure 5, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D spec. I_D is limited by package and device construction.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 6, maximum drain current graphs.
(5) $I_{DM} = 4 \times I_{D1}$ as calculated in note 2.

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

1.4 Primary electrical characteristics. Unless otherwise specified, T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = -1 mA dc	$V_{GS(th)1}$ $V_{DS} \geq V_{GS}$ I_D = -0.25 mA		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}	Max $r_{DS(on)1}$ (1) V_{GS} = -10 V dc $I_D = I_{D2}$	
					T_J = +25°C	T_J = +150°C
	V dc	V dc Min	V dc Max	µA dc	ohm	ohm
2N6849, 2N6849U	-100	-2.0	-4.0	-25	0.30	0.60
2N6851, 2N6851U	-200	-2.0	-4.0	-25	0.80	1.68

(1) Pulsed, (see 4.5.1).

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: “JAN”, “JANTX”, “JANTXV” and "JANS".

* 1.5.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".

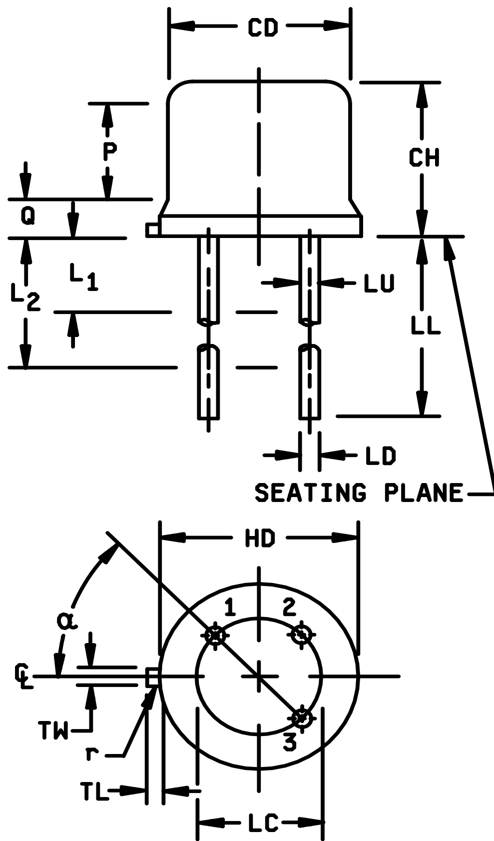
* 1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

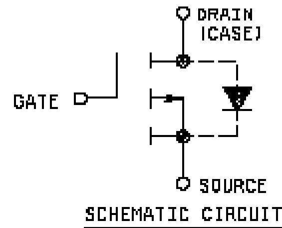
* 1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "6849" and "6851".

* 1.5.4 Suffix letters. The suffix letter "U" indicates that the transistor is a surface mount type package.

* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.

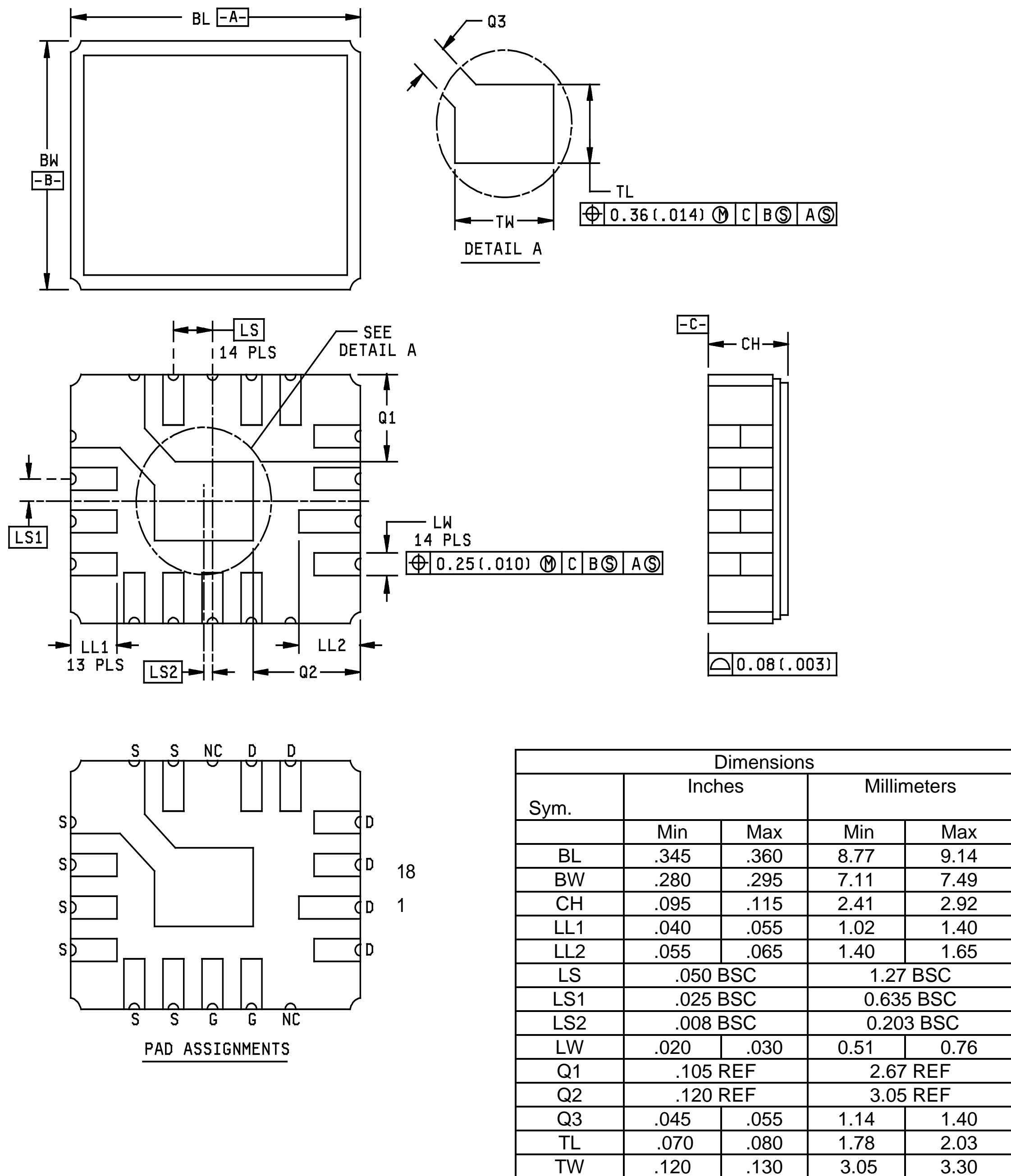


Ltr	Dimensions				
	Inches		Millimeters		Notes
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.160	.180	4.07	4.57	
HD	.335	.370	8.51	9.39	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	7, 8
LL	.500	.750	12.7	19.05	7, 8
LU	.016	.019	0.41	0.48	7, 8
L_1		.050		1.27	7, 8
L_2	.250		6.35		7, 8
P	.100		2.54		5
Q		.050		1.27	4
r		.010		0.25	9
TL	.029	.045	0.74	1.14	3
TW	.028	.034	0.72	0.86	2
α	45° TP		45° TP		6



NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Beyond radius (r) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
3. Dimension TL measured from maximum HD.
4. Outline in this zone is not controlled.
5. Dimension CD shall not vary more than .010 (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 +.001, -.000 (1.37 +0.03, -0.00 mm) below seating plane shall be within .007 (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. LU applies between L_1 and L_2. LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. Radius (r) applies to both inside corners of tab.
10. Drain is electrically connected to the case.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
12. Lead 1 = source, lead 2 = gate, lead 3 = drain.

FIGURE 1. Physical dimensions for TO-205AF (2N6849 and 2N6851).

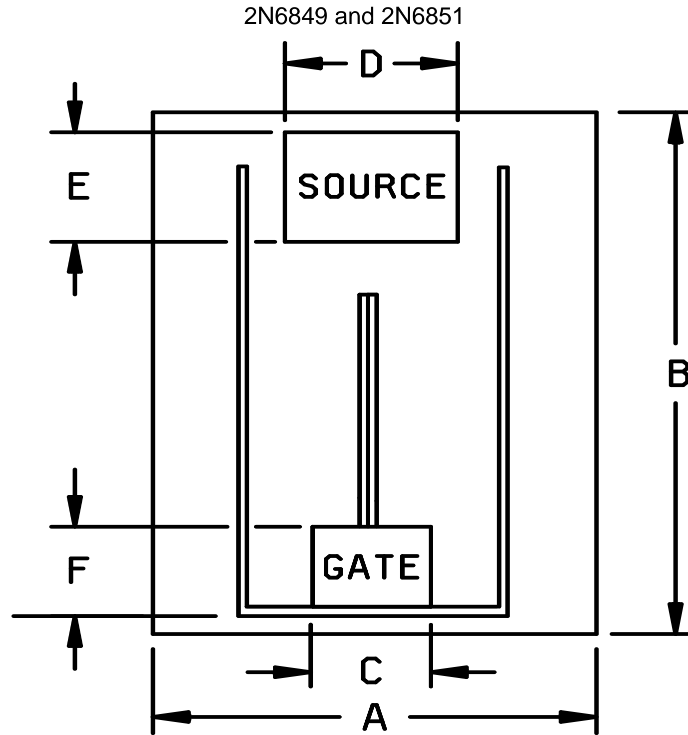


Sym.	Dimensions Inches		Millimeters	
	Min	Max	Min	Max
BL	.345	.360	8.77	9.14
BW	.280	.295	7.11	7.49
CH	.095	.115	2.41	2.92
LL1	.040	.055	1.02	1.40
LL2	.055	.065	1.40	1.65
LS	.050 BSC		1.27 BSC	
LS1	.025 BSC		0.635 BSC	
LS2	.008 BSC		0.203 BSC	
LW	.020	.030	0.51	0.76
Q1	.105 REF		2.67 REF	
Q2	.120 REF		3.05 REF	
Q3	.045	.055	1.14	1.40
TL	.070	.080	1.78	2.03
TW	.120	.130	3.05	3.30

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions for LCC (2N6849U and 2N6851U).

2N6849 and 2N6851

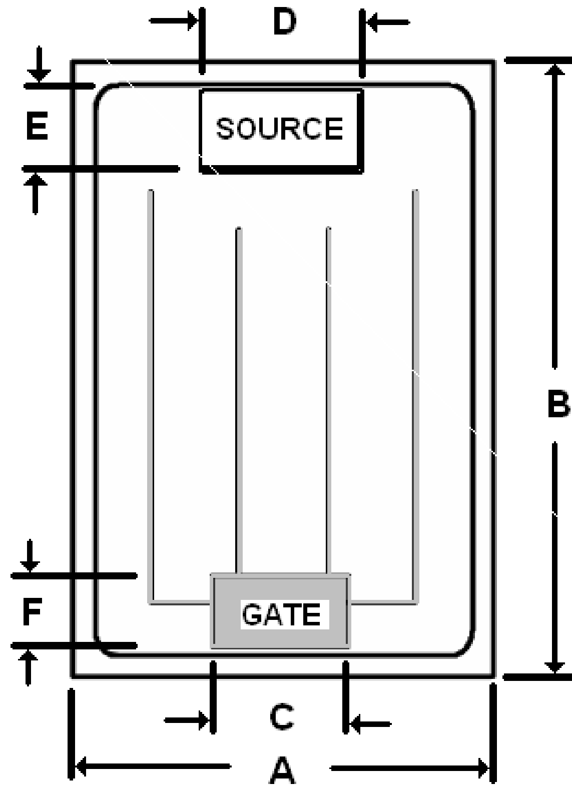


Ltr	Dimensions							
	2N6849				2N6851			
	Inches		Millimeters		Inches		Millimeters	
	Min	Max	Min	Max	Min	Max	Min	Max
A	.106	.122	2.69	3.10	.108	.124	2.74	3.15
B	.172	.188	4.37	4.78	.173	.189	4.39	4.80
C	.021	.029	0.53	0.74	.022	.030	0.56	0.76
D	.035	.043	0.89	1.09	.030	.038	0.76	0.97
E	.028	.036	0.71	0.91	.021	.029	0.53	0.74
F	.014	.022	0.36	0.56	.012	.020	0.30	0.51

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The physical characteristics of the die are: The back metals are chromium, nickel, and silver and comprise the drain. The top metal is aluminum.
4. Die thickness is .0187 inch (0.475 mm), the tolerance is ±.0050 inch (±0.13 mm).

FIGURE 3. JANHCA and JANKCA die dimensions.

2N6849



Ltr	Dimensions			
	2N6849			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.116	.120	2.95	3.05
B	.181	.185	4.60	4.70
C	.032	.034	0.81	0.86
D	.035	.037	0.89	0.94
E	.024	.026	0.61	0.66
F	.018	.019	0.46	0.48

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The physical characteristics of the die are: The back metals are chromium, nickel, and silver and comprise the drain. The top metal is aluminum.
4. Die thickness is .015 inch (0.381 mm), the tolerance is ±.0010 inch (±0.025 mm).

FIGURE 4. JANHCB die dimensions (2N6849 only).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

I_{AS} ....Rated avalanche current, nonrepetitive.
nC ....nano Coulomb.

3.4 Interface and physical dimensions. The Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1 (TO-205AF), 2 (LCC), and 3 and 4 (JANHC/JANKC die) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Internal construction. Multiple chip construction shall not be permitted.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking of country of origin may be omitted from the body of the transistor, but shall be retained on the initial container.

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

a. Devices shall be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100$ kΩ, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in paragraph 1.3, 1.4, and table I.

3.8 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I).

* 4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and table II herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 JANHC and JANKC die. Qualification shall be in accordance with MIL-PRF-19500.

* 4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTX and JANTXV levels
(3)	Gate stress test (see 4.3.2)	Gate stress test (see 4.3.2).
(3)	Method 3470 of MIL-STD-750 (see 4.3.3), optional	Method 3470 of MIL-STD-750 (see 4.3.3), optional
(3) 3c	Method 3161 of MIL-STD-750 (see 4.3.4)	Method 3161 of MIL-STD-750 (see 4.3.4)
9	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, subgroup 2 of table 1 herein.	Subgroup 2 of table 1 herein.
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(th)1}$ subgroup 2 of table I herein: ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 μA dc or ±100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(on)1}$, $V_{GS(th)1}$ subgroup 2 of table I herein:
12	Method 1042 of MIL-STD-750, test condition A, t = 240 hours	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein; ΔI_{GSSF1} = ±20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 μA dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ±20 percent of initial value. $\Delta V_{GS(th)1}$ = ±20 percent of initial value.	Subgroup 2 of table I herein; ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±25 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ±20 percent of initial value. $\Delta V_{GS(th)1}$ = ±20 percent of initial value.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and $V_{GS(th)1}$ shall be invoked.
* (3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Screening (JANHC and JANKC). Screening of die shall be in accordance with MIL-PRF-19500. As a minimum, die shall be 100-percent probed in accordance with table I, subgroup 2.

4.3.2 Gate stress test. Apply V_{GS} = ±30 V minimum for t = 250 µs minimum.

4.3.3 Unclamped inductive switching.

a. Peak current (I_D) .... Rated I_{D1}.

b. Peak gate voltage (V_{GS}) .... -10 V dc.

c. Gate to source resistor (R_{GS}).............. 25 Ω ≤ R_{GS} ≤ 200 Ω.

d. Initial case temperature (T_C)............... +25°C +10°C, -5°C.

e. Inductance (L)..................................... 100 µH ±10 percent.

f. Number of pulses to be applied .... 1 pulse minimum.

g. Pulse repetition rate............................ None.

4.3.4 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 µs max. See table II, group E, subgroup 4 herein.

* 4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

* 4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and herein.

* 4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1051	Test condition G.
B3	2075	See 3.4.2 herein.
B3	2077	Scanning electron microscope (SEM) qualification may be performed anytime prior to lot formation.
* B4	1042	Test condition D. The heating cycle shall be 1 minute minimum.
B5	1042	Accelerated steady-state operation life; test condition A; V_{DS} = rated T_A = +175°C, t = 120 hours. Read and record $V_{(BR)DSS}$ (pre and post) at 1 mA = I_D. Read and record I_{DSS1} (pre and post). Deltas for $V_{(BR)DSS}$ shall not exceed 10 percent and I_{DSS1} shall not exceed 25 µA. Accelerated steady-state gate stress; condition B, V_{GS} = rated, T_A +175°C, t = 24 hours.
B5	2037	Bond strength; test condition D.

* 4.4.2.2 Group B inspection, table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles.
* B3	1042	Test condition D. The heating cycle shall be 1 minute minimum.
B4	2075	See 3.4.2.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

Subgroup	Method	Condition
C2	2036	Test condition E; weight = 8 ounces, 3 arcs of 90 degrees (Not required for LCC).
C5	3161	See 4.5.2, $R_{\theta JC(max)}$ = 5.0°C/W.
* C6	1042	Test condition D. The heating cycle shall be 1 minute minimum.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. The thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW} (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 µs max. See table E-IX of MIL-PRF-19500, group E, subgroup 4.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.4	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source	3407	Bias condition C, V_{GS} = 0V, I_D = -1 mA dc	$V_{(BR)DSS}$			
2N6849, 2N6849U				-100		V dc
2N6851, 2N6851U				-200		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = -0.25 mA	$V_{GS(th)1}$	-2.0	-4.0	V dc
Gate current	3411	Bias condition C, V_{GS} = +20 V dc V_{DS} = 0	I_{GSSF1}		+100	nA dc
Gate current	3411	Bias condition C, V_{GS} = -20 V dc V_{DS} = 0	I_{GSSR1}		-100	nA dc
Drain current	3413	Bias condition C, V_{GS} = 0, V_{DS} = 80 percent of rated V_{DS}	I_{DSS1}		-25	μA dc
Static drain to source on-state resistance	3421	V_{GS} = -10 V dc, condition A, pulsed (see 4.5.1), I_D = rated I_{D2} (see 1.3)	$r_{DS(on)1}$			
2N6849, 2N6849U					0.30	Ω
2N6851, 2N6851U					0.80	Ω
Static drain to source on-state resistance	3421	V_{GS} = -10 V dc, condition A, pulsed (see 4.5.1), I_D = rated I_{D1}, (see 1.3)	$r_{DS(on)2}$			
2N6849, 2N6849U					0.32	Ω
2N6851, 2N6851U					0.83	Ω
* Forward voltage	4011	V_{GS} = 0, I_D = rated I_{D1}, condition A	V_{SD}			V
2N6849, 2N6849U					-4.3	V
2N6851, 2N6851U					-5.6	V

See footnote at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 3						
High temperature operation:		$T_C = T_J = +125°C$				
Gate current	3411	Bias condition C, $V_{GS} = \pm 20$ V dc, $V_{DS} = 0$	I_{GSS2}		±200	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		-0.25	mA dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = -.25 mA	$V_{GS(th)2}$	-1.0		V dc
* Static drain to source on-state resistance	3421	V_{GS} = -10 V dc, condition A, pulsed (see 4.5.1), I_D = rated I_{D2}	$r_{DS(on)3}$			
2N6849, 2N6849U					0.54	Ω
2N6851, 2N6851U					1.60	Ω
Low temperature operation:		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = -.25 mA	$V_{GS(th)3}$		-5.0	V dc
Subgroup 4						
Switching time test	3472	I_D = rated I_{D1}; V_{GS} = -10 V dc; gate drive impedance = 7.5 Ω;				
Turn-on delay time			$t_{d(on)}$			
2N6849, 2N6849U		V_{DD} = -40 V dc			60	ns
2N6851, 2N6851U		V_{DD} = -75 V dc			50	ns
Rise time			t_r			
2N6849, 2N6849U		V_{DD} = -40 V dc			140	ns
2N6851, 2N6851U		V_{DD} = -75 V dc			100	ns
Turn-off delay time			$t_{d(off)}$			
2N6849, 2N6849U		V_{DD} = -40 V dc			140	ns
2N6851, 2N6851U		V_{DD} = -75 V dc			80	ns
Fall time			t_f			
2N6849, 2N6849U		V_{DD} = -40 V dc			140	ns
2N6851, 2N6851U		V_{DD} = -75 V dc			80	ns

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

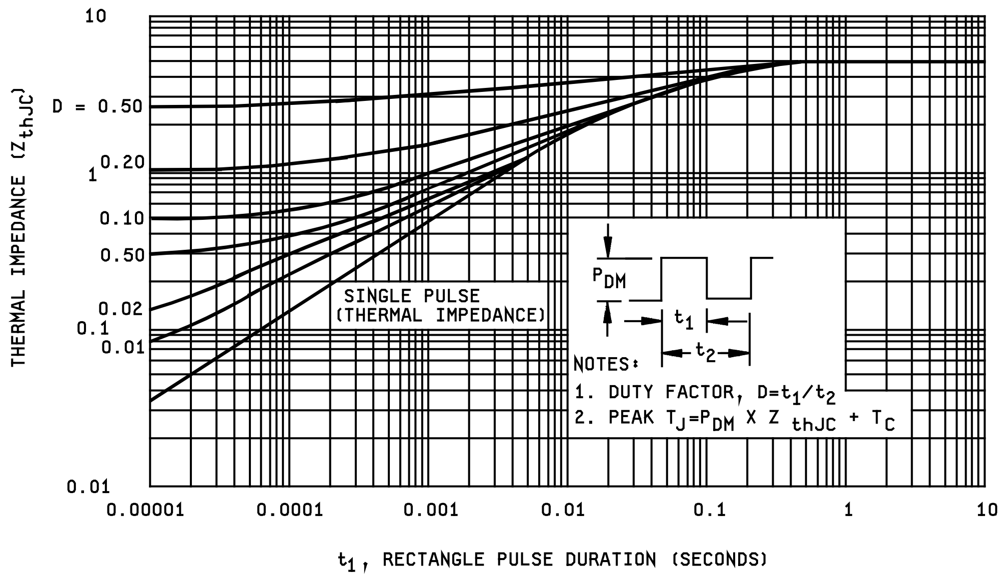
Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 5						
Single pulse unclamped inductive switching 3/	3470	See 4.3.3				
Electrical measurements		See table I, subgroup 2				
Safe operating area test (high voltage)	3474	See figure 7 t_p = 10 ms, V_{DS} = 80 percent of rated V_{DS}, V_{DS} ≤200 V dc max.				
Electrical measurements		See table I, subgroup 2				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B				
On-state gate charge			$Q_{g(on)}$			
2N6849, 2N6849U					34.8	nC
2N6851, 2N6851U					34.8	nC
Gate to source charge			Q_{gs}			
2N6849, 2N6849U					6.8	nC
2N6851, 2N6851U					6.1	nC
Gate to drain charge			Q_{gd}			
2N6849, 2N6849U					23.1	nC
2N6851, 2N6851U					20.5	nC
Reverse recovery time	3473	d_i/d_t ≤ -100 A/µs, V_{DD} ≤ -50 V,	t_{rr}			
2N6849, 2N6849U		I_F = -6.5 A			250	ns
2N6851, 2N6851U		I_F = -4.0 A			400	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ This test is required for the following end-point measurement only (not intended for 4.3, screen 9, 11, or 13): JANS, table E-VIA of MIL-PRF-19500, group B, subgroups 3 and 4; JAN, JANTX, and JANTXV, table E-VIB of MIL-PRF-19500, group B, subgroups 2 and 3; and table E-VII of MIL-PRF-19500, group C, subgroups 2 and 6, and table E-IX of MIL-PRF-19500, group E, subgroup 1.
3/ This test is optional if performed as a 100 percent screen.

TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

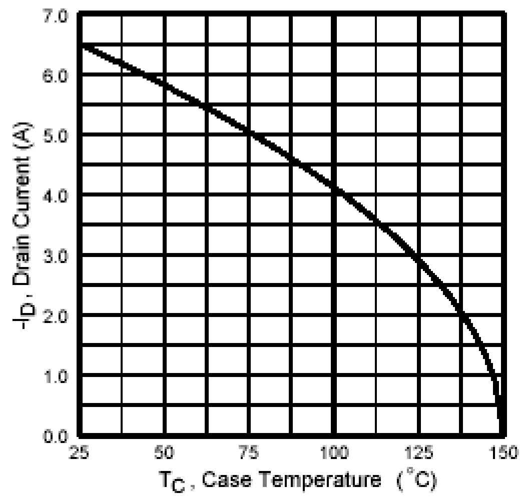
Inspection	MIL-STD-750		Qualification inspection
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycle	1051	Condition G, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2	
Subgroup 2 1/			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			
Not applicable			
Subgroup 10			
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	22 devices c = 0

1/ A separate sample for each test may be pulled.

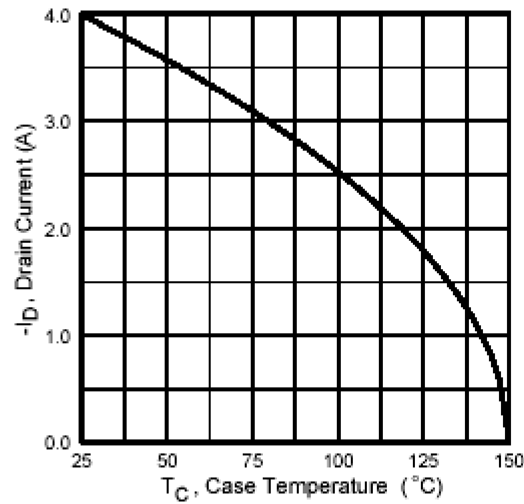


2N6849, 2N6849U, 2N6851, and 2N6851U

FIGURE 5. Normalized transient thermal impedance.



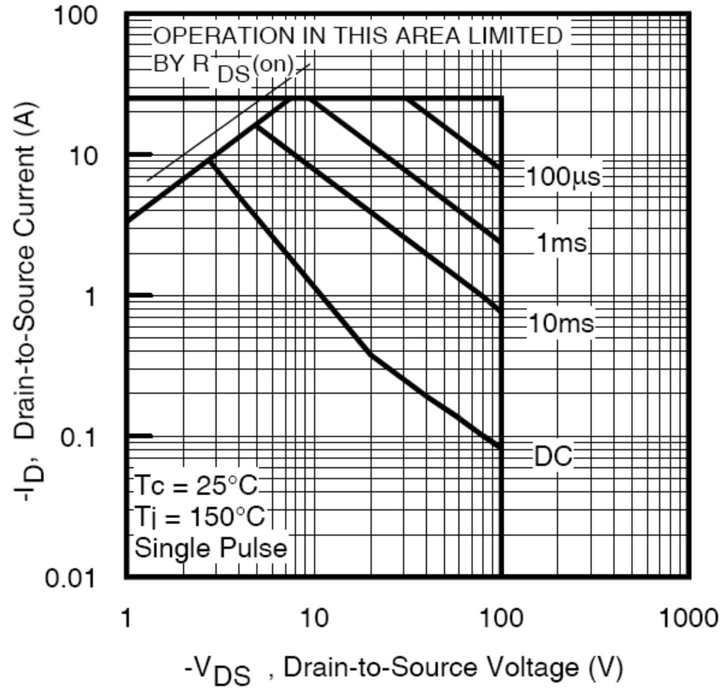
2N6849, 2N6849U



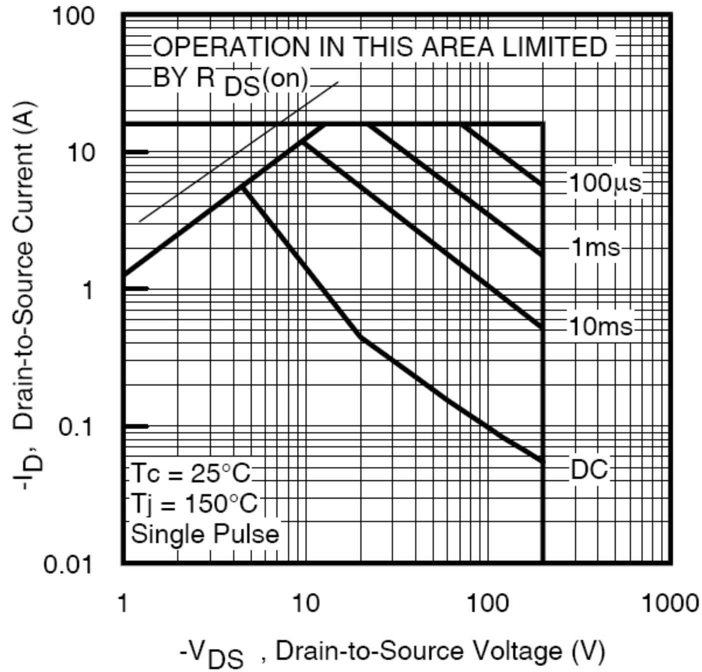
2N6851, 2N6851U

FIGURE 6. Maximum drain current versus case temperature graphs.

ACTIVE REGION - 2N6849, 2N6849U



ACTIVE REGION - 2N6851, 2N6851U



* FIGURE 7. Maximum safe operating area.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

* d. The complete Part or Identifying Number (PIN), see 1.5.

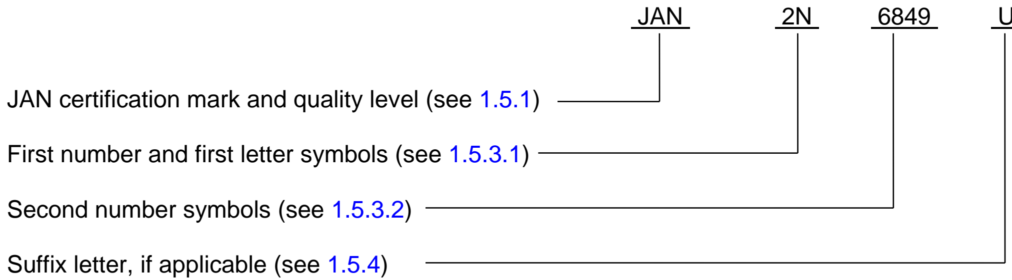
* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil .

6.4 Cross-reference and complement list. Parts from this specification may be used to replace the following commercial Part or Identifying Number (PIN's). The term PIN is equivalent to the term part number which was previously used in this specification.

Preferred types	Commercial types (1)
2N6849	IRFF9130, IRFF9131, IRFF9132, IRFF9133
2N6851	IRFF9230, IRFF9231, IRFF9232, IRFF9233
2N6849U	IRFE9130, IRFE9131, IRFE9132, IRFE9133
2N6851U	IRFE9230, IRFE9231, IRFE9232, IRFE9233

(1) Complementary devices can be found on MIL-PRF-19500/557

* 6.5 PIN construction example. The PINs for encapsulated devices are construction using the following form.



* 6.6 List of PINs.

* 6.6.1 PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN2N6849	JANTX2N6849	JANTXV2N6849	JANS2N6849
JAN2N6849U	JANTX2N6849U	JANTXV2N6849U	JANS2N6849U
JAN2N6851	JANTX2N6851	JANTXV2N6851	JANS2N6851
JAN2N6851U	JANTX2N6851U	JANTXV2N6851U	JANS2N6851U

* 6.6.2 PINs for unencapsulated devices (die). The following is a list of possible PINs for unencapsulated devices available on this specification sheet.

Quality level HC	Quality level KC
JANHCA2N6849	JANKCA2N6849
JANHCB2N6849	
JANHCA2N6851	JANKCA2N6851

6.7 Suppliers of JANC die. The qualified JANC suppliers with the applicable letter version (example JANHCA2N6849) will be identified on the QML.

JANC ordering information		
PIN	Manufacturer	
	59993	43611
2N6849	JANHCA2N6849 JANKCA2N6849	JANHCB2N6849
2N6851	JANHCA2N6851 JANKCA2N6851	

6.8 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Army - MI, SM
Navy - AS, MC
Air Force - 19, 70

Preparing activity:
DLA - CC

(Project 5961-2014-085)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.