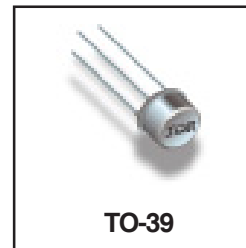


**REPETITIVE AVALANCHE AND dv/dt RATED
 HEXFET[®] TRANSISTORS
 THRU-HOLE (TO-39)**

**IRLF120
 100V, N-CHANNEL**

Product Summary

Part Number	BVDSS	R _{DS(on)}	I _D
IRLF120	100V	0.35Ω	5.3A



The Logic Level 'L' series of power MOSFETs are designed to be operated with level logic gate-to-source voltage of 5V. In addition to the well established characteristics of HEXFETs[®], they have the added advantage of providing low drive requirements to interface power loads to logic level IC's and microprocessors.

Fields of applications include: high speed power applications such as switching regulators, switching converters, motor drivers, solenoid and relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gatedrive voltage.

The HEXFET technology is the key to International Rectifier's advanced line of logic level power MOSFET transistors. The efficient geometry and unique processing of the HEXFET achieve very low on-state resistance combined with high transconductance and great device ruggedness.

Features:

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Low Drive Requirements
- Excellent Temperature Stability
- Fast Switching Speeds
- Ease of Paralleling
- Hermetically Sealed
- Light Weight

Absolute Maximum Ratings

	Parameter		Units
I _D @ V _{GS} = 5.0V, T _C = 25°C	Continuous Drain Current	5.3	A
I _D @ V _{GS} = 5.0V, T _C = 100°C	Continuous Drain Current	3.4	
I _{DM}	Pulsed Drain Current ①	21	
P _D @ T _C = 25°C	Max. Power Dissipation	20	W
	Linear Derating Factor	0.16	W/°C
V _{GS}	Gate-to-Source Voltage	±10	V
EAS	Single Pulse Avalanche Energy ②	120	mJ
I _{AR}	Avalanche Current ①	5.3	A
E _{AR}	Repetitive Avalanche Energy ①	2.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T _J	Operating Junction	-55 to 150	°C
T _{STG}	Storage Temperature Range		
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	0.98 (typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.13	—	V/°C	Reference to 25°C, I _D = 250μA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.35	Ω	V _{GS} = 5.0V, I _D = 3.4A ④
		—	—	0.42		V _{GS} = 4.0V, I _D = 2.7A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	3.1	—	—	S	V _{DS} = 50V, I _{DS} = 3.4A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	250	μA	V _{DS} = 100V, V _{GS} = 0V
		—	—	1000		V _{DS} = 80V V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -10V
Q _g	Total Gate Charge	—	—	13	nC	V _{GS} = 5.0V, I _D = 5.3A V _{DS} = 80V
Q _{gs}	Gate-to-Source Charge	—	—	2.4		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	7.1		
t _{d(on)}	Turn-On Delay Time	—	—	13	ns	V _{DD} = 50V, I _D = 5.3A, V _{GS} = 5.0V, R _G = 18Ω
t _r	Rise Time	—	—	73		
t _{d(off)}	Turn-Off Delay Time	—	—	41		
t _f	Fall Time	—	—	27		
LS + LD	Total Inductance	—	7.0	—	nH	Measured from drain lead (6mm/ 0.25in. from package) to source lead (6mm/0.25in. from package)
C _{iss}	Input Capacitance	—	480	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	150	—		
C _{rss}	Reverse Transfer Capacitance	—	30	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	5.3	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	21		
V _{SD}	Diode Forward Voltage	—	—	2.5	V	T _j = 25°C, I _S = 5.3A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	220	ns	T _j = 25°C, I _F = 5.3A, di/dt ≤ 100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	1.1	μC	V _{DD} ≤ 50V ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	6.25	°C/W	Typical socket mount.
R _{thJA}	Junction-to-Ambient	—	—	175		

Note: Corresponding Spice and Saber models are available on International Rectifier website.

For footnotes, refer to the last page

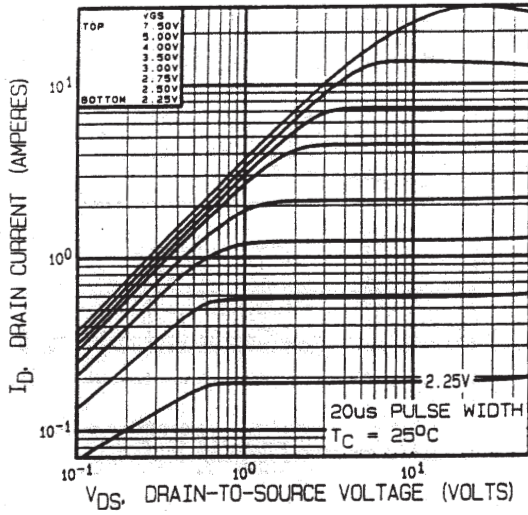


Fig1. Typical Output Characteristics

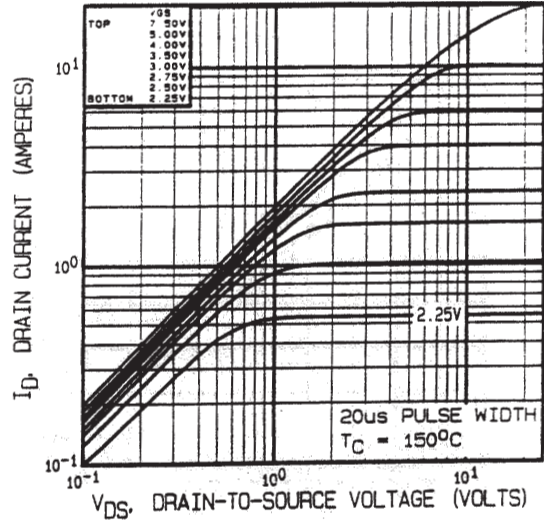


Fig2. Typical Output Characteristics

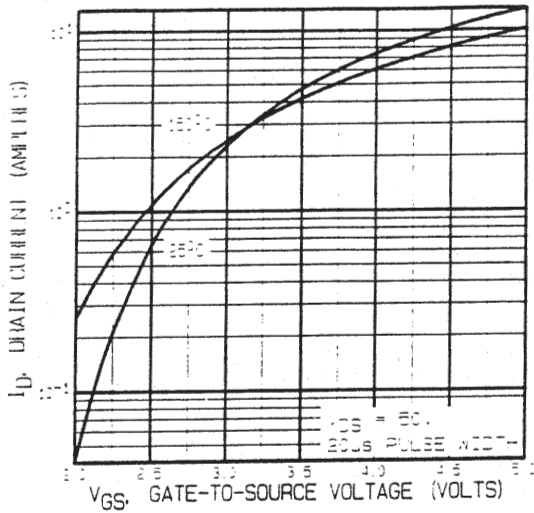


Fig3. Typical Transfer Characteristics

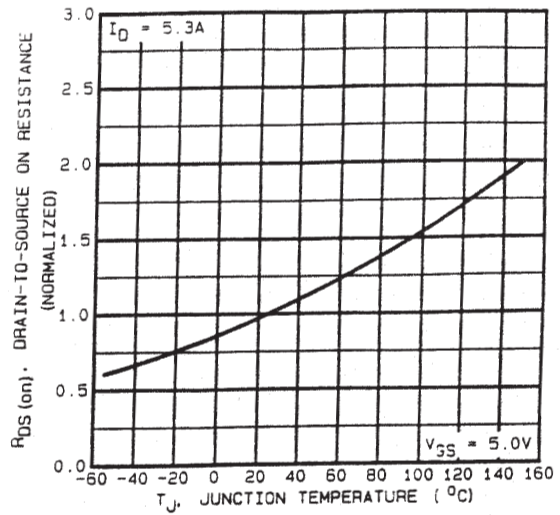


Fig4. Normalized On-Resistance Vs. Temperature

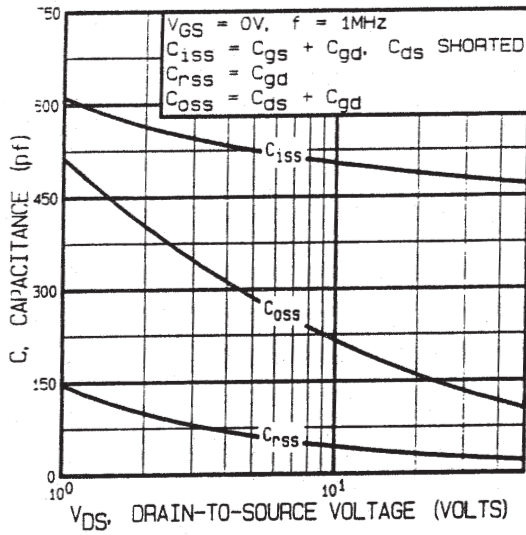


Fig5. Typical Capacitance Vs. Drain-to-Source Voltage

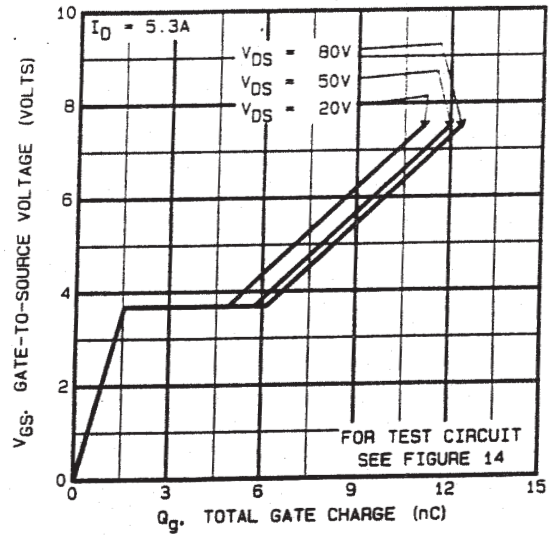


Fig6. Typical Gate Charge Vs. Gate-to-Source Voltage

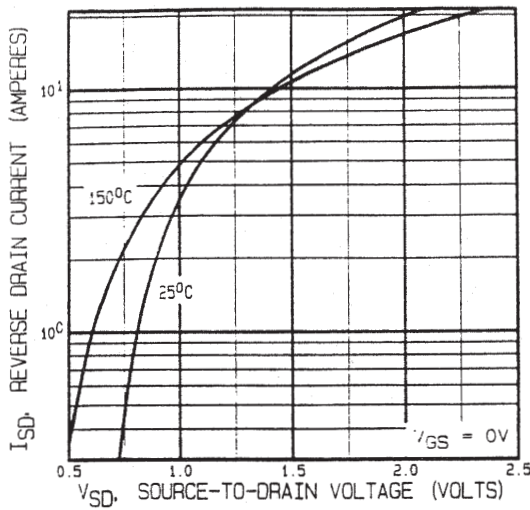


Fig7. Typical Source-Drain Diode Forward Voltage

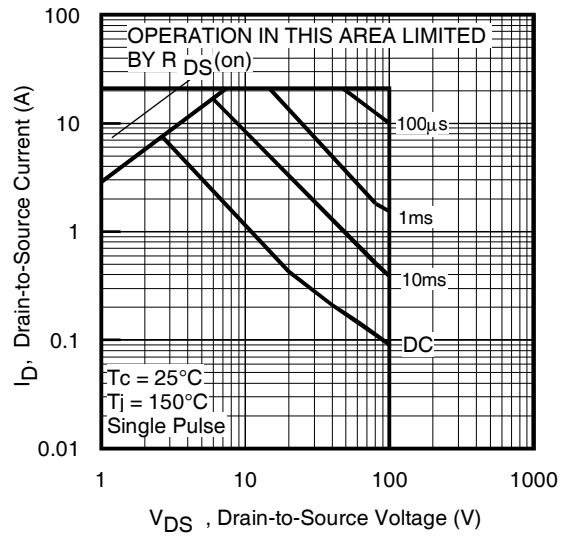


Fig8. Maximum Safe Operating Area

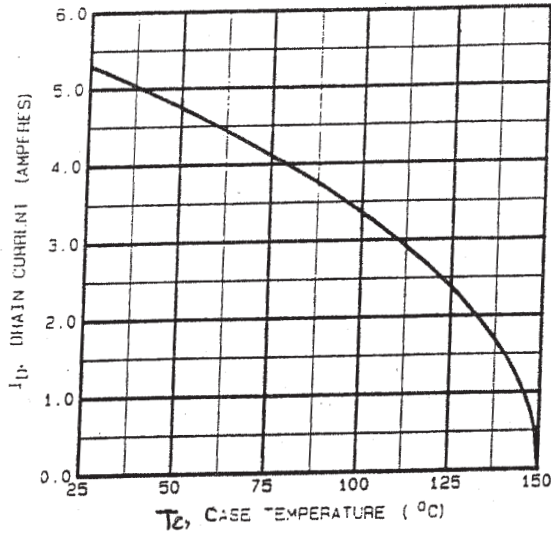


Fig9. Maximum Drain Current Vs. Case Temperature

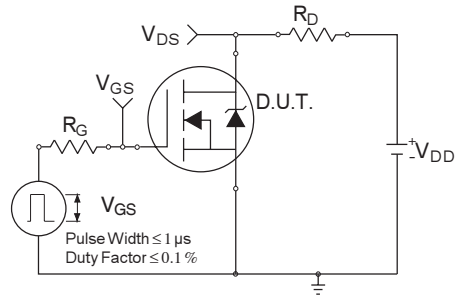


Fig 10a. Switching Time Test Circuit

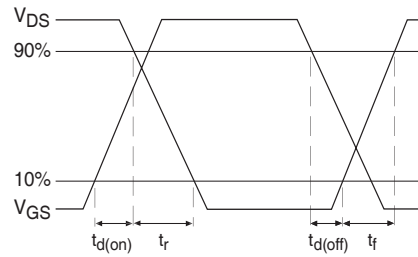


Fig 10b. Switching Time Waveforms

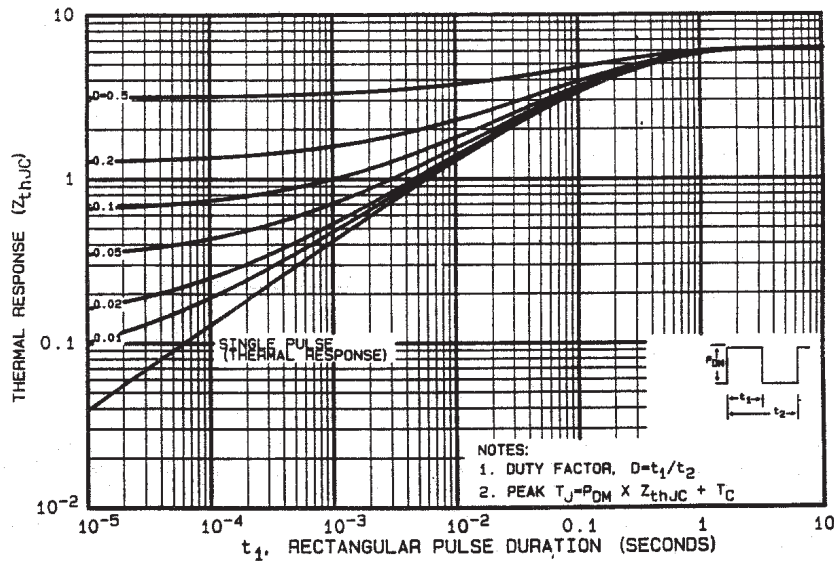


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

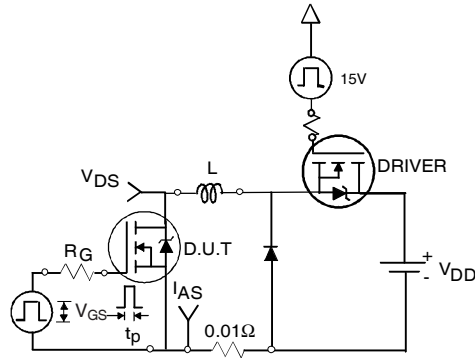


Fig 12a. Unclamped Inductive Test Circuit

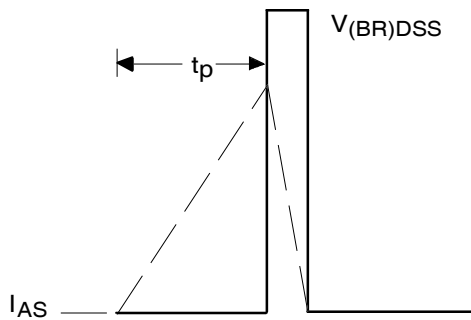


Fig 12b. Unclamped Inductive Waveforms

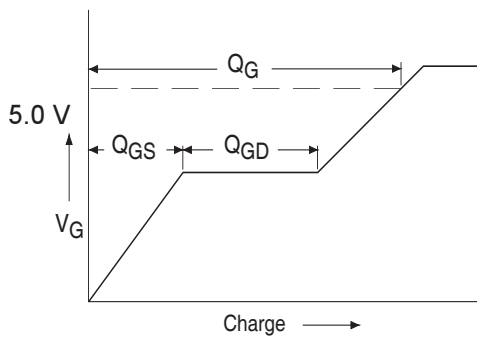


Fig 13a. Basic Gate Charge Waveform

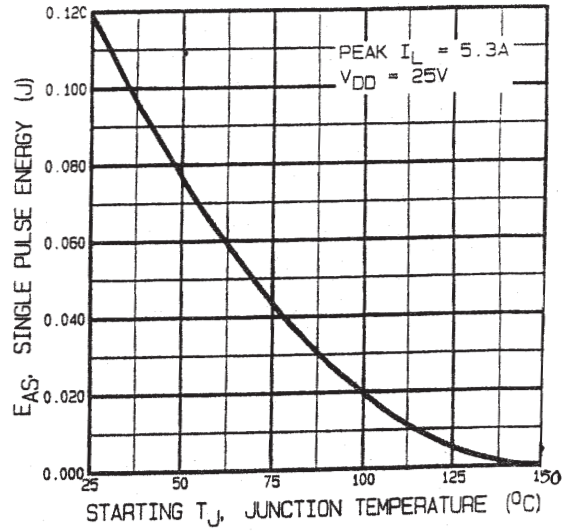


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

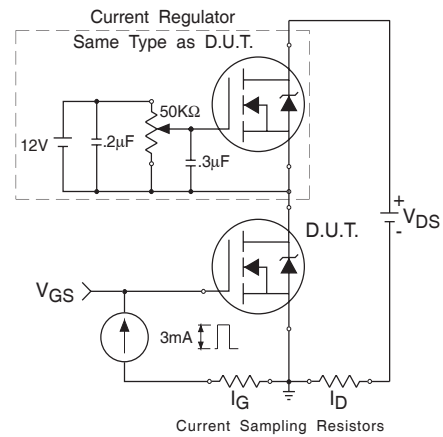
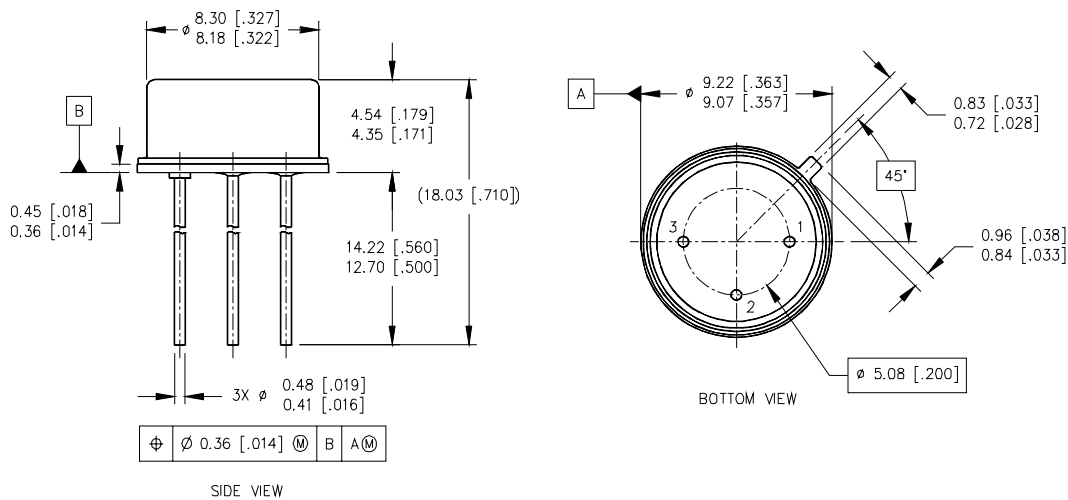


Fig 13b. Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25\text{ V}$, Starting $T_J = 25^\circ\text{C}$, $L = 6.1\text{mH}$
 Peak $I_{AS} = 5.3\text{A}$, $V_{GS} = 5.0\text{V}$, $R_G = 25\Omega$
- ③ $I_{SD} \leq 5.3\text{A}$, $di/dt \leq 110\text{A}/\mu\text{s}$,
 $V_{DD} \leq 100\text{V}$, $T_J \leq 150^\circ\text{C}$
 Suggested $R_G = 18\ \Omega$
- ④ Pulse width $\leq 300\ \mu\text{s}$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions —TO-205AF (TO-39)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME 14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-205AF (TO-39).

LEGEND

- 1- SOURCE
- 2- GATE
- 3- DRAIN