PD - 93955A

International
IOR Rectifier

LOGIC LEVEL HEXFET® POWER MOSFET SURFACE MOUNT (SMD-0.5)

IRL5NJ024
55V, N-CHANNEL

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRL5NJ024	55V	0.06Ω	17A

SMD-0.5

Fifth Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon unit area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

These devices are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits.

Features:

- Logic Level Gate Drive
- Low $R_{DS(on)}$
- Avalanche Energy Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Light Weight

Absolute Maximum Ratings

	Parameter		Units
I_D @ V_{GS} = 10V, T_C = 25°C	Continuous Drain Current	17	A
I_D @ V_{GS} = 10V, T_C = 100°C	Continuous Drain Current	11	
I_{DM}	Pulsed Drain Current ①	68	
P_D @ T_C = 25°C	Max. Power Dissipation	35	W
	Linear Derating Factor	0.28	W/°C
V_{GS}	Gate-to-Source Voltage	±16	V
E_{AS}	Single Pulse Avalanche Energy ②	56	mJ
I_{AR}	Avalanche Current ①	11	A
E_{AR}	Repetitive Avalanche Energy ①	3.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.3	V/ns
T_J	Operating Junction	-55 to 150	°C
T_{STG}	Storage Temperature Range		
	Package Mounting Surface Temperature	300 (for 5 s)	
	Weight	2.6	g

For footnotes refer to the last page

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.057	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.060	Ω	V_{GS} = 10V, I_D = 11A ④
		—	—	0.075		V_{GS} = 5.0V, I_D = 11A ④
		—	—	0.105		V_{GS} = 4.0V, I_D = 9.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	6.5	—	—	S	V_{DS} = 25V, I_D = 11 A
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -16V
Q_g	Total Gate Charge	—	—	15	nC	I_D = 11A
Q_{gs}	Gate-to-Source Charge	—	—	3.7		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	8.5		V_{GS} = 5.0V
$t_{d(on)}$	Turn-On Delay Time	—	—	11	ns	V_{DD} = 28V
t_r	Rise Time	—	—	133		I_D = 11A
$t_{d(off)}$	Turn-Off Delay Time	—	—	35		R_G = 12 Ω
t_f	Fall Time	—	—	66		V_{GS} = 5.0V
$L_S + L_D$	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitanc	—	514	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	—	137	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	51	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	17	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	68		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_j = 25°C, I_S = 11A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	90	nS	T_j = 25°C, I_F = 11A, di/dt ≤ 100A/µs
Q_{RR}	Reverse Recovery Charge	—	—	200	nC	V_{DD} ≤ 25V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	3.57	°C/W	

Note: Corresponding Spice and Saber models are available on the G&S Website.
For footnotes refer to the last page

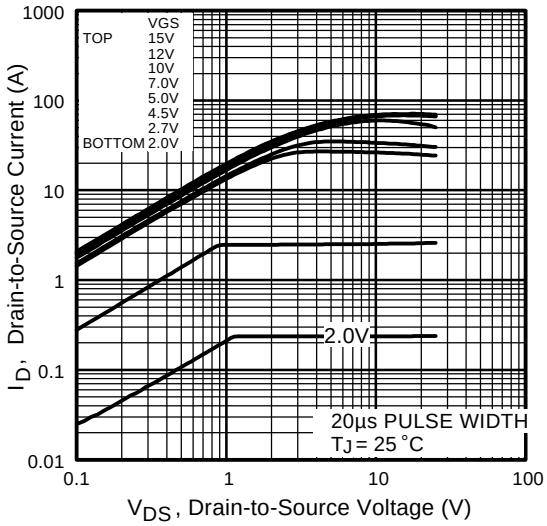


Fig 1. Typical Output Characteristics

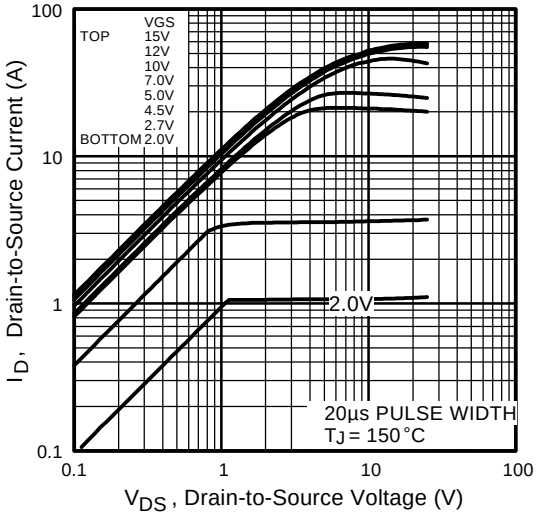


Fig 2. Typical Output Characteristics

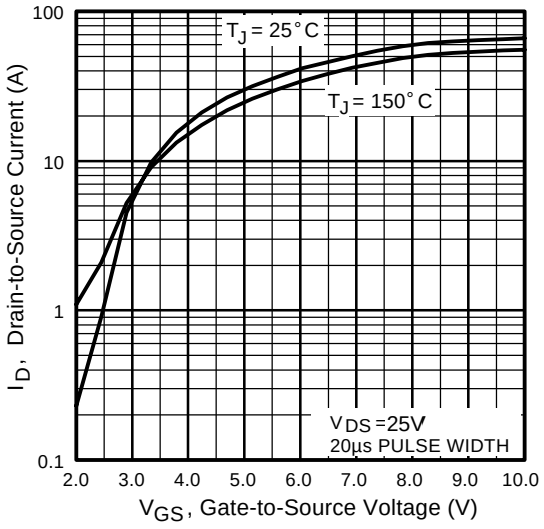


Fig 3. Typical Transfer Characteristics

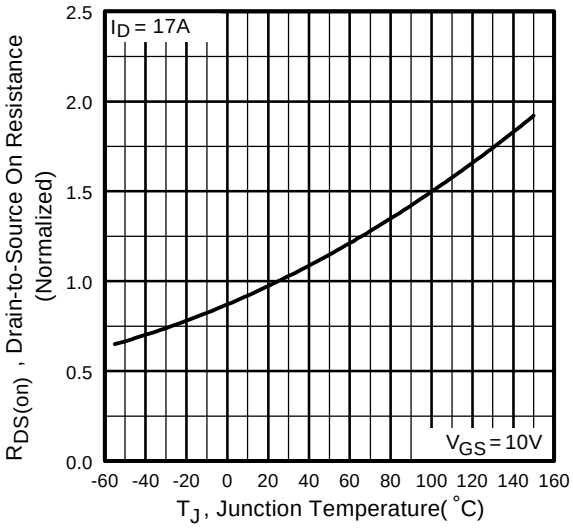


Fig 4. Normalized On-Resistance
Vs. Temperature

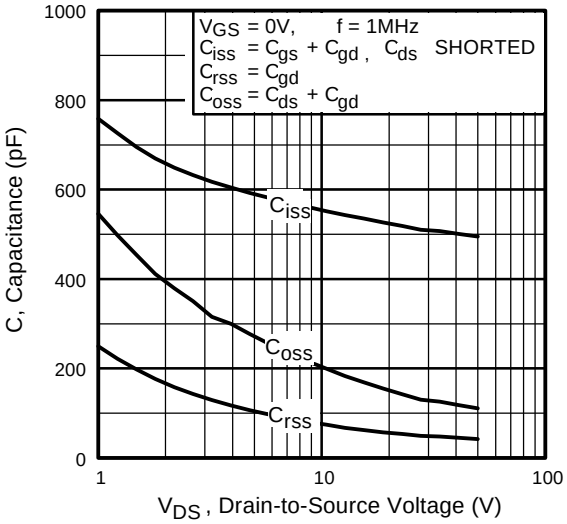


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

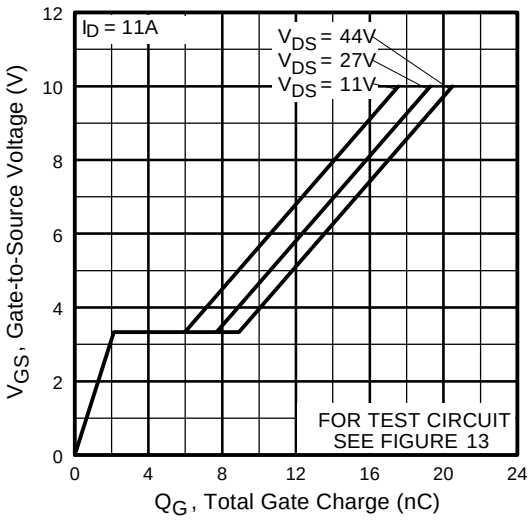


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

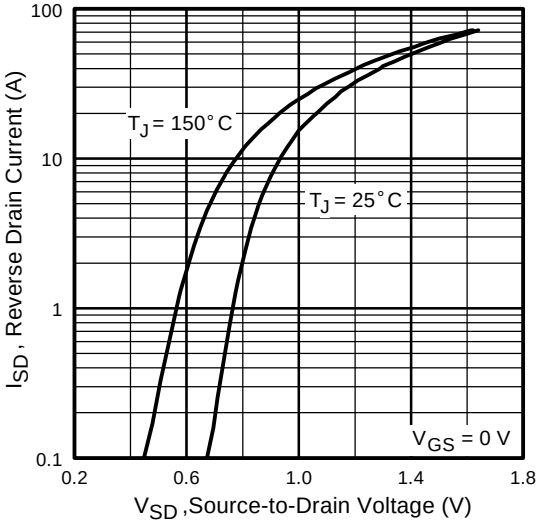


Fig 7. Typical Source-Drain Diode Forward Voltage

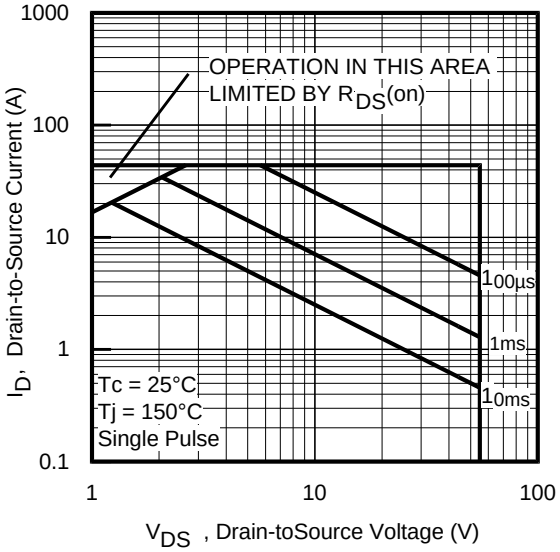


Fig 8. Maximum Safe Operating Area

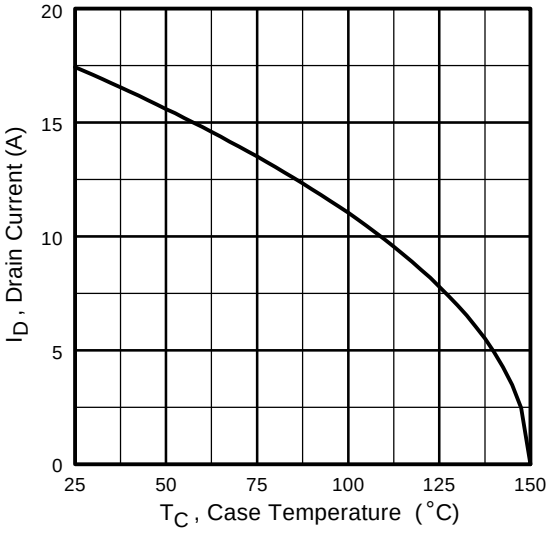


Fig 9. Maximum Drain Current Vs. Case Temperature

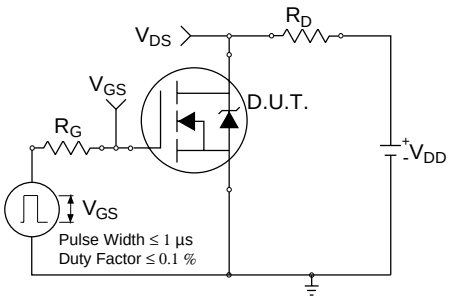


Fig 10a. Switching Time Test Circuit

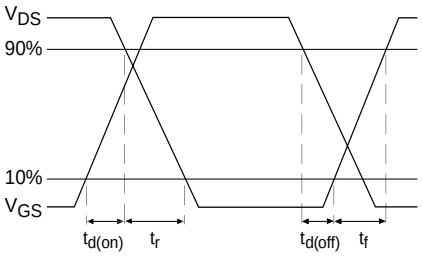


Fig 10b. Switching Time Waveforms

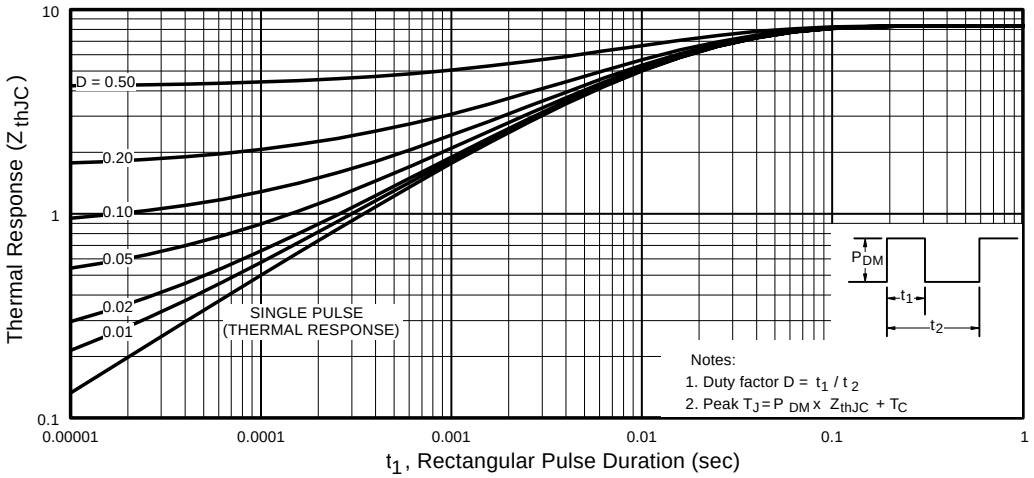


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

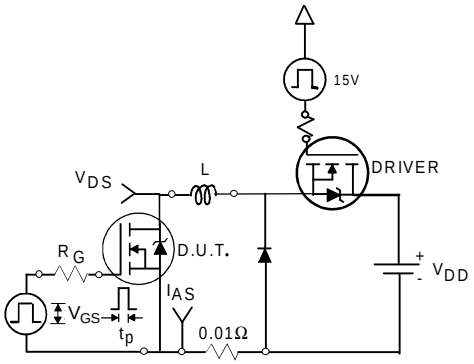


Fig 12a. Unclamped Inductive Test Circuit

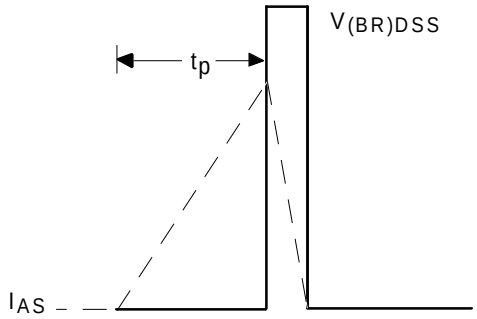


Fig 12b. Unclamped Inductive Waveforms

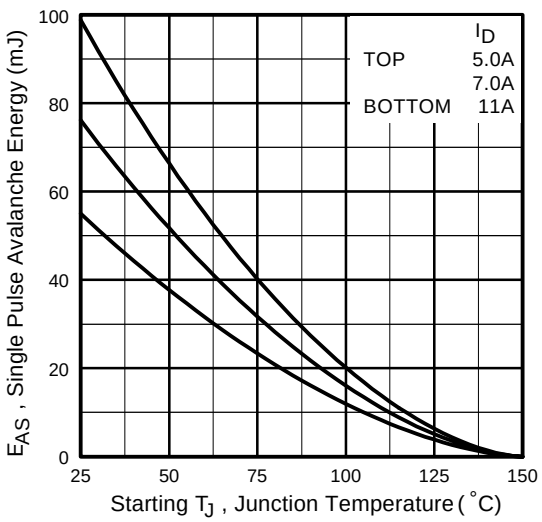


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

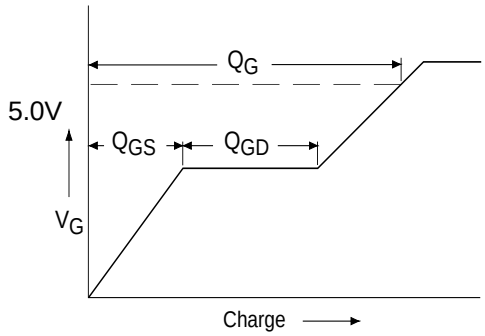


Fig 13a. Basic Gate Charge Waveform

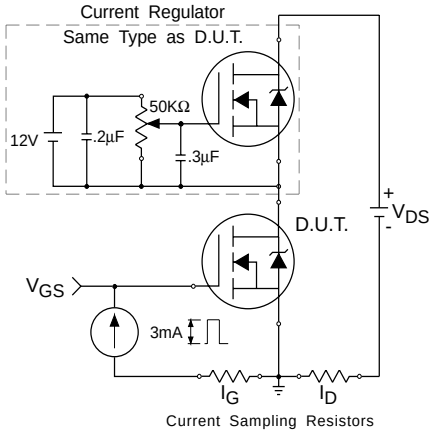
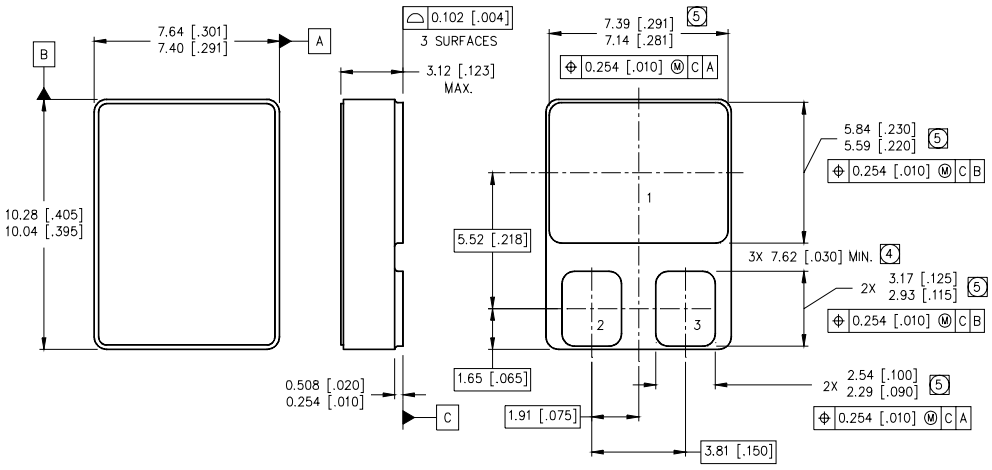


Fig 13b. Gate Charge Test Circuit

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.
② V_{DD} = 25 V, Starting T_J = 25°C, L=0.9mH Peak I_{AS} =11A, V_{GS} = 5.0 V, R_G= 25Ω
③ I_{SD} ≤ 11A, di/dt ≤ 230 A/μs, V_{DD} ≤ 55V, T_J ≤ 150°C
④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

Case Outline and Dimensions — SMD-0.5



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. DIMENSION INCLUDES METALLIZATION FLASH.
5. DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS
1 = DRAIN
2 = GATE
3 = SOURCE

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