M-MOS Semiconductor Hong Kong Limited

N-Channel Enhancement-Mode MOSFET

V_{DS}= 25V

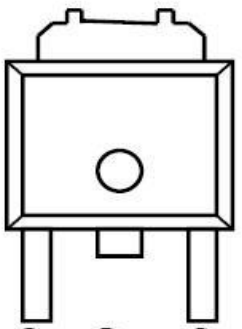
$R_{DS(ON)}$, V_{gs}@10V, I_{ds}@30A = 9mΩ

$R_{DS(ON)}$, V_{gs}@4.5V, I_{ds}@30A = 13mΩ

Features

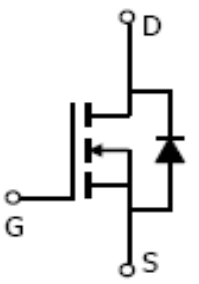
Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance
Fully Characterized Avalanche Voltage and Current

TO-252 (D-PAK)



Top View

Internal Schematic Diagram



N-Channel MOSFET

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	25	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current		I_D	35	A
Pulsed Drain Current [1)]		I_{DM}	120	
Maximum Power Dissipation	TA = 25°C	P_D	56	W
	TA = 75°C		23	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Avalanche Energy with Single Pulse		EAS	150	mJ
Junction-to-Case Thermal Resistance		$R_{\theta JC}$	2.7	°C/W
Junction-to-Ambient Thermal Resistance (PCB mounted) [2)]		$R_{\theta JA}$	50	

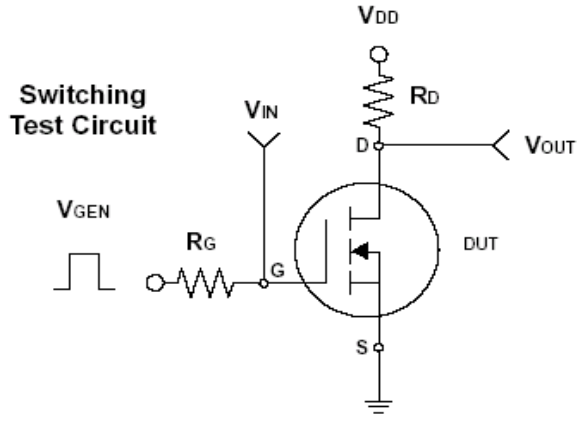
Note: 1. Repetitive Rating: Pulse width limited by the maximum junction temperature
2. 1-in^2 2oz Cu PCB board

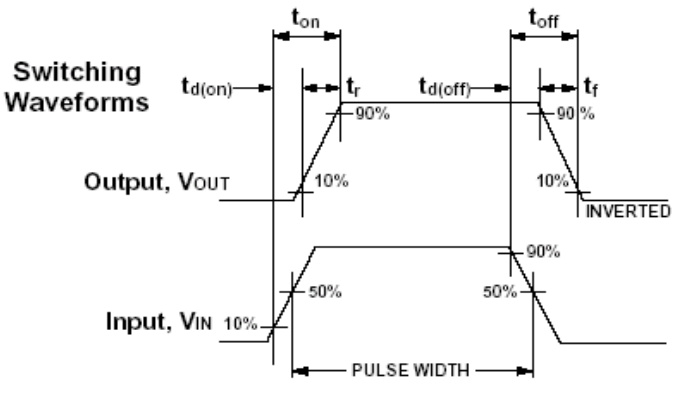
ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250uA	25			V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 30A		6.8	9.0	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 30A		9.3	13.0	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	1	1.9	3	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25V, V_{GS} = 0V			1	uA
Gate Body Leakage	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
Dynamic[3)]						
Total Gate Charge	Q_g	V_{DS} = 15V, I_D = 20A V_{GS} = 5V		10.26		nC
Gate-Source Charge	Q_{gs}			3.76		
Gate-Drain Charge	Q_{gd}			3.58		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15V, R_G = 6Ω I_D = 1A, V_{GS} = 10V		15.44		ns
Turn-On Rise Time	t_r			4.16		
Turn-Off Delay Time	$t_{d(off)}$			34.72		
Turn-Off Fall Time	t_f			5.08		
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0V f = 1.0 MHz		1176.14		pF
Output Capacitance	C_{oss}			277.66		
Reverse Transfer Capacitance	C_{rss}			142.5		
Source-Drain Diode						
Max. Diode Forward Current	I_S				20	A
Diode Forward Voltage	V_{SD}	I_S = 20A, V_{GS} = 0V			1.5	V

Note: Pulse test: pulse width <= 300us, duty cycle<= 2%

3. Guaranteed by design; not subject to production testing





Typical Characteristics Curves (Ta=25°C, unless otherwise noted)

Fig.1 Output Characteristic

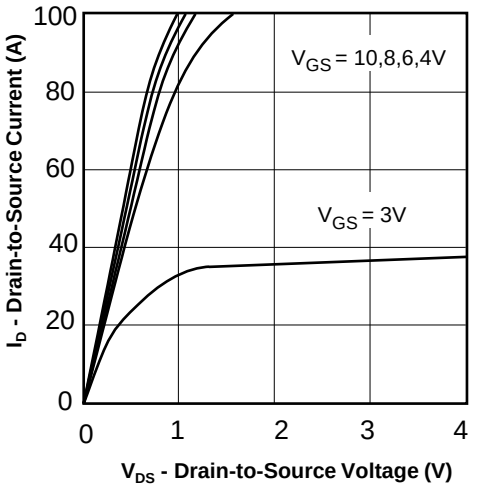


Fig.2 Transfer Characteristics

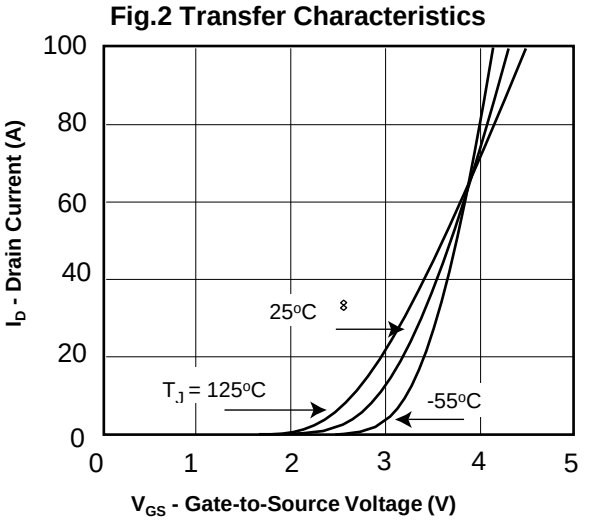


Fig.3 On-Resistance Variation with Temperature

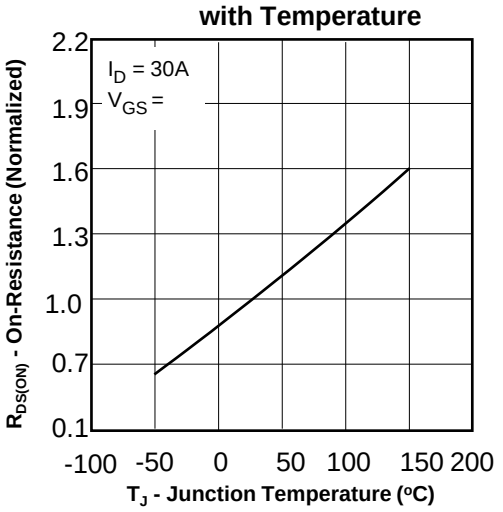


Fig.4 Body Diode Forward Voltage Variation with Source Current

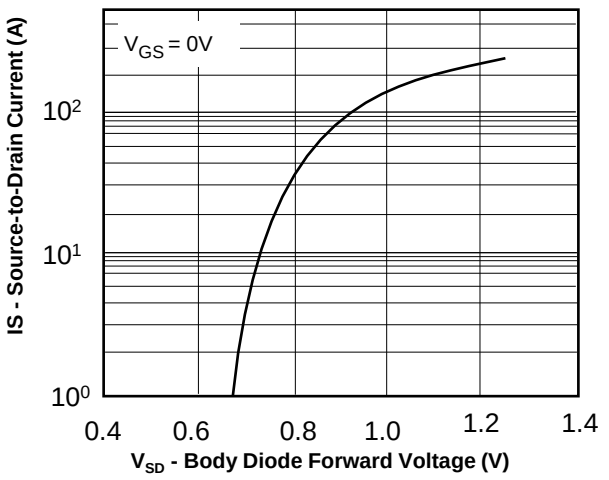


Fig.5 Gate Threshold Variation with Temperature

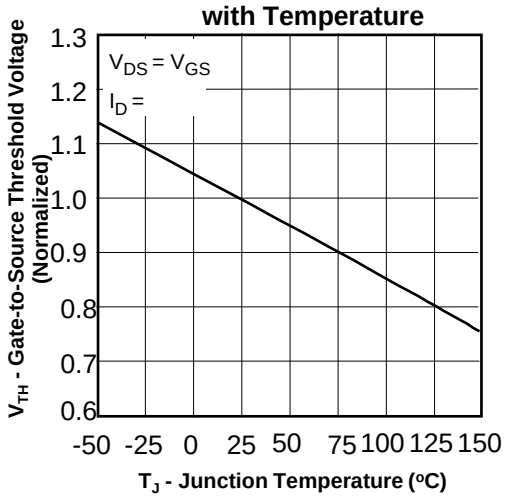
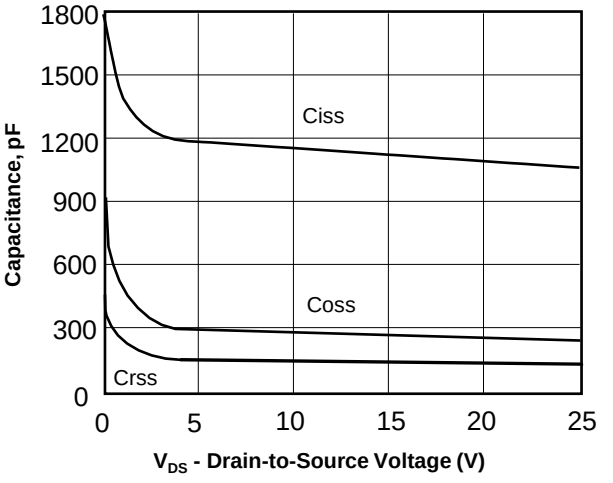


Fig.6 Capacitance



Typical Characteristics Curves (Ta=25°C, unless otherwise noted)

Fig. 7 Gate Charge Waveform

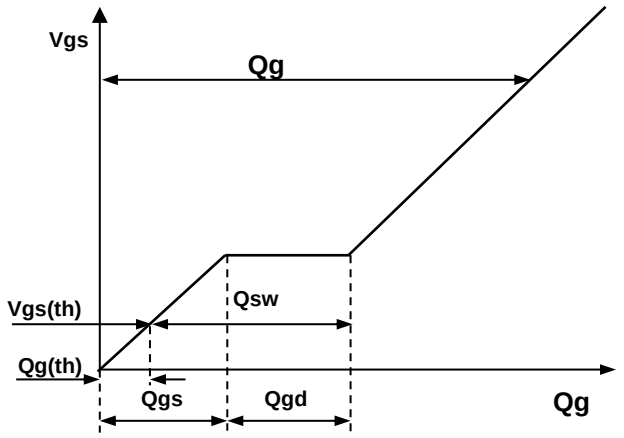


Fig. 8 Gate Charge

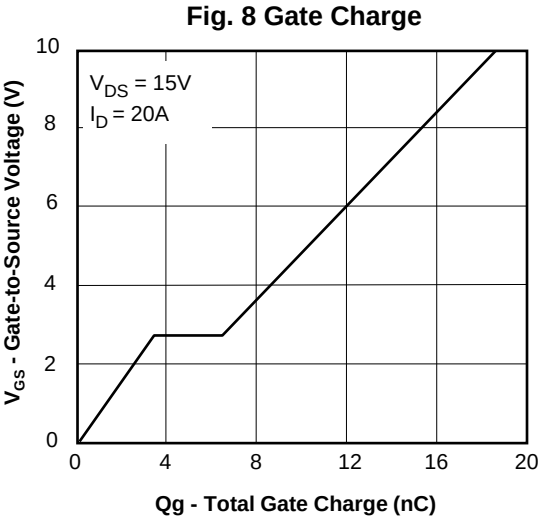


Fig. 9 Maximum Safe Operating Area

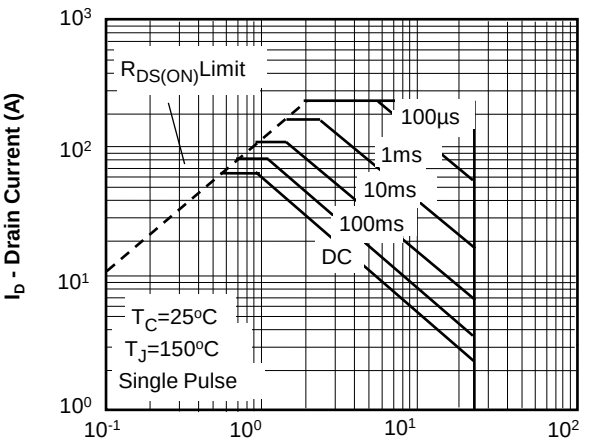
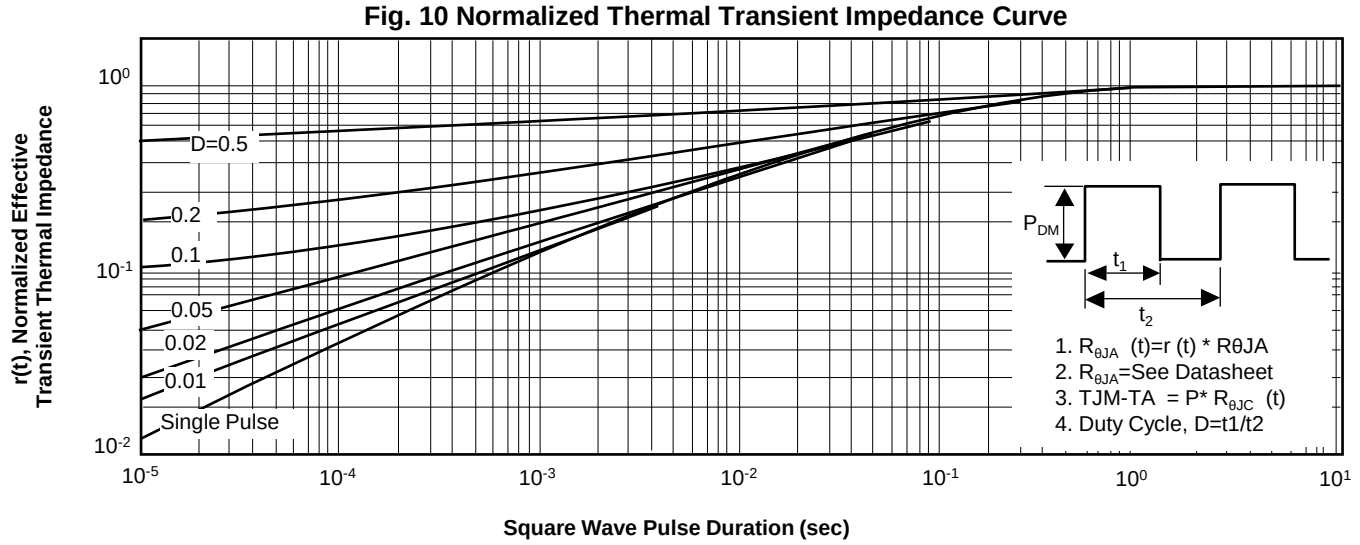


Fig. 10 Normalized Thermal Transient Impedance Curve

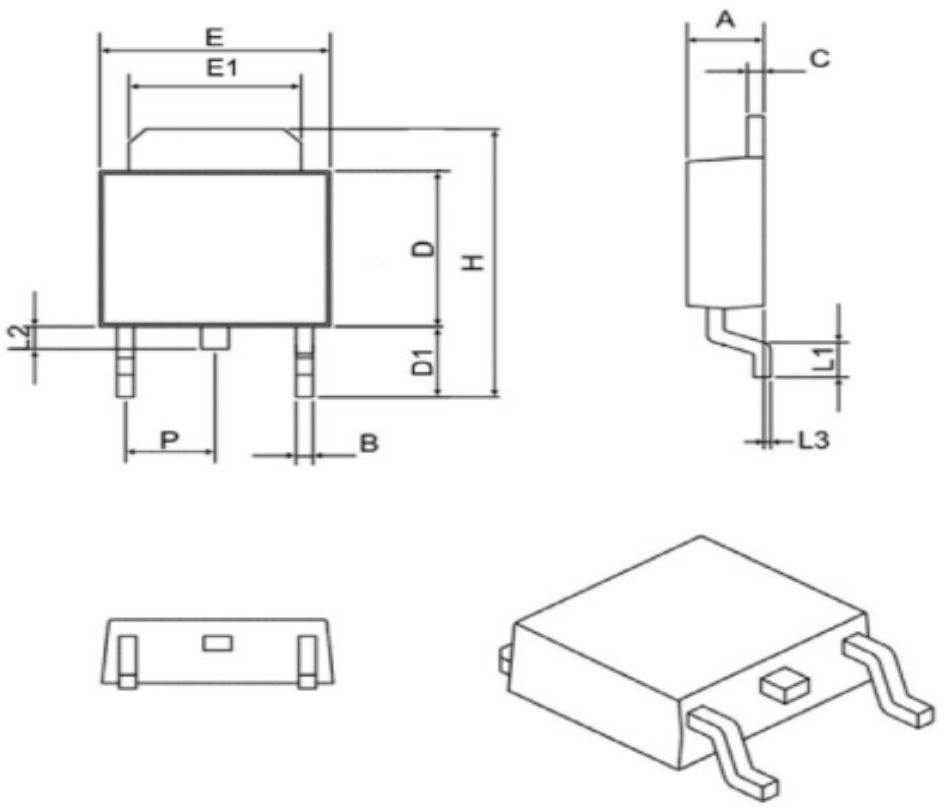


Notice

1. Specification of the products displayed herein are subject to change without notice. Continuous development may necessitate changes in technical data without notice. M-MOS Semiconductor Sdn. Bhd. or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TO-252 Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	