International
IOR Rectifier

# RADIATION HARDENED POWER MOSFET THRU-HOLE (T0-204AA/AE)

# IRH7130
## 100V, N-CHANNEL
**RAD Hard™ HEXFET® TECHNOLOGY**

### Product Summary

| Part Number | Radiation Level | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| IRH7130 | 100K Rads (Si) | 0.18Ω | 14A |
| IRH3130 | 300K Rads (Si) | 0.18Ω | 14A |
| IRH4130 | 600K Rads (Si) | 0.18Ω | 14A |
| IRH8130 | 1000K Rads (Si) | 0.18Ω | 14A |


TO-204AA

International Rectifier's RADHard HEXFET® technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low Rdson and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

### Features:
- Single Event Effect (SEE) Hardened
- Low $R_{DS(on)}$
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Package
- Light Weight

## Absolute Maximum Ratings — Pre-Irradiation

| | Parameter | | Units |
|---|---|---|---|
| $I_D$ @ $V_{GS}$ = 12V, $T_C$ = 25°C | Continuous Drain Current | 14 | A |
| $I_D$ @ $V_{GS}$ = 12V, $T_C$ = 100°C | Continuous Drain Current | 9.0 | |
| $I_{DM}$ | Pulsed Drain Current ① | 56 | |
| $P_D$ @ $T_C$ = 25°C | Max. Power Dissipation | 75 | W |
| | Linear Derating Factor | 0.60 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 160 | mJ |
| $I_{AR}$ | Avalanche Current ① | 14 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 7.5 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 5.5 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction<br>Storage Temperature Range | -55 to 150 | °C |
| | Lead Temperature | 300 ( 0.063 in.(1.6mm) from case for 10s) | |
| | Weight | 11.5 (Typical ) | g |

For footnotes refer to the last page

## Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 100 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 1.0mA |
| $\Delta BV_{DSS}/\Delta T_J$ | Temperature Coefficient of Breakdown Voltage | — | 0.12 | — | V/°C | Reference to 25°C, $I_D$ = 1.0mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-State Resistance | — | — | 0.18 | Ω | $V_{GS}$ = 12V, $I_D$ =9.0A ④ |
| | | — | — | 0.20 | | $V_{GS}$ = 12V, $I_D$ = 14A |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 1.0mA |
| $g_{fs}$ | Forward Transconductance | 3.3 | — | — | S (℧) | $V_{DS}$ > 15V, $I_{DS}$ = 9.0A ④ |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | — | — | 25 | µA | $V_{DS}$= 80V ,$V_{GS}$=0V |
| | | — | — | 250 | | $V_{DS}$ = 80V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Leakage Forward | — | — | 100 | nA | $V_{GS}$ = 20V |
| $I_{GSS}$ | Gate-to-Source Leakage Reverse | — | — | -100 | | $V_{GS}$ = -20V |
| $Q_g$ | Total Gate Charge | — | — | 45 | nC | $V_{GS}$ =12V, $I_D$ =14A $V_{DS}$ = 50V |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 11 | | |
| $Q_{gd}$ | Gate-to-Drain ('Miller') Charge | — | — | 17 | | |
| $t_{d(on)}$ | Turn-On Delay Time | — | — | 30 | ns | $V_{DD}$ = 50V, $I_D$ =14A $V_{GS}$ =12V, $R_G$ = 7.5Ω |
| $t_r$ | Rise Time | — | — | 120 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | — | — | 49 | | |
| $t_f$ | Fall Time | — | — | 64 | | |
| $L_S + L_D$ | Total Inductance | — | 10 | — | nH | Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad |
| $C_{iss}$ | Input Capacitance | — | 1100 | — | pF | $V_{GS}$ = 0V, $V_{DS}$ = 25V f = 1.0MHz |
| $C_{oss}$ | Output Capacitance | — | 310 | — | | |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 55 | — | | |

## Source-Drain Diode Ratings and Characteristics

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 14 | A | |
| $I_{SM}$ | Pulse Source Current (Body Diode) ① | — | — | 56 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.8 | V | $T_j$ = 25°C, $I_S$ = 14A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | — | 370 | nS | $T_j$ = 25°C, $I_F$ = 14A, di/dt ≤ 100A/µs $V_{DD}$ ≤ 50V ④ |
| $Q_{RR}$ | Reverse Recovery Charge | — | — | 3.5 | µC | |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$. | | | | |

## Thermal Resistance

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $R_{thJC}$ | Junction-to-Case | — | — | 1.67 | °C/W | |
| $R_{thJA}$ | Junction-to-Ambient | — | — | 30 | | |
| $R_{thCS}$ | Case-to-Sink | — | 0.12 | — | | Typical socket mount |

**Note: Corresponding Spice and Saber models are available on the G&S Website.**

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

### Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

| | Parameter | 100K Rads(Si)[1] | | 300 - 1000K Rads (Si)[2] | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 100 | — | 100 | — | V | $V_{GS}$ = 0V, $I_D$ = 1.0mA |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | 4.0 | 1.25 | 4.5 | | $V_{GS}$ = $V_{DS}$, $I_D$ = 1.0mA |
| $I_{GSS}$ | Gate-to-Source Leakage Forward | — | 100 | — | 100 | nA | $V_{GS}$ = 20V |
| $I_{GSS}$ | Gate-to-Source Leakage Reverse | — | -100 | — | -100 | | $V_{GS}$ = -20 V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | — | 25 | — | 25 | µA | $V_{DS}$=80V, $V_{GS}$ =0V |
| $R_{DS(on)}$ | Static Drain-to-Source ④ On-State Resistance (TO-3) | — | 0.18 | — | 0.24 | Ω | $V_{GS}$ = 12V, $I_D$ =9.0A |
| $R_{DS(on)}$ | Static Drain-to-Source ④ On-State Resistance (TO-204AA) | — | 0.18 | — | 0.24 | Ω | $V_{GS}$ = 12V, $I_D$ =9.0A |
| $V_{SD}$ | Diode Forward Voltage ④ | — | 1.8 | — | 1.8 | V | $V_{GS}$ = 0V, $I_S$ = 14A |

1. Part numbers IRH7130,
2. Part number IRH8130, IRH3130 and IRH4130

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

### Table 2. Single Event Effect Safe Operating Area

| Ion | LET MeV/(mg/cm²)) | Energy (MeV) | Range (µm) | $V_{DS}$(V) @$V_{GS}$=0V | @$V_{GS}$=-5V | @$V_{GS}$=-10V | @$V_{GS}$=-15V | @$V_{GS}$=-20V |
|---|---|---|---|---|---|---|---|---|
| Cu | 28 | 285 | 43 | 100 | 100 | 100 | 80 | 60 |
| Br | 36.8 | 305 | 39 | 100 | 90 | 70 | 50 | — |

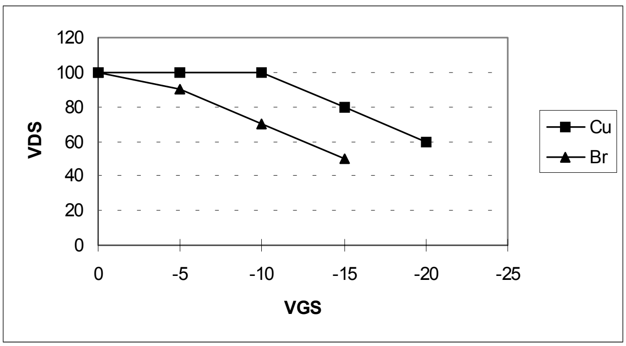



**Fig a.** Single Event Effect, Safe Operating Area

For footnotes refer to the last page

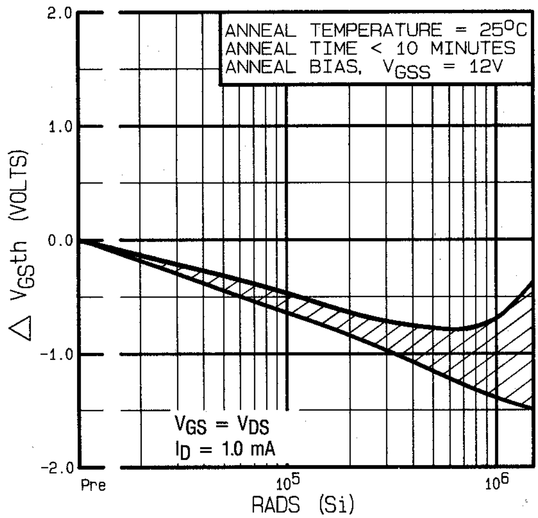



**Fig 1.** Typical Response of Gate Threshhold Voltage Vs. Total Dose Exposure

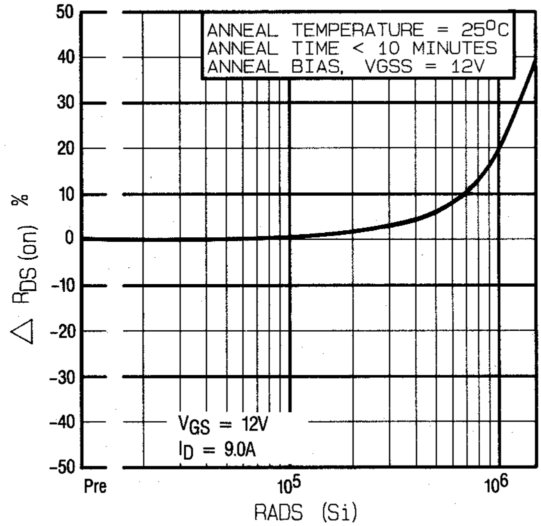



**Fig 2.** Typical Response of On-State Resistance Vs. Total Dose Exposure

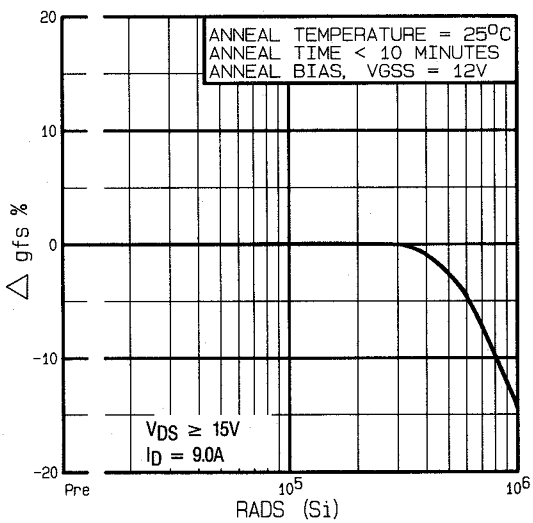



**Fig 3.** Typical Response of Transconductance Vs. Total Dose Exposure

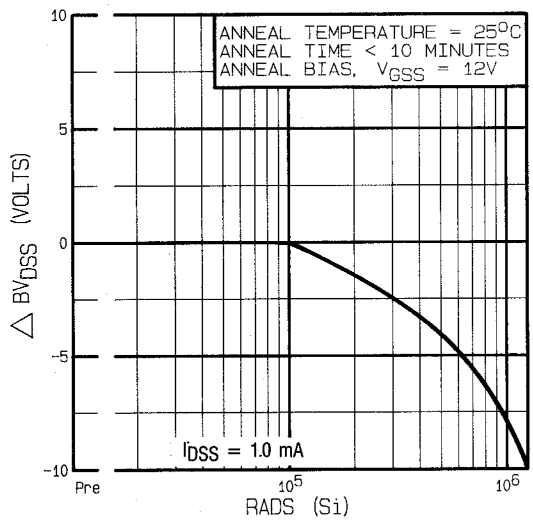



**Fig 4.** Typical Response of Drain to Source Breakdown Vs. Total Dose Exposure

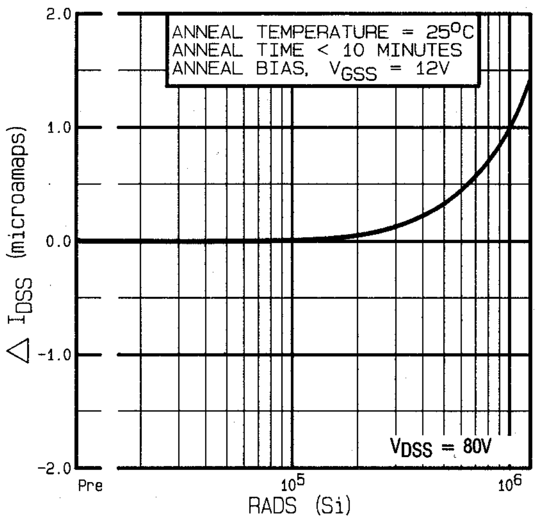



**Fig 5.** Typical Zero Gate Voltage Drain Current Vs. Total Dose Exposure

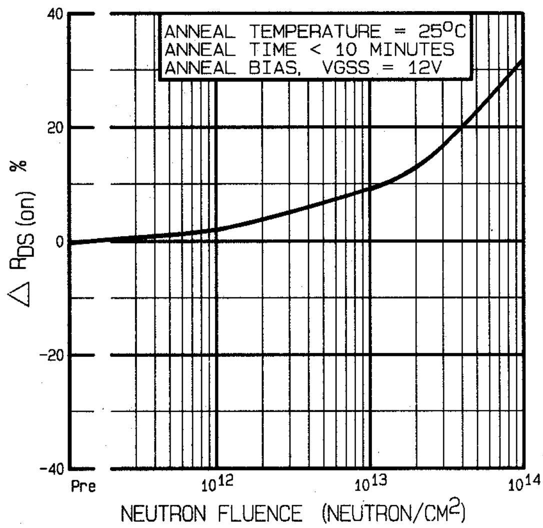



**Fig 6.** Typical On-State Resistance Vs. Neutron Fluence Level

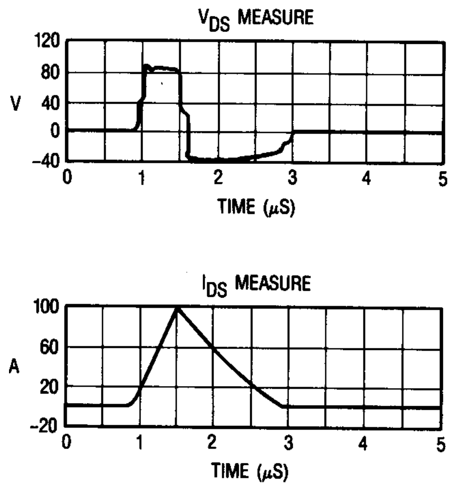



**Fig 7.** Typical Transient Response of Rad Hard HEXFET During 1x$10^{12}$ Rad (Si)/Sec Exposure

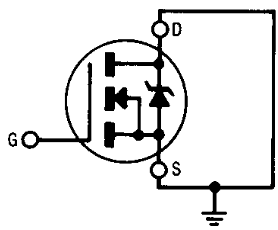



**Fig 8a.** Gate Stress of $V_{GSS}$ Equals 12 Volts During Radiation

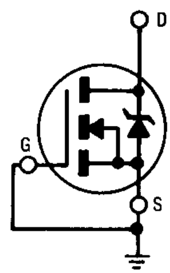



**Fig 8b.** $V_{DSS}$ Stress Equals 80% of $B_{VDSS}$ During Radiation

Note: Bias Conditions during radiation: $V_{GS}$ = 12 Vdc, $V_{DS}$ = 0 Vdc

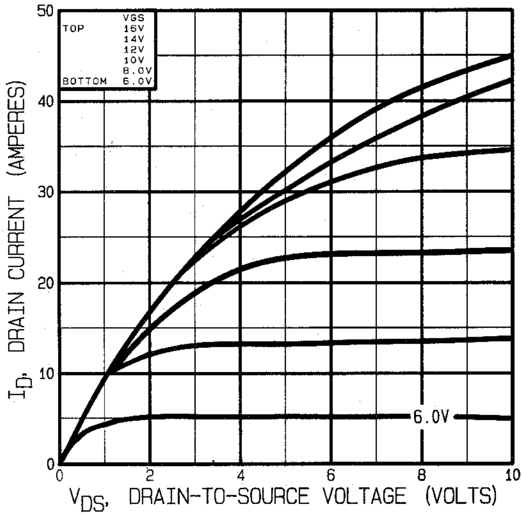



**Fig 9.** Typical Output Characteristics Pre-Irradiation

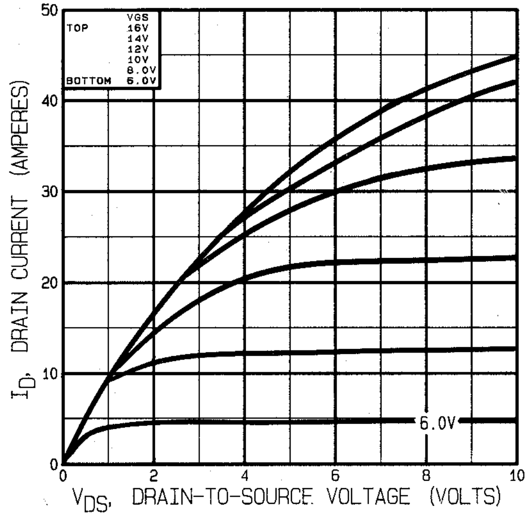



**Fig 10.** Typical Output Characteristics Post-Irradiation 100K Rads (Si)

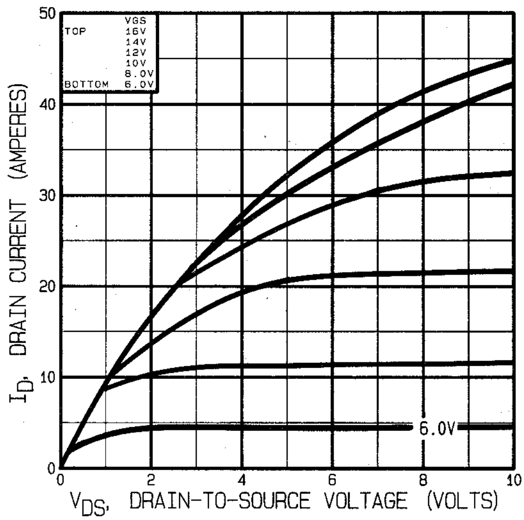



**Fig 11.** Typical Output Characteristics Post-Irradiation 300K Rads (Si)

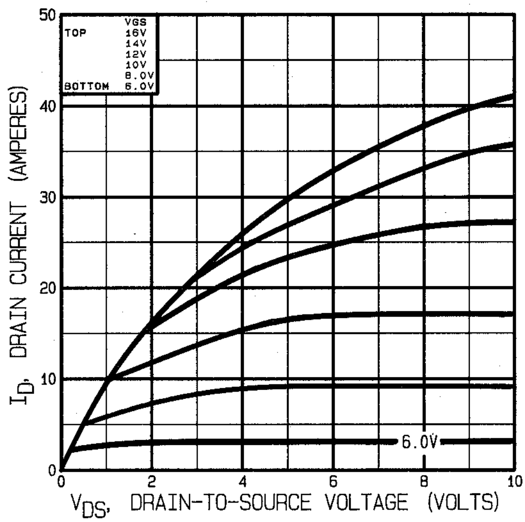



**Fig 12.** Typical Output Characteristics Post-Irradiation 1 Mega Rads (Si)

Note: Bias Conditions during radiation: $V_{GS}$ = 0 Vdc, $V_{DS}$ = 80 Vdc

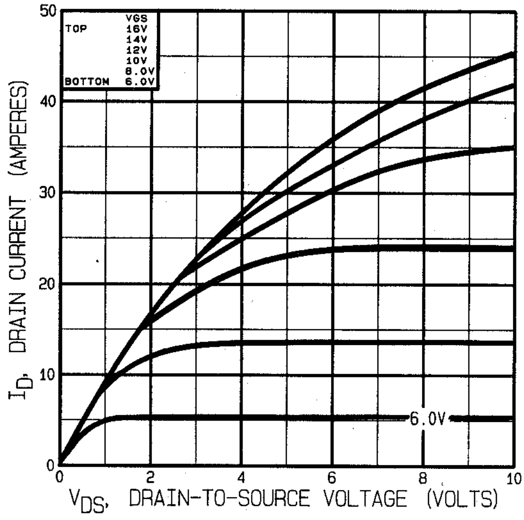



**Fig 13.** Typical Output Characteristics
Pre-Irradiation

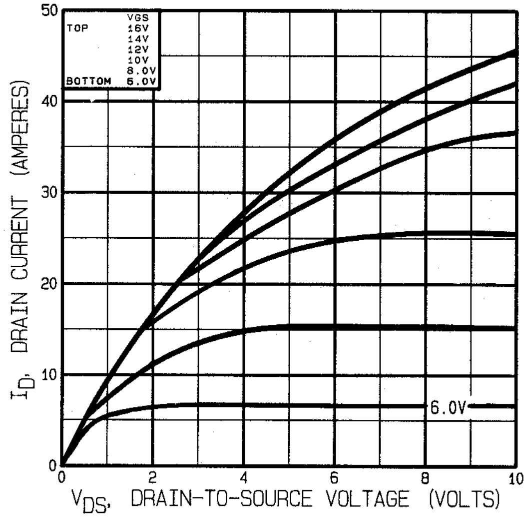



**Fig 14.** Typical Output Characteristics
Post-Irradiation 100K Rads (Si)

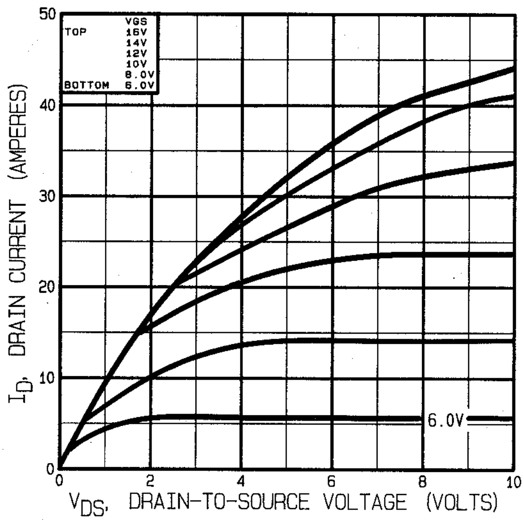



**Fig 15.** Typical Output Characteristics
Post-Irradiation 300K Rads (Si)

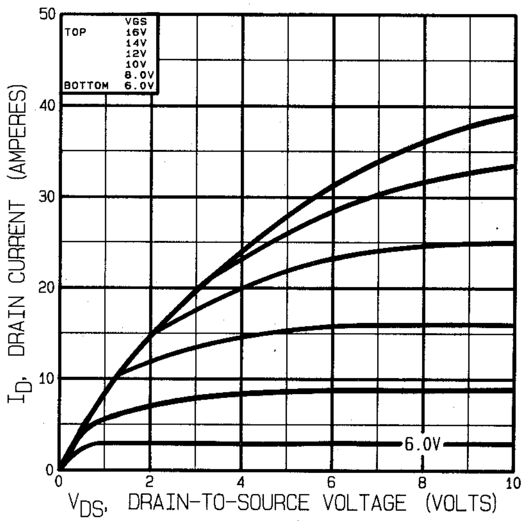



**Fig 16.** Typical Output Characteristics
Post-Irradiation 1 Mega Rads (Si)

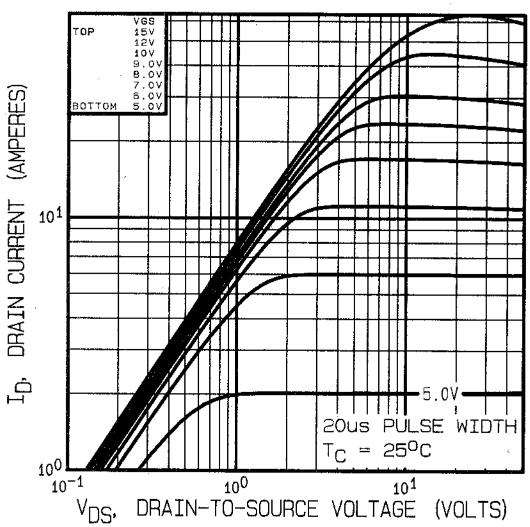



**Fig 17.** Typical Output Characteristics

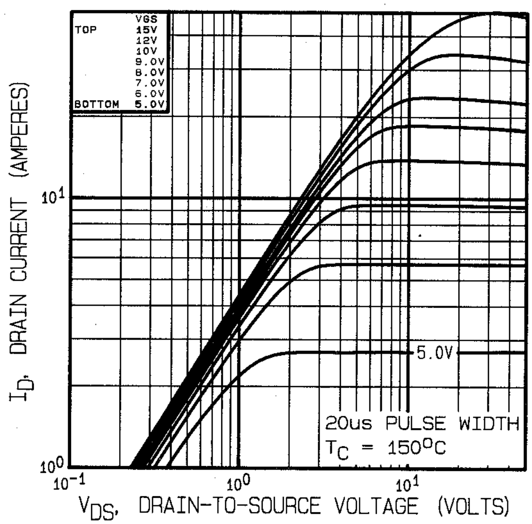



**Fig 18.** Typical Output Characteristics

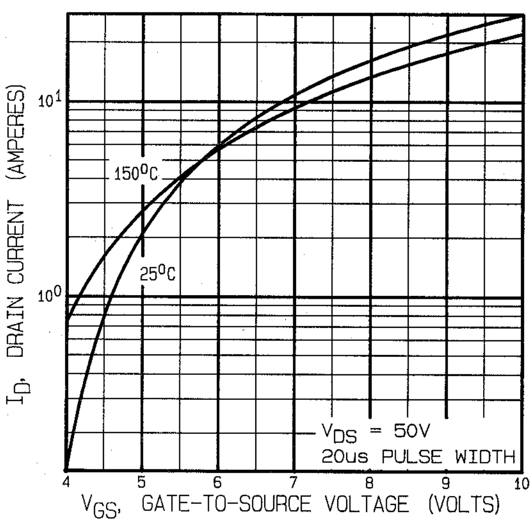



**Fig 19.** Typical Transfer Characteristics

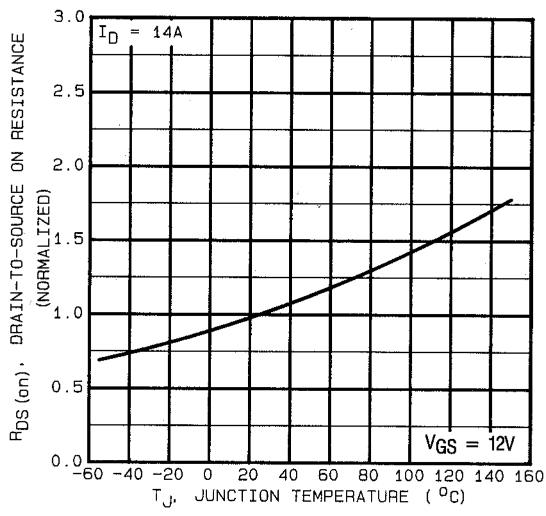



**Fig 20.** Normalized On-Resistance Vs. Temperature

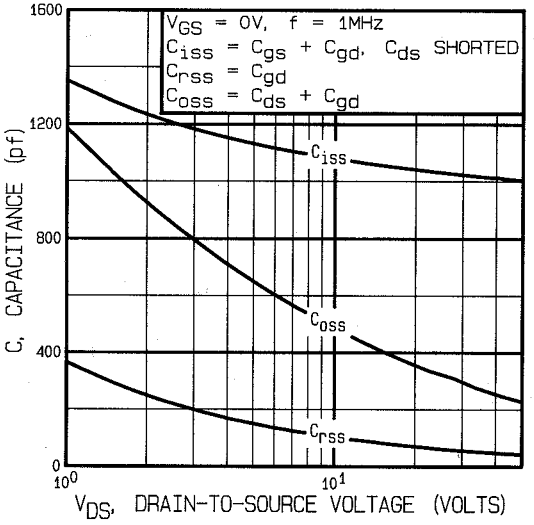



**Fig 21.** Typical Capacitance Vs. Drain-to-Source Voltage

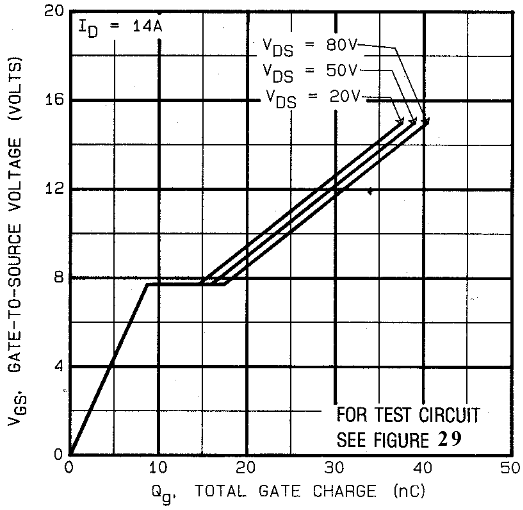



**Fig 22.** Typical Gate Charge Vs. Gate-to-Source Voltage

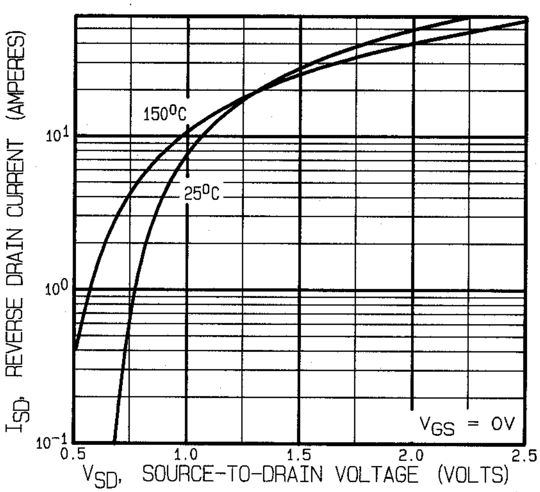



**Fig 23.** Typical Source-Drain Diode Forward Voltage

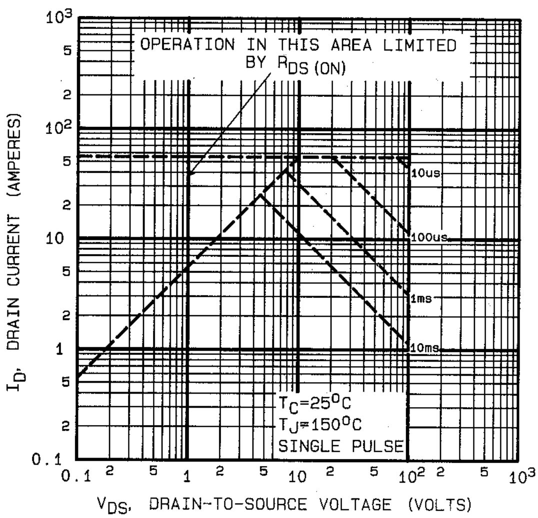



**Fig 24.** Maximum Safe Operating Area

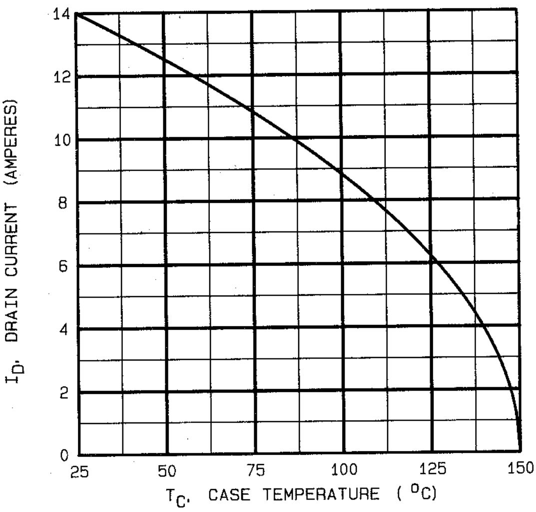



**Fig 25.** Maximum Drain Current Vs. Case Temperature

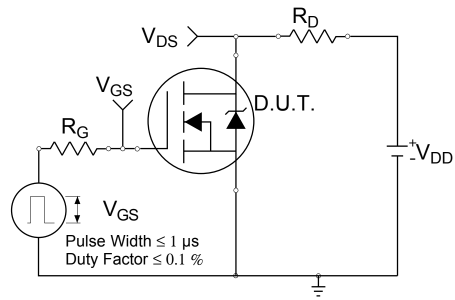



**Fig 26a.** Switching Time Test Circuit

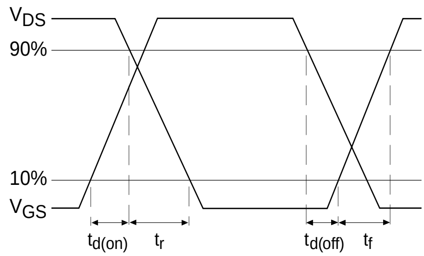



**Fig 26b.** Switching Time Waveforms

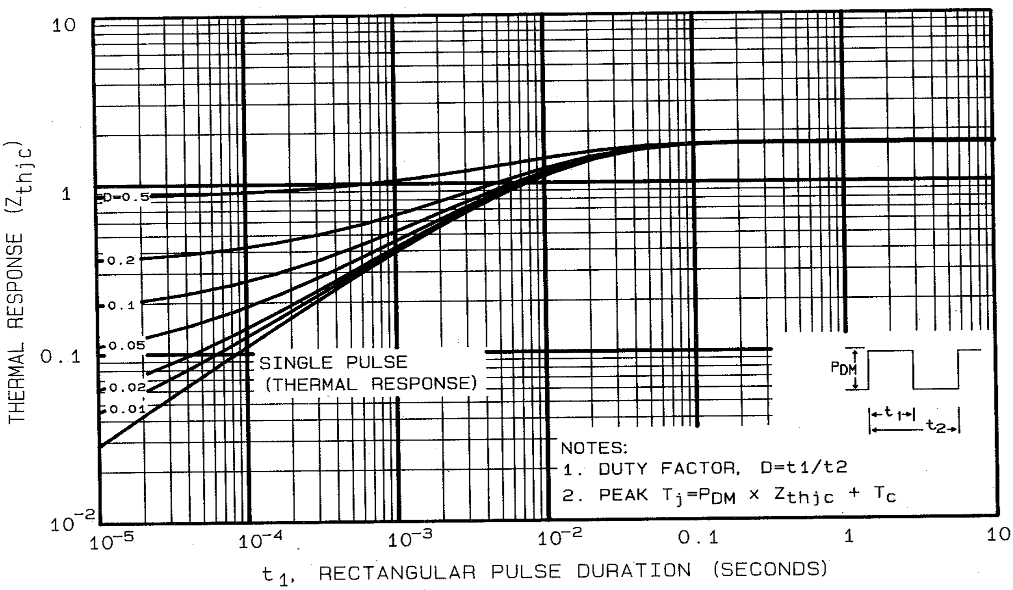



**Fig 27.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

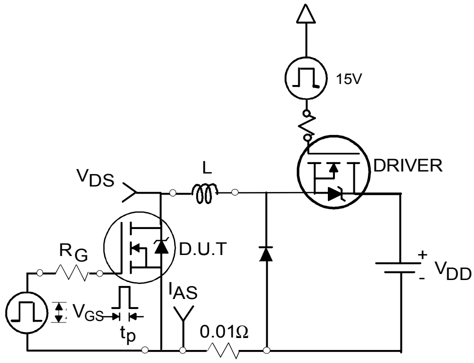



**Fig 28a.** Unclamped Inductive Test Circuit

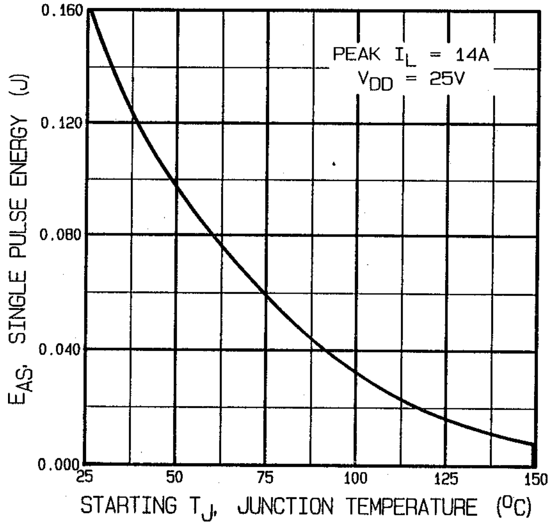



**Fig 28c.** Maximum Avalanche Energy Vs. Drain Current

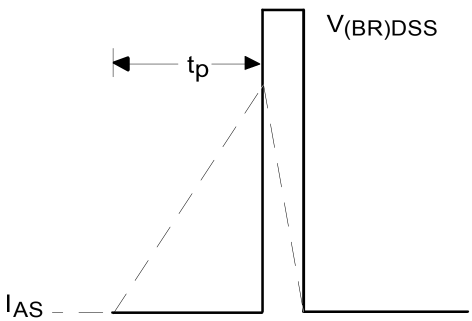



**Fig 28b.** Unclamped Inductive Waveforms

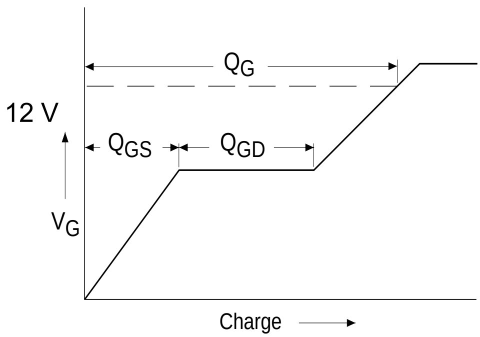



**Fig 29a.** Basic Gate Charge Waveform

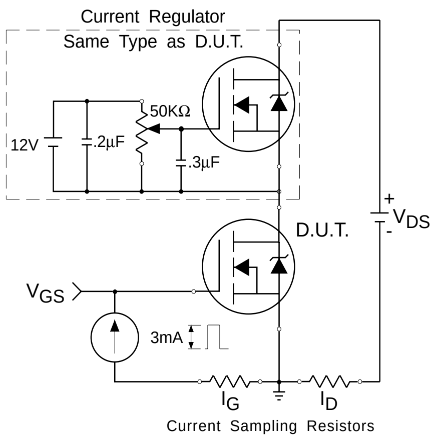



**Fig 29b.** Gate Charge Test Circuit

## Foot Notes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② $V_{DD}$ = 25V, starting $T_J$ = 25°C, L=1.63mH Peak $I_L$ = 14A, $V_{GS}$ =12V

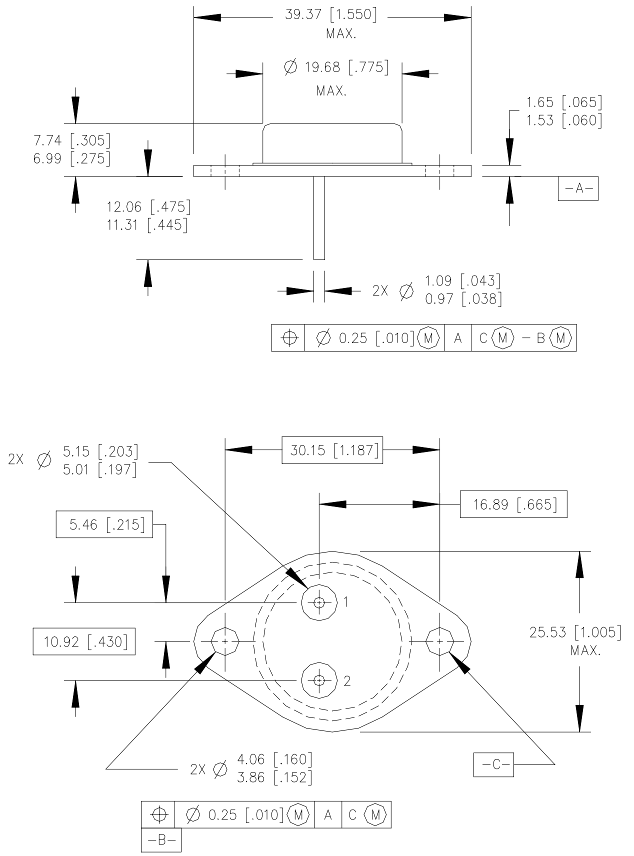
③ $I_{SD} \leq$ 14A, di/dt $\leq$ 140A/µs, $V_{DD} \leq$ 100V, $T_J \leq$ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ **Total Dose Irradiation with $V_{GS}$ Bias.** 12 volt $V_{GS}$ applied and $V_{DS}$ = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑥ **Total Dose Irradiation with $V_{DS}$ Bias.** 80 volt $V_{DS}$ applied and $V_{GS}$ = 0 during irradiation per MIL-STD-750, method 1019, condition A.

## Case Outline and Dimensions — TO-204AA




PIN ASSIGNMENTS

1 - SOURCE
2 - GATE
3 - DRAIN (CASE)

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-204-AA.

International
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Visit us at www.irf.com for sales contact information.

*Data and specifications subject to change without notice. 08/01*