

The documentation and process conversion measures necessary to comply with this revision shall be completed by 17 July 2013.

INCH-POUND

MIL-PRF-19500/601K
17 April 2013
SUPERSEDING
MIL-PRF-19500/601J
14 March 2012

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, FIELD EFFECT POWER
* TRANSISTORS, N-CHANNEL, SILICON, TYPES 2N7261 AND 2N7262 U AND U5 SUFFIXES, JANTXV, AND RADIATION HARDENED TYPE SUFFIXES, JANTXVR, F, G, AND H AND JANSR, F, G, AND H

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode, MOSFET, radiation hardened and non-hardened, power transistors. Two levels of product assurance are provided for each device type as specified in [MIL-PRF-19500](#), with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). See 6.5 for JANHC and JANKC die versions.

1.2 Physical dimensions. See [figure 1](#) (TO-205AF) and [figure 2](#) (LCC).

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type (1)	P_T (2) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$ (free air)	$R_{\theta JC}$ (3)	$R_{\theta JA}$	V_{DS} and V_{DG}	V_{GS}	I_{D1} (4) (5) $T_C = +25^\circ\text{C}$	I_{D2} (4) (5) $T_C = +100^\circ\text{C}$	I_S	I_{DM} (6)	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>°C/W</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A(pk)</u>	<u>°C</u>
2N7261	25	0.71	5.0	175	100	±20	8.0	5.0	8.0	32	-55 to +150
2N7262	25	0.71	5.0	175	200	±20	5.5	3.5	5.5	22	-55 to +150

(1) Unless otherwise specified, electrical characteristics, ratings, and conditions for "U" and "U5" suffix devices (surface mount LCC) are identical to the corresponding non "U" and "U5" suffix devices.

(2) Derate linearly 0.2 W/°C for $T_C > +25^\circ\text{C}$.

(3) See [figure 3](#), thermal impedance curves.

(4) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter:

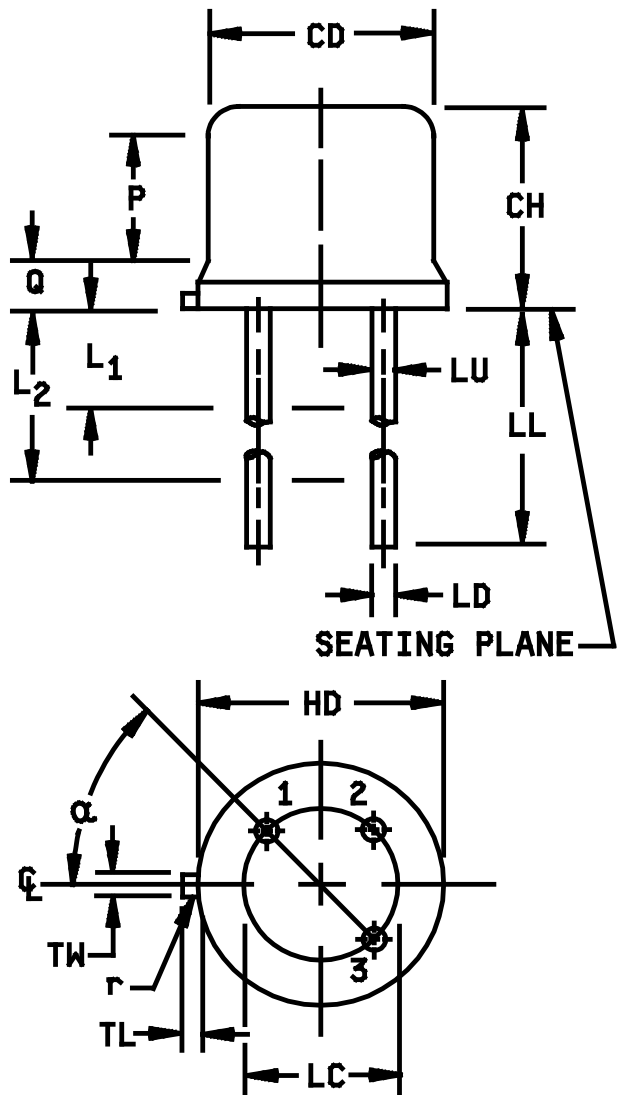
$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

(5) See [figure 4](#), maximum drain current graph.

(6) $I_{DM} = 4 \times I_{D1}$ as calculated in note (4).

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.

Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
CD	.315	.355	8.00	9.01
CH	.160	.180	4.07	4.57
HD	.340	.370	8.64	9.40
LC	.200 BSC		5.08 BSC	
LD	.016	.021	0.41	0.53
LL	.500	.750	12.70	19.05
LU	.016	.019	0.41	0.48
L ₁		.050		1.27
L ₂	.250		6.35	
P	.070		1.78	
Q		.050		1.27
r		.010		0.25
TL	.029	.045	0.74	1.14
TW	.028	.034	0.71	0.86
α	45° BSC			
Term 1	Source			
Term 2	Gate			
Term 3	Drain			



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Lead number 1 is the source, lead number 2 is the gate, lead 3 is the drain and is electrically connected to the case, lead number 4 is omitted from this outline.
4. Dimensions and tolerancing shall be in accordance with ASME Y14.5M.

FIGURE 1. Physical dimensions for TO-205AF (2N7261 and 2N7262).

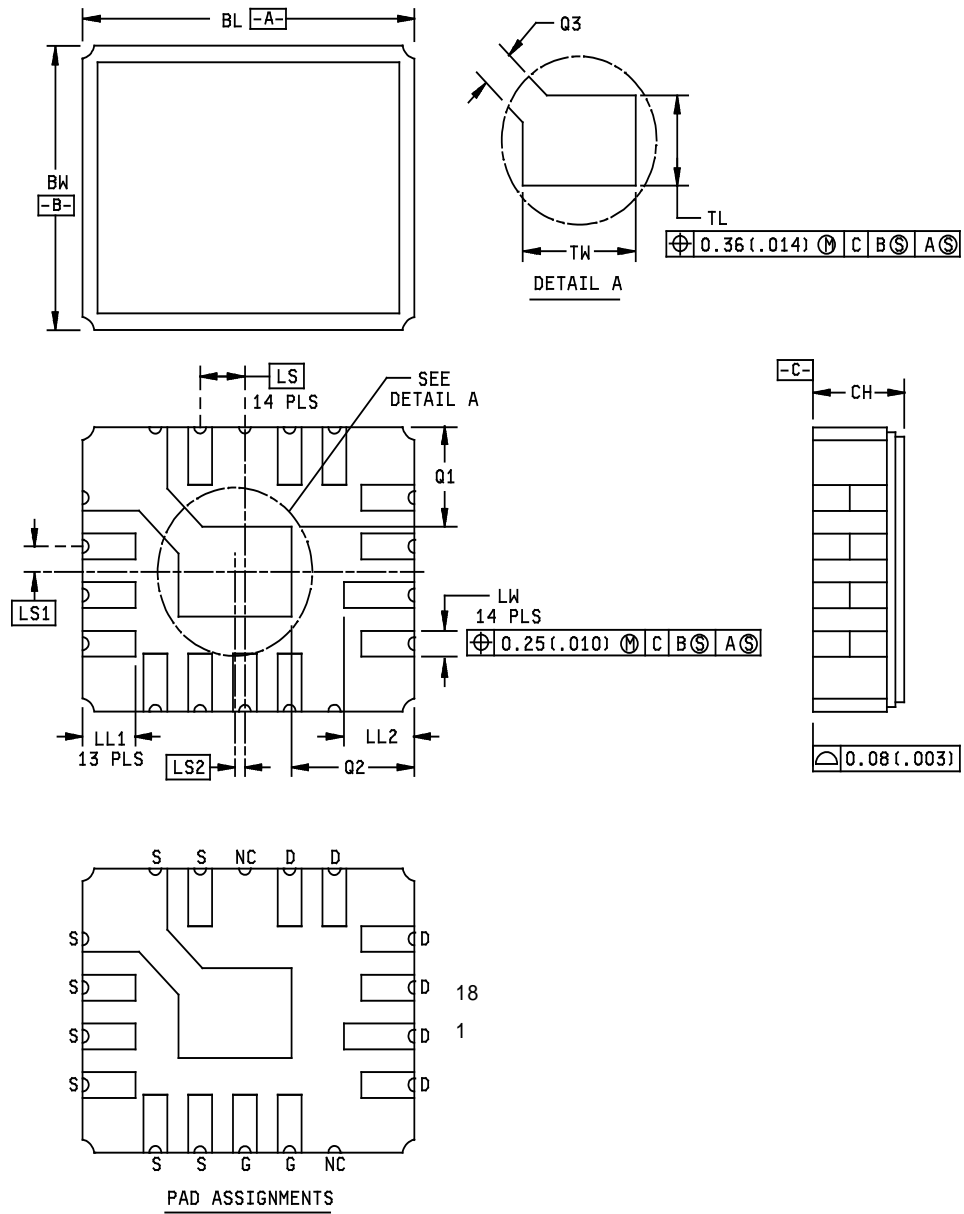


FIGURE 2. Physical dimensions for LCC (2N7261U, 2N7261U5, 2N7262U, and 2N7262U5).

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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.345	.360	8.77	9.14
BW	.280	.295	7.11	7.49
CH	.095	.115	2.41	2.92
LL ₁	.040	.055	1.02	1.40
LL ₂	.055	.065	1.40	1.65
LS	.059 BSC		1.50 BSC	
LS ₁	.025 BSC		0.635 BSC	
LS ₂	.008 BSC		0.203 BSC	
LW	.020	.030	0.51	0.76
Q ₁	.105 REF		2.67 REF	
Q ₂	.120 REF		3.05 REF	
Q ₃	.045	.055	1.14	1.40
TL	.070	.080	1.78	2.03
TW	.120	.130	3.05	3.30

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimensions and tolerancing shall be in accordance with ASME Y14.5M.
4. The U5 suffix is the preferred suffix designation for this LCC package.

FIGURE 2. Physical dimensions for LCC (2N7261U, 2N7261U5, 2N7262U, and 2N7262U5) - Continued.

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1.4 Primary electrical characteristics at $T_C = +25^\circ\text{C}$.

Type (1)	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0$ mA dc	$V_{GS(TH)}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0$ mA dc	Max I_{DSS1} $V_{GS} = 0$ $V_{DS} = 80$ percent of rated V_{DS}	Max $r_{DS(ON)}$ (2) $V_{GS} = 12$ V dc		E_{AS} at I_{D1}	I_{AS}	
				$T_J = +25^\circ\text{C}$ at I_{D2}	$T_J = +150^\circ\text{C}$ at I_{D2}			
	<u>V dc</u>	<u>V dc</u>		<u>$\mu\text{A dc}$</u>	<u>ohm</u>	<u>ohm</u>	<u>mJ</u>	<u>A</u>
		Min	Max					
2N7261	100	2.0	4.0	25	0.180	0.390	130	8.0
2N7262	200	2.0	4.0	25	0.350	0.840	240	5.5

- (1) Unless otherwise specified, electrical characteristics, ratings, and conditions for “U” and “U5” suffix devices (surface mount LCC) are identical to the corresponding non “U” and “U5” suffix devices.
 (2) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <https://assist.dla.mil/quicksearch/> or <https://assist.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

I_{AS} Rated avalanche current, non-repetitive.
nC nano Coulomb.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on [figures 1](#) (TO-205AF) and [2](#) (LCC) herein.

3.4.1 Lead finish. Lead finish shall be solderable as defined in [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead material or finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Internal construction. Multiple chip construction is not permitted.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see [3.5](#)).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.8 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II herein).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.1.1 Single event effects (SEE). SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with table II. SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

* 4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with, table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV levels
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, (see 4.3.2)	Method 3470 of MIL-STD-750, (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, (see 4.3.3)	Method 3161 of MIL-STD-750, (see 4.3.3)
9	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , subgroup 2 of table I herein	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein; $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater.	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(on)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value.	Subgroup 2 of table I herein $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value.

(1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.

(2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} , and $V_{GS(th)1}$ shall be invoked.

* (3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply $V_{GS} = +30$ V minimum for $t = 250$ μ s minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current (I_{AS}) $I_{AS(max)}$.
- b. Peak gate voltage (V_{GS}) 10 V.
- c. Gate to source resistor (R_{GS}) $25\Omega \leq R_{GS} \leq 200\Omega$.
- d. Initial case temperature (T_C) $+25^\circ\text{C} +10^\circ\text{C}, -5^\circ\text{C}$.
- e. Inductance (L) $L = \left[\frac{2 E_{AR}}{(I_{DI})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right]$ nH minimum
- f. Number of pulses to be applied 1 pulse minimum.
- g. Supply voltage (V_{DD}) 25 V for 2N7261, 2N7261U, 50 V for 2N7262, 2N7262U.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μ s max. See [table III](#), group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#). End-point electrical measurements shall be in accordance with [table I](#), subgroup 2 herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of [MIL-PRF-19500](#) and herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

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4.4.2.1 Group B inspection, table E-VIA (JANS) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>	
B3	1051	Test condition G, 100 cycles.	
B3	2075	See 3.4.2 herein.	
B3	2077	Scanning electron microscope (SEM) qualification may be performed anytime prior to lot formation.	
B3	2037	Test condition A, all internal wires for each device shall be pulled separately.	
B4	1042	Condition D, 2,000 cycles. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 30 seconds minimum.	
B5	1042	Test condition A, $V_{DS} = \text{rated}$ $T_A = +175^\circ\text{C}$, $t = 120$ hours.	
B5	1042	Condition B, $V_{GS} = \text{rated}$; $T_A = 175^\circ\text{C}$; $t = 24$ hours.	
*	B5	2037	Bond strength; test condition D.
B6	3161	Not applicable.	

4.4.2.2 Group B inspection, table E-VIB (JANTXV) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
B3	1042	Test condition D, 2,000 cycles; The heating cycle shall be 30 seconds minimum.
B4	2075	See 3.4.2 herein.
B5 and B6		Not applicable.

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4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	1056	Test condition B.
C2	2036	Test condition E; weight = 8 ounces, 3 arcs of 90 degrees (applicable to TO-205AF only).
C2	1021	Omit initial conditioning.
C5	3161	See 4.3.3, $R_{\theta JC(max)} = 5.0^{\circ}C/W$.
C6	1042	Test condition D, 6,000 cycles. The heating cycle shall be 30 seconds minimum.

4.4.4 Group D Inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

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TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source	3407	$V_{GS} = 0$, $I_D = 1$ mA dc, bias condition C	$V_{(BR)DSS}$	100 200		V dc V dc
2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5						
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ $I_D = 1$ mA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate current	3411	$V_{GS} = +20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSF1}		+100	nA dc
Gate current	3411	$V_{GS} = -20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSR1}		-100	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS1}		25	μA dc
Static drain to source on-state resistance	3421	$V_{GS} = 12$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)1}$			
2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5					0.180 0.350	ohm ohm
Static drain to source on-state resistance	3421	$V_{GS} = 12$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$r_{DS(on)2}$			
2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5					0.185 0.364	ohm ohm
Forward voltage	4011	Pulsed (see 4.5.1), $I_D = I_{D1}$, $V_{GS} = 0$	V_{SD}			
2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5					1.5 1.4	V V

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/ <u>Subgroup 3</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
High-temperature operation:		$T_C = T_J = +125^\circ\text{C}$				
Gate current	3411	$V_{GS} = +20\text{ V dc and } -20\text{ V dc, bias condition C, } V_{DS} = 0$	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 100$ percent of rated V_{DS}	I_{DSS2}		1.0	mA dc
		$V_{DS} = 80$ percent of rated V_{DS}	I_{DSS3}		0.25	mA dc
Static drain to source on-state resistance	3421	$V_{GS} = 12\text{ V dc, pulsed (see 4.5.1), } I_D = I_{D2}$	$r_{DS(on)3}$			
2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5					0.350 0.6	ohm ohm
Gate to source voltage (thresholds)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1\text{ mA dc}$	$V_{GS(TH)2}$	1.0		V dc
Low-temperature operation:		$T_C = T_J = -55^\circ\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1\text{ mA dc}$	$V_{GS(TH)3}$		5.0	V dc
<u>Subgroup 4</u>						
Forward transconductance	3475	$I_D = \text{rated } I_{D2}$, $V_{DD} = 15\text{ V, pulsed (see 4.5.1)}$	g_{FS}			
2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5				2.5 2.5		S S
Switching time test	3472	$I_D = I_{D1}$, $V_{GS} = 12\text{ V dc, } R_G = 2.35\Omega$, $V_{DD} = 50$ percent of rated V_{DS}				
Turn-on delay time			$t_{d(on)}$			
2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5					25 25	ns ns

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u> - Continued.						
Rise time 2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5			t_r		32 40	ns ns
Turn-off delay time 2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5			$t_{d(off)}$		40 60	ns ns
Fall time 2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5			t_f		40 45	ns ns
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 5, $t_p = 10$ ms minimum, $V_{DS} = 80$ percent of maximum rated V_{DS} , ($V_{DS} \leq 200$)				
Electrical measurements		See table I, subgroup 2 herein.				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge On-state gate charge 2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5	3471	Condition B	$Q_{G(on)}$		50 50	nC nC
Gate to source charge 2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5			Q_{GS}		10 10	nC nC

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 7</u> - Continued.						
Gate to drain charge 2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5			Q_{GD}		20 25	nC nC
Reverse recovery time 2N7261, 2N7261U, 2N7261U5 2N7262, 2N7262U, 2N7262U5	3473	$d/d_t \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq 30 \text{ V}$, $I_D = I_{D1}$	t_{rr}		270 400	ns ns

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:

- Group B, subgroups 3 and 4 (JANS).
- Group B, subgroups 2 and 3 (JANTXV).
- Group C, subgroups 2 and 6.
- Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection <u>1/ 2/ 3/ 4/</u>	MIL-STD-750		Symbol	Pre-irradiation limits				Post-irradiation limits				Unit
	Method	Conditions		R		F, G, and H <u>5/</u>		R		F, G, and H <u>5/</u>		
				Min	Max	Min	Max	Min	Max	Min	Max	
<u>Subgroup 1</u>												
Not applicable												
<u>Subgroup 2</u>		$T_C = +25^\circ\text{C}$										
Steady-state total dose irradiation (V_{GS} bias) <u>6/</u>	1019	$V_{GS} = 12\text{ V},$ $V_{DS} = 0$										
Steady-state total dose irradiation (V_{DS} bias) <u>6/</u>	1019	$V_{GS} = 0,$ $V_{DS} = 80$ percent of rated V_{DS} (pre-irradiation)										
End-point electrical												
Breakdown voltage, drain to source	3407	$V_{GS} = 0,$ $I_D = 1\text{ mA},$ bias condition C	V_{BRDSS}									
2N7261 2N7262				100 200		100 200		100 200		100 200		V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ $I_D = 1\text{ mA}$	V_{GSth}									
2N7261 2N7262				2 2	4 4	2 2	4 4	2 2	4 4	1.25 1.25	4.50 4.50	V dc V dc
Gate current	3411	$V_{GS} = 20\text{ V},$ $V_{DS} = 0,$ bias condition C	I_{GSSF1}		100		100		100		100	nA dc
Gate current	3411	$V_{GS} = -20\text{ V},$ $V_{DS} = 0,$ bias condition C	I_{GSSR1}		-100		-100		-100		-100	nA dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

Inspection <u>1/ 2/ 3/ 4/</u>	MIL-STD-750		Symbol	Pre-irradiation limits				Post-irradiation limits				Unit
	Method	Conditions		R		F, G, and H <u>5/</u>		R		F, G, and H <u>5/</u>		
				Min	Max	Min	Max	Min	Max	Min	Max	
<u>Subgroup 2</u> - Continued.												
Drain current	3413	$V_{GS} = 0$ Bias condition C $V_{DS} = 80$ percent of rated V_{DS} (pre-irradiation)	I_{DSS}									
2N7261 2N7262					25 25		25 25		25 25		50 50	μA dc μA dc
Static drain to source on- state voltage	3405	$V_{GS} = 12$ V condition A pulsed (see 4.5.1) $I_D = I_{D2}$	V_{DSON1}									
2N7261 2N7262					0.9 1.225		0.9 1.225		0.9 1.225		1.2 1.68	V dc V dc
Forward voltage Source drain diode	4011	$V_{GS} = 0$ $I_D = I_{D1}$	V_{SD}									
2N7261 2N7262					1.5 1.4		1.5 1.4		1.5 1.4		1.5 1.4	V dc V dc

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.

3/ At the manufacturers option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ Unless otherwise specified, electrical characteristics, ratings, and conditions for "U" and "U5" suffix devices (surface mount LCC) are identical to the corresponding non "U" or "U5" suffix devices.

5/ The F designation represent devices which pass end-points at both 100K and 300K rad (Si). The G designation represents devices which pass 100K, 300K, and 500K rad (Si) end-points. The H designation represents devices which pass 100K, 300K, 500K and 1000K rad (Si).

6/ Separate samples shall be pulled for each bias.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	
<u>Subgroup 11</u>			3 devices
SEE 2/ 3/	1080	See MIL-STD-750 method 1080.	

1/ A separate sample for each test shall be pulled.

2/ Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

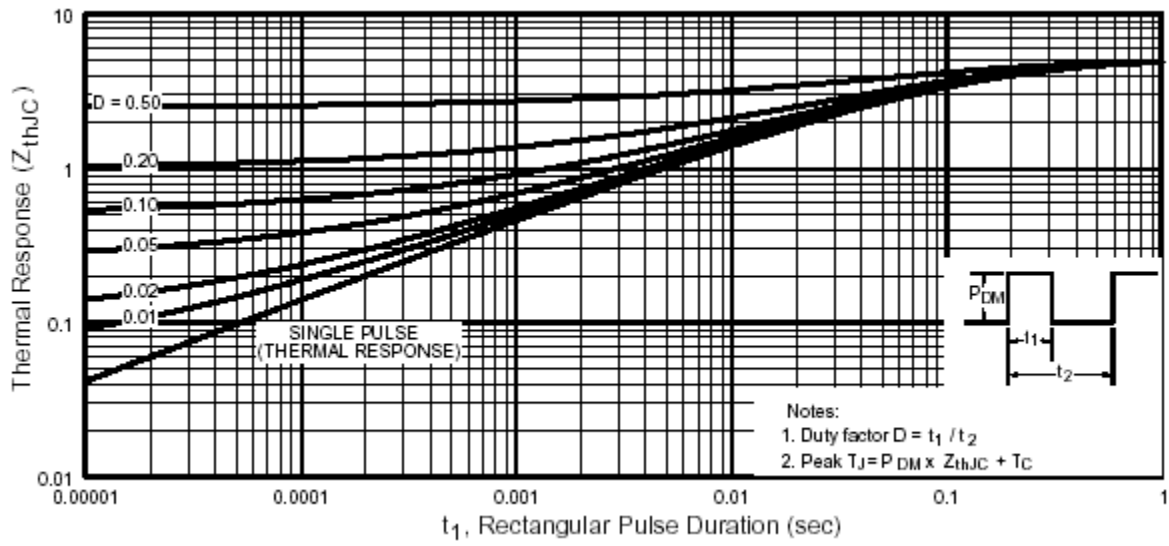


FIGURE 3. Thermal impedance curves (all devices).

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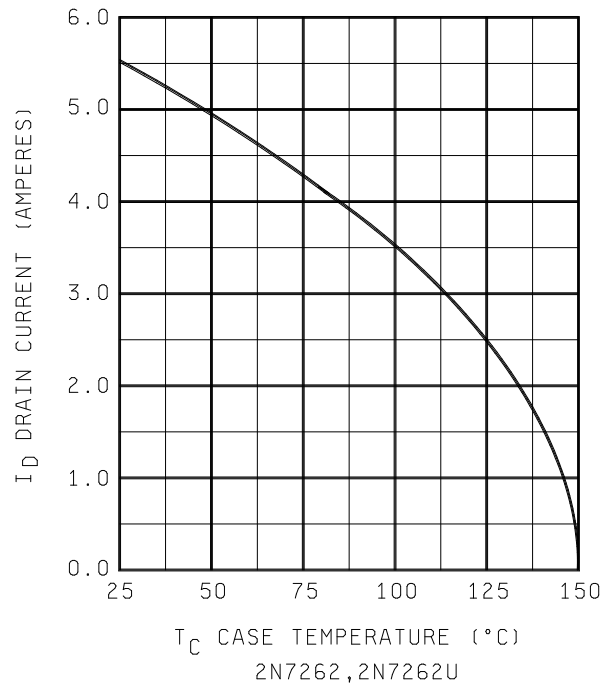
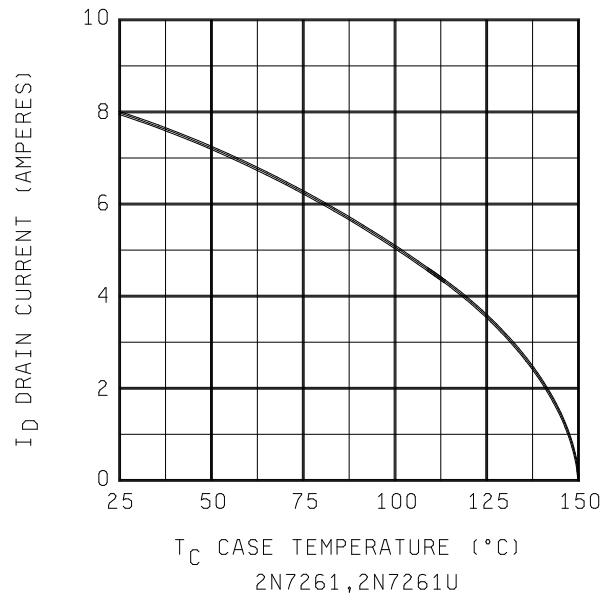
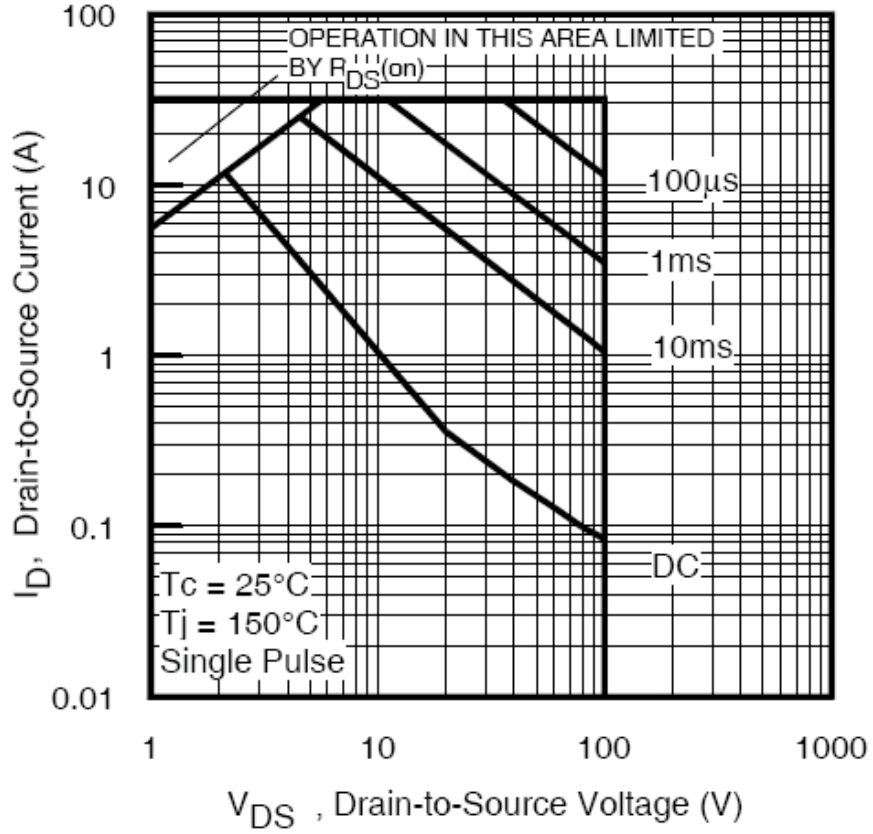
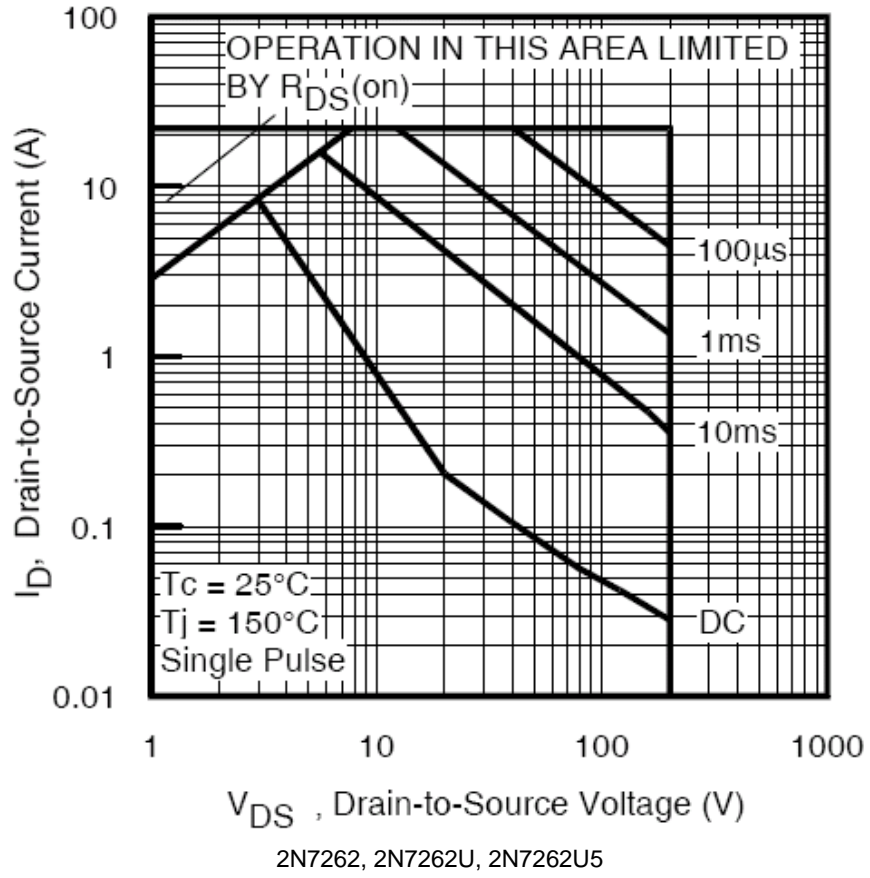


FIGURE 4. Maximum drain current versus case temperature graphs.



2N7261, 2N7261U, 2N7261U5

* FIGURE 5. Safe operating area graphs.



* FIGURE 5. Safe operating area graphs - continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.
- * e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract or order.
- * f. If SEE testing data is desired, it should be specified in the contract or order.
- * g. If specific SEE characterization conditions are desired (see section 6.6 and table IV), manufacturer's cage code should be specified in the contract or order.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

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6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types	Commercial types	
	TO-205AF	LCC
2N7261, U 2N7262, U	IRHFX130 (1) IRHFX230 (1)	IRHEX130 (1) IRHEX230 (1)

- (1) Replace "X" with number indicating qualified radiation hardness as follows:
 7 = 100K Rad Si.
 3 = 300K Rad Si.
 4 = 500K Rad Si.
 8 = 1,000K Rad Si.

6.5 JANC die versions. The JANHC and JANKC die versions of these devices are covered under performance specification sheet [MIL-PRF-19500/657](#).

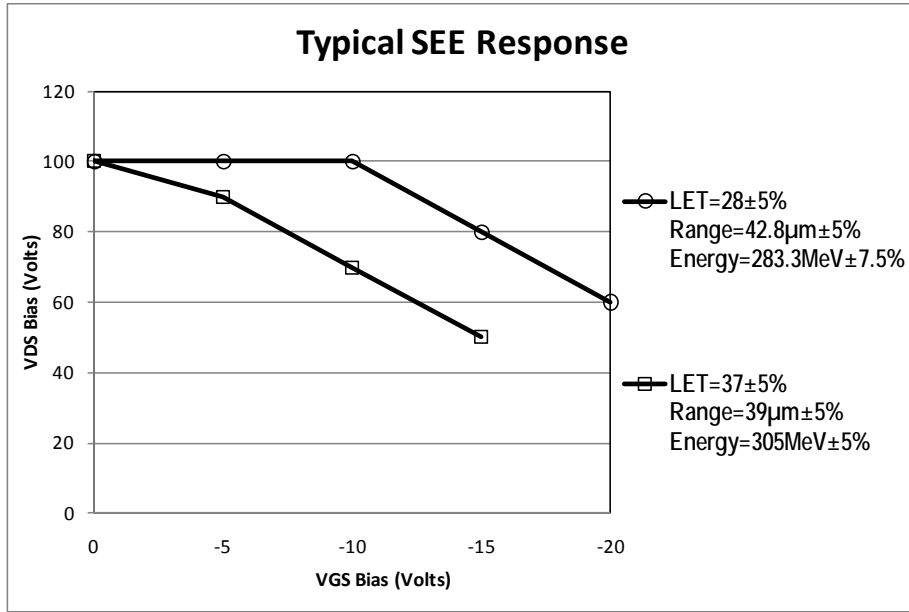
* 6.6 Application data.

* 6.6.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of [MIL-STD-750](#) method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the [MIL-STD-750](#) method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see [table IV](#)) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

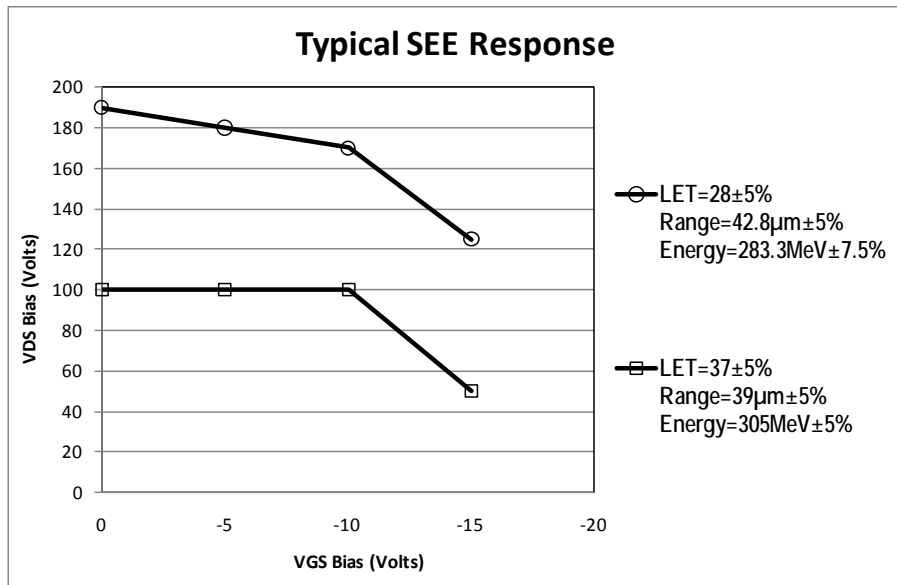
* TABLE IV. Manufacturers characterization conditions.

Manufactures cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of 14 March 2012 and older)	SEE <u>1/</u>	1080	See MIL-STD-750E method 1080.0 dated 20 November 2006. See figure 6.	3 devices
	Electrical measurements		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I, subgroup 2	
	SEE irradiation:		Fluence = $3E5 \pm 20$ percent ions/cm ² Flux = $2E3$ to $2E4$ ions/cm ² /sec, temperature = $25^\circ \pm 5^\circ C$	
	(2N7261, 2N7261U, 2N7261U5)		Surface LET = $28 \text{ MeV-cm}^2/\text{mg} \pm 5.0\%$, range = $42.8 \mu\text{m} \pm 7.5\%$, energy = $283.3 \text{ MeV} \pm 7.5\%$ In-situ bias conditions: $V_{DS} = 100 \text{ V}$ and $V_{GS} = -10 \text{ V}$ $V_{DS} = 80 \text{ V}$ and $V_{GS} = -15 \text{ V}$ $V_{DS} = 60 \text{ V}$ and $V_{GS} = -20 \text{ V}$ (nominal 4.53 MeV/nucleon at Brookhaven National Lab Accelerator)	
	(2N7262, 2N7262U, 2N7262U5)		In-situ bias conditions: $V_{DS} = 190 \text{ V}$ and $V_{GS} = 0 \text{ V}$ $V_{DS} = 180 \text{ V}$ and $V_{GS} = -5 \text{ V}$ $V_{DS} = 170 \text{ V}$ and $V_{GS} = -10 \text{ V}$ $V_{DS} = 125 \text{ V}$ and $V_{GS} = -15 \text{ V}$ (nominal 4.53 MeV/nucleon at Brookhaven National Lab Accelerator)	
(2N7261, 2N7261U, 2N7261U5)	Surface LET = $37 \text{ MeV-cm}^2/\text{mg} \pm 5\%$, range = $39 \mu\text{m} \pm 10\%$, energy = $305 \text{ MeV} \pm 7.5\%$ In-situ bias conditions: $V_{DS} = 100 \text{ V}$ and $V_{GS} = 0 \text{ V}$ $V_{DS} = 90 \text{ V}$ and $V_{GS} = -5 \text{ V}$ $V_{DS} = 70 \text{ V}$ and $V_{GS} = -10 \text{ V}$ $V_{DS} = 50 \text{ V}$ and $V_{GS} = -15 \text{ V}$ (typical 3.77 MeV/nucleon at Brookhaven National Lab Accelerator)			
(2N7262, 2N7262U, 2N7262U5)	In-situ bias conditions: $V_{DS} = 100 \text{ V}$ and $V_{GS} = -10 \text{ V}$ $V_{DS} = 50 \text{ V}$ and $V_{GS} = -15 \text{ V}$ (nominal 3.77 MeV/nucleon at Brookhaven National Lab Accelerator)			
	Electrical measurements		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I, subgroup 2	
<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;"> Upon qualification, all manufacturers should provide the verification test conditions to be added to this table. </div>				

1/ I_{GSSF1} , I_{GSSR1} , and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.



2N7261, 2N7261U, 2N7261U5



2N7262, 2N7262U, 2N7262U5

* FIGURE 6. Typical single-event-effects safe-operating-area graphs.

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:

DLA - CC

(Project - 5961-2012-077)

Review activities:

Army - MI
Air Force - 19, 70

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.