The documentation and process conversion measures necessary to comply with this revision shall be completed by 5 July 2013.

INCH-POUND

MIL-PRF-19500/753B
20 May 2013
SUPERSEDING
MIL-PRF-19500/753A
19 May 2010

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED
(TOTAL DOSE AND SINGLE EVENT EFFECTS) TRANSISTOR, N-CHANNEL,
SILICON, TYPES 2N7580T1, 2N7582T1, 2N7584T1, AND 2N7586T1,
JANTXVR, JANTXVF, JANSR, AND JANSF

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}).

1.2 Physical dimensions. See figure 1, (TO-254AA).

1.3 Maximum ratings. T_A = +25°C, unless otherwise specified.

Type	P_T (1) T_C =+25°C	P_T T_A =+25°C	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) T_C =+25°C	I_{D2} T_C =+100°C	I_S	I_{DM} (5)	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A (pk)	°C
2N7580T1	208	2.60	0.6	100	100	±20	45	45	45	180	-55 to +150
2N7582T1	208	2.60	0.6	150	150	±20	45	44	45	180	
2N7584T1	208	2.60	0.6	200	200	±20	45	35	45	180	
2N7586T1	208	2.60	0.6	250	250	±20	45	28.5	45	180	

(1) Derate linearly by 1.67 W/°C for T_C > +25°C.
(2) See figure 2, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D limit. I_D is limited to 45 A (by package and internal wires and may be limited by pin diameter):

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 3, maximum drain current graph.
(5) I_{DM} = 4 X I_{D1}; I_{D1} as calculated by footnote (3).

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80% of rated V_{DS}	Max $r_{DS(on)}$ (1) V_{GS} = 12V, I_D = I_{D2}		V_{ISO} 70,000 ft. altitude	E_{AS}
					T_J = +25°C	T_J = +150°C		
	V dc	V dc		µA dc	Ω	Ω	V dc	mJ
		Min	Max					
2N7580T1	100	2.0	4.0	10	0.011	0.021		512
2N7582T1	150	2.0	4.0	10	0.019	0.043		353
2N7584T1	200	2.0	4.0	10	0.029	0.068		344
2N7586T1	250	2.0	4.0	10	0.041	0.103	250	251

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

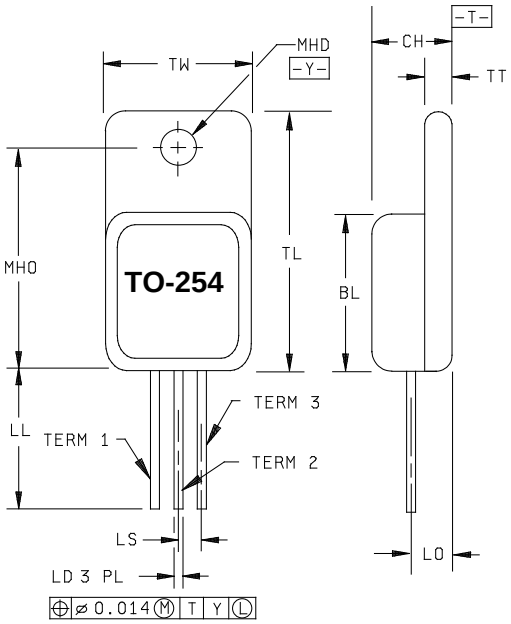
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil/ or https://assist.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.570	12.95	14.48	3
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.78	
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	4
TT	.040	.050	1.02	1.27	
TW	.535	.545	13.59	13.84	4
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Dimensions and configuration, TO-254AA.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (TO-254AA) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Multiple chip construction. Multiple chip construction is not permitted to meet the requirements of this specification.

3.5 Electrostatic discharge (ESD) protection. The devices covered by this specification require electrostatic discharge protection (see 3.5.1).

3.5.1 Handling. Metal oxide semiconductor (MOS) devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq$ or 100 kΩ, whenever bias voltage is applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS and JANTXV). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS	JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
9	Subgroup 2 of table I herein I_{GSSF1}, I_{GSSR1}, I_{DSS1} as a minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein. ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.	Subgroups 2 and 3 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.
* 17	Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein.	Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and $V_{GS(th)1}$ shall be invoked.
* (3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 24 V minimum for t = 250 μs minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current ..... $I_{AS} = I_{D1}$.

b. Inductance: ..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

c. Gate to source resistor (R_{GS}) ..... $25 \leq R_{GS} \leq 200\ \Omega$.

d. Supply voltage (V_{DD}) ..... V_{DD} = 25 V dc, except V_{DD} = 50 V dc (2N7586T1), up to rated V_{DS}.

e. Peak gate voltage (V_{GS}) ..... 12 V, up to maximum rated V_{GS}.

f. Initial case temperature ..... T_C = +25°C +10°C, -5°C.

g. Number of pulses to be applied ..... 1 pulse minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 30 - 60 μs max. See table III, group E, subgroup 4 herein.

* 4.3.4 Dielectric withstanding voltage.

a. Magnitude of test voltage……900 V dc.

b. Duration of application of test voltage……..15 seconds (min).

c. Points of application of test voltage……All leads to case (bunch connection).

d. Method of connection……Mechanical.

e. Kilovolt-ampere rating of high voltage source……..1,200V /1.0 mA (min).

f. Maximum leakage current……1.0 mA.

g. Voltage ramp up time……500V /second.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

* 4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1051	Test condition G, 100 cycles.
* B4	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle; t_{on} = 30 seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated; T_A = +175°C, t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.
B5	2037	Test condition D.

* 4.4.2.2 Group B inspection, table E-VIB (JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles.
* B3	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle; t_{on} = 30 seconds minimum.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

Subgroup	Method	Condition
C2	2036	Test condition A, weight = 10 lbs., t = 10 s.
C5	3161	See 4.3.3, $R_{\theta JC}$ = 0.60 °C/W.
* C6	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with MIL-PRF-19500, and table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.5.1 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. See the safe operation area graph herein. End-point measurements shall be in accordance with table III.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source	3407	Bias condition C, V_{GS} = 0 V, I_D = 1 mA dc	$V_{(BR)DSS}$			
2N7580T1				100		V dc
2N7582T1				150		V dc
2N7584T1				200		V dc
2N7586T1				250		V dc
Gate to source voltage (threshold)	3404	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate current	3411	V_{GS} = +20 V dc, bias condition C, V_{DS} = 0 V	I_{GSSF1}		+100	nA dc
Gate current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0 V	I_{GSSR1}		-100	nA dc
Drain current	3413	V_{GS} = 0 V dc, bias condition C, V_{DS} = 80 percent of rated V_{DS},	I_{DSS1}		10	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$			
2N7580T1					0.011	Ω
2N7582T1					0.019	Ω
2N7584T1					0.029	Ω
2N7586T1					0.041	Ω
Forward voltage	4011	V_{GS} = 0 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}		1.2	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 3						
High temperature operation		$T_C = T_J = +125°C$				
Gate current	3411	$V_{GS} = \pm 20$ V dc, bias condition C, $V_{DS} = 0$ V	I_{GSS2}		±200	nA dc
Drain current	3413	$V_{GS} = 0$ V dc, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		25	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)3}$			
2N7580T1					0.019	Ω
2N7582T1					0.037	Ω
2N7584T1					0.061	Ω
2N7586T1					0.092	Ω
Gate to source voltage (threshold)	3404	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)2}$	1.0		V dc
Low temperature operation		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3404	$V_{DS} \geq V_{GS(TH)3}$, I_D = 1 mA dc	$V_{GS(TH)3}$		5.0	V dc
Subgroup 4						
Forward transconductance	3475	$I_D = I_{D2}$, V_{DD} = 15 V dc (see 4.5.1)	g_{FS}			
2N7580T1				45		S
2N7582T1				49		S
2N7584T1				40		S
2N7586T1				37		S
Gate series resistance	3402	Condition A	R_G			
2N7580T1, 2N7484T1					2	Ω
2N7582T1, 2N7486T1					1	Ω
Electrical measurements		See table I, subgroup 2				
Subgroup 5						
Safe operating area test (high voltage)	3474	V_{DS} = 80 percent of rated V_{DS} (see 1.3), t_P = 10 ms, I_D as specified in figure 4				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B, $I_D = I_{D1}$, V_{GS} = 12 V dc V_{DD} = 50 percent of rated V_{DS}				
On-state gate charge (turn-on and turn-off)			$Q_{G(ON)}$ $Q_{G(OFF)}$			
2N7580T1					170	nC
2N7582T1					230	nC
2N7584T1					240	nC
2N7586T1					220	nC
Gate to source charge (turn-on and turn-off)			Q_{GS1} Q_{GS2}			
2N7580T1					60	nC
2N7582T1					55	nC
2N7584T1					65	nC
2N7586T1					50	nC
Gate to drain charge (turn-on and turn-off)			Q_{GD1} Q_{GD2}			
2N7580T1					80	nC
2N7582T1					90	nC
2N7584T1					60	nC
2N7586T1					70	nC
Reverse recovery time	3473	di/dt = -100 A/μs, $V_{DD} \leq 50$ V $I_D = I_{D1}$	t_{rr}			
2N7580T1					500	ns
2N7582T1					370	ns
2N7584T1					640	ns
2N7586T1					700	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ This test required for the following end-point measurements only:
Group B, subgroups 2 and 3 (JANTXV).
Group B, subgroups 3 and 4 (JANS).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R and F		R and F		
				Min	Max	Min	Max	
Subgroup 1								
Not applicable								
Subgroup 2		T_C = + 25°C						
Steady-state total dose irradiation (V_{GS} bias) 4/	1019	V_{GS} = 12 V; V_{DS} = 0						
Steady-state total dose irradiation (V_{DS} bias) 4/	1019	V_{GS} = 0; V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)						
End-point electricals:								
Breakdown voltage, drain to source	3407	Bias condition C, V_{GS} = 0; I_D = 1 mA	$V_{(BR)DSS}$					
2N7580T1				100		100		V dc
2N7582T1				150		150		V dc
2N7584T1				200		200		V dc
2N7586T1				250		250		V dc
Gate to source voltage (threshold)	3404	$V_{DS} \geq V_{GS}$ I_D = 1 mA	$V_{GS(th)1}$	2.0	4.0	2.0	4.0	V dc
Gate current	3411	Bias condition C, V_{GS} = +20 V; V_{DS} = 0	I_{GSSF1}		100		100	nA dc
Gate current	3411	Bias condition C, V_{GS} = -20 V; V_{DS} = 0	I_{GSSR1}		-100		-100	nA dc
Drain current	3413	Bias condition C, V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)	I_{DSS}		10		10	µA dc
Static drain to source on-state voltage	3405	V_{GS} = 12 V; I_D = I_{D2} condition A, pulsed (see 4.5.1)	$V_{DS(on)}$					
2N7580T1					0.495		0.495	V dc
2N7582T1					0.836		0.836	V dc
2N7584T1					1.015		1.015	V dc
2N7586T1					1.168		1.168	V dc
Forward voltage source drain diode	4011	Bias condition C, V_{GS} = 0; I_D = I_{D1}	V_{SD}		1.2		1.2	V dc

1/ For sampling plan see MIL-PRF-19500.
2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheets utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
4/ Separate samples shall be pulled for each bias.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	-55°C to +150°C, 500 cycles.	
Hermetic seal Fine leak Gross leak	1071	As applicable.	
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 2 1/			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours.	
Electrical measurements		See table I, subgroup 2 herein.	
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 3			n = 45, c = 0
Switching time test	3472	$I_D = I_{D1}$, V_{GS}= 12 Vdc, R_G = 2.35Ω, V_{DD} = 50 percent rated V_{DS}. Maximum limits: $t_{d(on)}$ = 40 ns; t_r = 125 ns; $t_{d(off)}$ = 85 ns; t_f = 30 ns.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			3 devices c = 0
Barometric pressure 2N7586T1 only	1001	To 70,000 feet.	
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	

See footnotes at end of table.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only - Continued.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
Subgroup 11 SEE 2/ 3/	1080	See MIL-STD-750 method 1080 and 6.2.	3 devices

1/ A separate sample may be pulled for each test condition.

* 2/ Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

* 3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

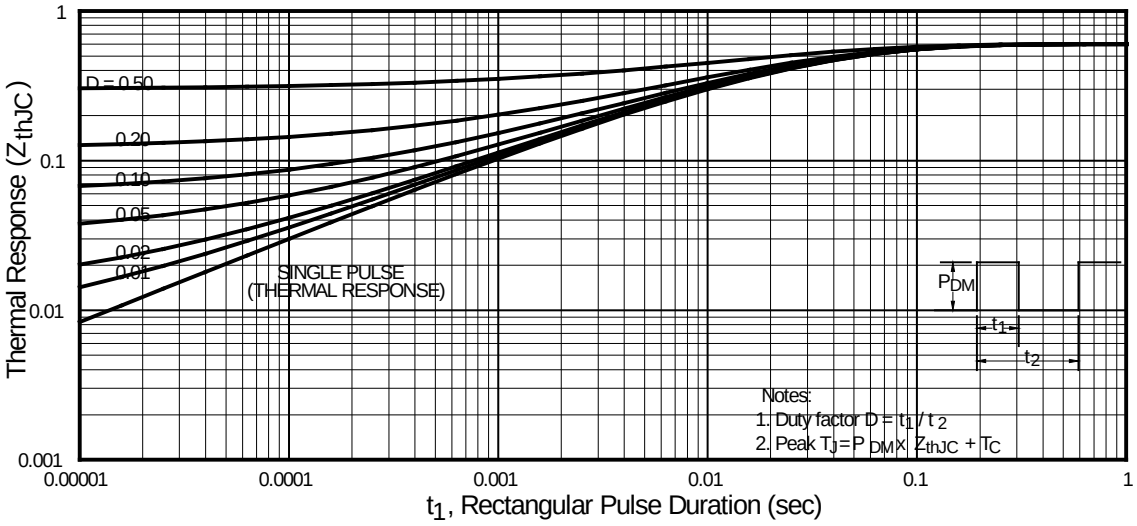


FIGURE 2. Thermal impedance curve.

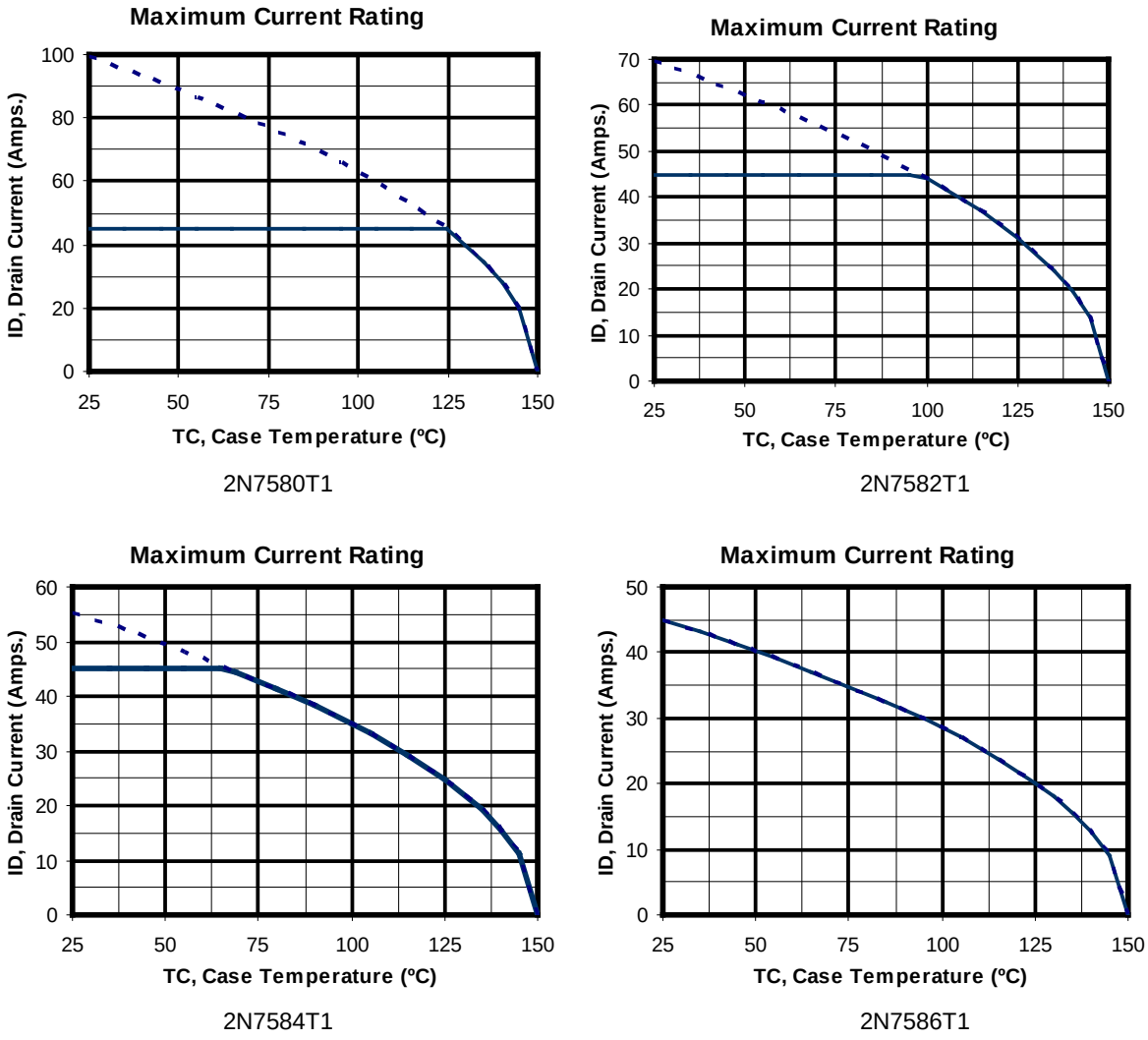
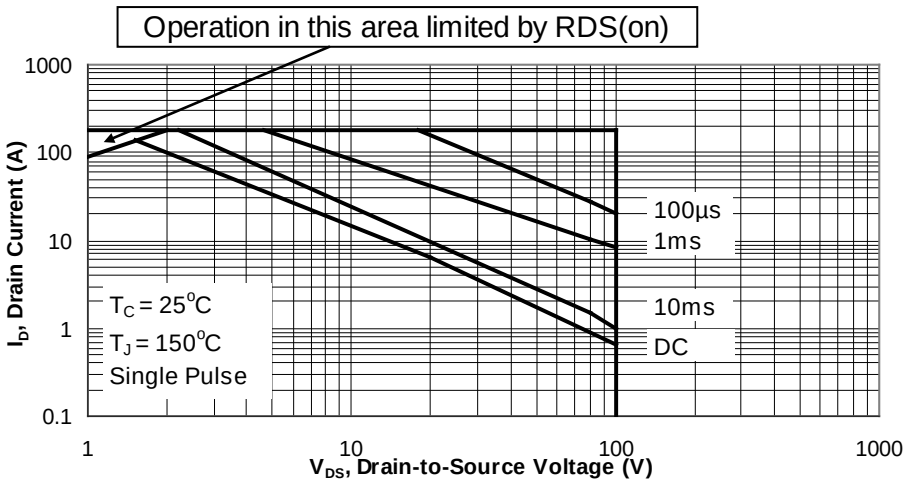


FIGURE 3. Maximum drain current versus case temperature graphs.

2N7580T1



2N7582T1

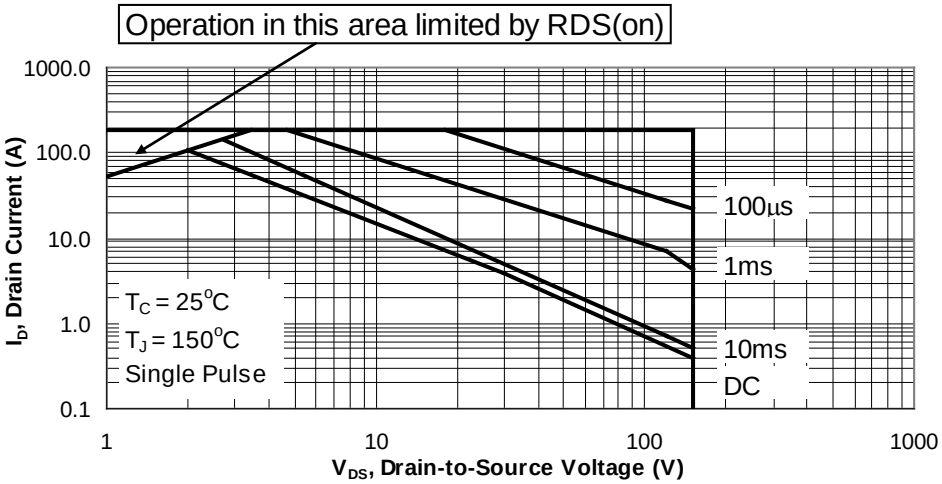
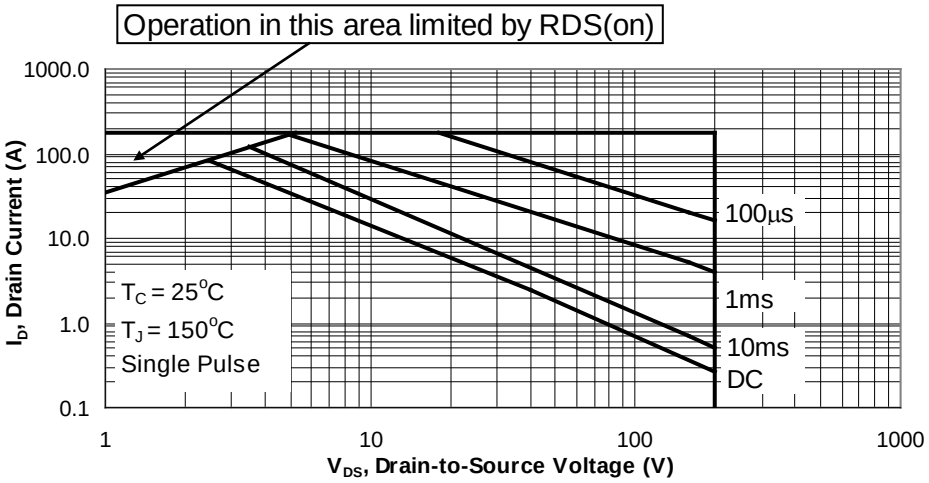


FIGURE 4. Safe operating area graph.

2N7584T1



2N7586T1

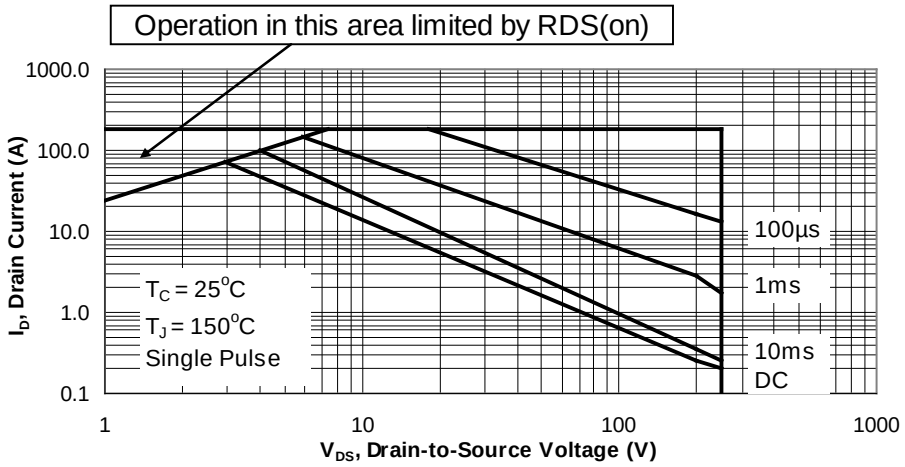
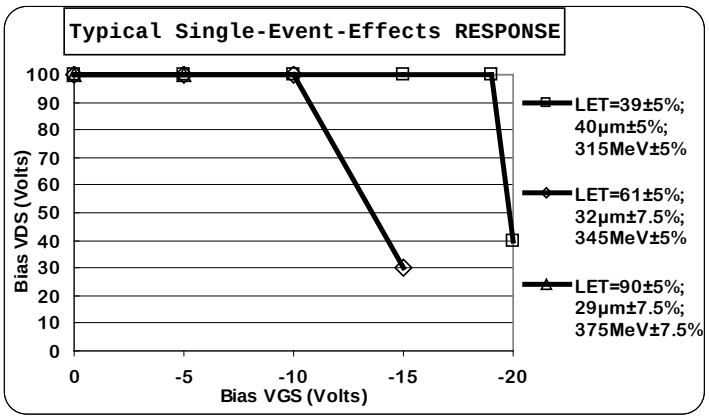
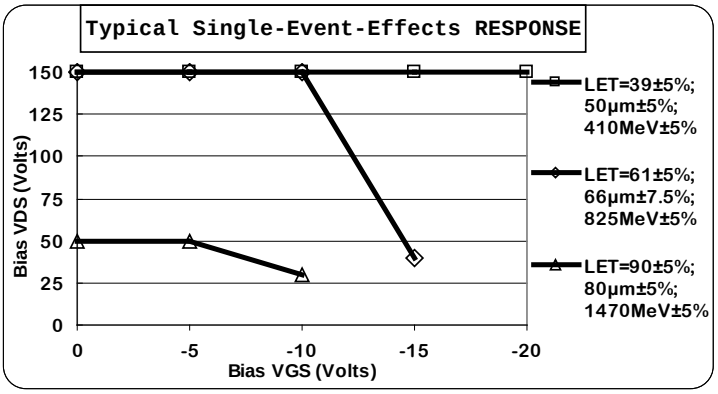


FIGURE 4. Safe operating area graph - Continued.

2N7580T1



2N7582T1



2N7584T1

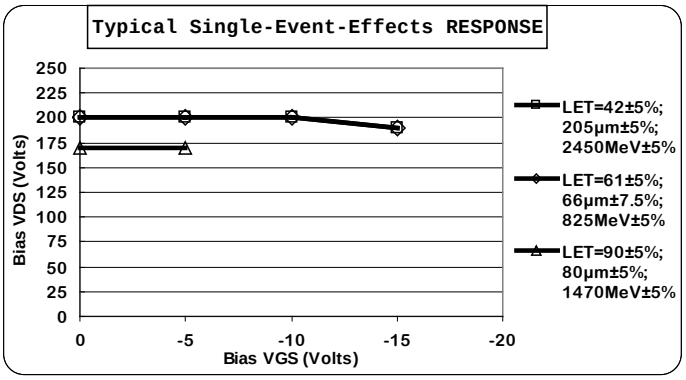


FIGURE 5. Typical SEE safe operating area graph

2N7586T1

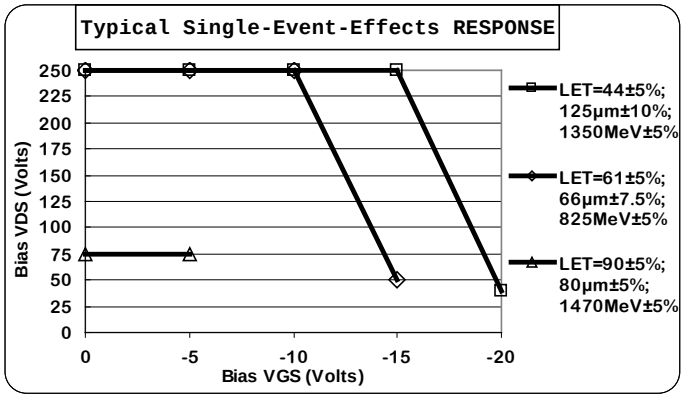


FIGURE 5. Typical SEE safe operating area graph - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

* e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.

* f. If specific SEE characterization conditions are desired (see 6.6 and table IV), manufacturer's cage code should be specified in the contract or order.

* g. If SEE testing data is desired, it should be specified in the contract or order.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil .

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN) (without JAN and RHA prefix). This information in no way implies that manufacturer's PINs are substitutable for the military PIN.

Preferred types military PIN	Commercial PIN
2N7580T1	IRHMS67160
2N7582T1	IRHMS67164
2N7584T1	IRHMS67260
2N7586T1	IRHMS67264

* 6.6 Application data.

* 6.6.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see table IV) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

* TABLE IV. Manufacturers characterization conditions.

Manufactures CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of February 2009 and older)	SEE 1/	1080	See figure 5. IGSSF1, IGSSR1, and IDSS1 in accordance with table I, subgroup 2. Fluence = 3E5 ±20 percent ions/cm2, flux = 2E3 to 2E4 ions/cm2/sec, temperature = +25 ±5°C. Surface LET = 39 MeV-cm2/mg ±5%, range = 40 µm ±7.5%, energy = 315 MeV ±5%. In situ bias conditions: VDS = 100 V and VGS = -19 V, VDS = 40 V and VGS = -20 V, (typical 3.80 MeV/Nucleon at Texas A & M Cyclotron).	3 devices
2N7580T1				
2N7582T1			Surface LET = 39 MeV-cm2/mg ±5%, range = 50 µm ±5%, energy = 410 MeV ±5%. In situ bias conditions: VDS = 150 V and VGS = -20 V, (typical 4.90 MeV/Nucleon at Texas A & M Cyclotron).	
2N7584T1			Surface LET = 42 MeV-cm2/mg ±5%, range = 205 µm ±5%, energy = 2,450 MeV ±5%. In situ bias conditions: VDS = 200 V and VGS = -10 V, VDS = 190 V and VGS = -15 V, (typical 8.49 MeV/Nucleon at Texas A & M Cyclotron).	
2N7586T1			Surface LET = 44 MeV-cm2/mg ±5%, range = 125 µm ±10%, energy = 1,350 MeV ±5%. In situ bias conditions: VDS = 250 V and VGS = -15 V, VDS = 40 V and VGS = -20 V, (typical 10.05 MeV/Nucleon at Texas A & M Cyclotron).	
2N7580T1			Surface LET = 61 MeV-cm2/mg ±5%, range = 32 µm ±7.5%, energy = 345 MeV ±5%. In situ bias conditions: VDS = 100 V and VGS = -10 V, VDS = 30 V and VGS = -15 V, (typical 2.70 MeV/Nucleon at Texas A & M Cyclotron).	
2N7582T1			Surface LET = 61 MeV-cm2/mg ±5%, range = 66 µm ±7.5%, energy = 825 MeV ±5%. In situ bias conditions: VDS = 150 V and VGS = -10 V, VDS = 40 V and VGS = -15 V, (typical 6.40 MeV/Nucleon at Texas A & M Cyclotron).	
	Electrical Measurements		IGSSF1, IGSSR1, and IDSS1 in accordance with table I, subgroup 2.	

See footnotes at end of table.

* TABLE IV. Manufacturers characterization conditions - continued.

Manufactures CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of February 2009 and older)	SEE 1/	1080	See figure 5. IGSSF1, IGSSR1, and IDSS1 in accordance with table I, subgroup 2.	3 devices
2N7584T1			Surface LET = 61 MeV-cm2/mg ±5%, range = 66 µm ±7.5%, energy = 825 MeV ±5%. In situ bias conditions: VDS = 200 V and VGS = -10 V; VDS = 190 V and VGS = -15 V, (typical 6.41 MeV/Nucleon at Texas A & M Cyclotron).	
2N7586T1			Surface LET = 61 MeV-cm2/mg ±5%, range = 66 µm ±7.5%, energy = 825 MeV ±5%. In situ bias conditions: VDS = 250 V and VGS = -10 V; VDS = 50 V and VGS = -15 V, (typical 6.41 MeV/Nucleon at Texas A & M Cyclotron).	
2N7580T1			Surface LET = 90 MeV-cm2/mg ±5%, range = 29 µm ±7.5%, energy = 375 MeV ±7.5%. In situ bias conditions: VDS = 100 V and VGS = -5 V, (typical 1.88 MeV/Nucleon at Texas A & M Cyclotron).	
2N7582T1			Surface LET = 90 MeV-cm2/mg ±5%, range = 80 µm ±5%, energy = 1,470 MeV ±5%. In situ bias conditions: VDS = 50 V and VGS = -5 V; VDS = 30 V and VGS = -10 V, (typical 7.47 MeV/Nucleon at Texas A & M Cyclotron).	
2N7584T1			Surface LET = 90 MeV-cm2/mg ±5%, range = 80 µm ±5%, energy = 1,470 MeV ±5%. In situ bias conditions: VDS = 170 V and VGS = -5V, (typical 7.47 MeV/Nucleon at Texas A & M Cyclotron).	
2N7586T1			Surface LET = 90 MeV-cm2/mg ±5%, range = 80 µm ±5%, energy = 1,470 MeV ±5%. In situ bias conditions: VDS = 75 V and VGS = -5 V, (typical 7.47 MeV/Nucleon at Texas A & M Cyclotron).	
	Electrical measurements		IGSSF1, IGSSR1, and IDSS1 in accordance with table I, subgroup 2.	
Upon qualification, all manufacturers shall provide the verification test conditions to be added to this table.				

1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Review activity:
Air Force - 99

Preparing activity:
DLA - CC

(Project 5961-2013-012)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/ .