The documentation and process conversion measures necessary to comply with this revision shall be completed by 16 January 2015.

INCH-POUND

MIL-PRF-19500/685G
16 October 2014
SUPERSEDING
MIL-PRF-19500/685F
6 May 2013

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, FIELD EFFECT RADIATION HARDENED, N-CHANNEL, SILICON,
DEVICE TYPES 2N7475, 2N7476, AND 2N7477
JANTXVR AND JANSR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for N-Channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistors, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}) for use in particular power-switching applications.. Two levels of product assurance (JANTXV and JANS) are provided for each device type as specified in MIL-PRF-19500. See 6.5 for JANHC and JANKC die versions.

* 1.2 Package outlines. The device package outlines are as follows: TO-254AA in accordance with figure 1 for all encapsulated device types. The dimensions and topography for JANHC and JANKC unencapsulated die are as listed in slash sheet MIL-PRF-19500/741.

1.3 Maximum ratings. T_A = +25°C, unless otherwise specified.

Type	P_T (1) T_C = +25°C	P_T T_A = +25°C	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) T_C =+25°C	I_{D2} (3) (4) T_C = +100°C	I_S	I_{DM} (5)	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A (pk)	°C
2N7475T1	208	3.0	0.60	130	130	±20	45	45	45	180	-55
2N7476T1	208	3.0	0.60	200	200	±20	45	29	45	180	to
2N7477T1	208	3.0	0.60	250	250	±20	37	23.5	37	148	+150

(1) Derate linearly 1.67 W/°C for T_C > +25°C.
(2) See figure 2, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D specs. I_D is limited to 45 A by package and device construction:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 3, maximum drain current graph.
(5) I_{DM} = 4 X I_{D1} as defined in note (3).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil . Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil .

* 1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0 mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}	Max $r_{DS(on)}$ (1) V_{GS} = 12V, $I_D = I_{D2}$		E_{AS}
					T_J = +25°C	T_J = +150°C	
	V dc	V dc Min	Max	μA dc	Ω	Ω	mJ
2N7475T1	130	2.5	4.5	10	0.0155	0.033	432
2N7476T1	200	2.5	4.5	10	0.044	0.101	256
2N7477T1	250	2.5	4.5	10	0.061	0.153	258

(1) Pulsed (see 4.5.1).

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

* 1.5.1 JAN brand and quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTXV" and "JANS".

* 1.5.2 JAN brand and quality level designators for unencapsulated devices (die). See 6.2 for unencapsulated devices.

* 1.5.3 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest for JANTXV and JANS quality levels are as follows: "M", "D", "P", "L", and "R".

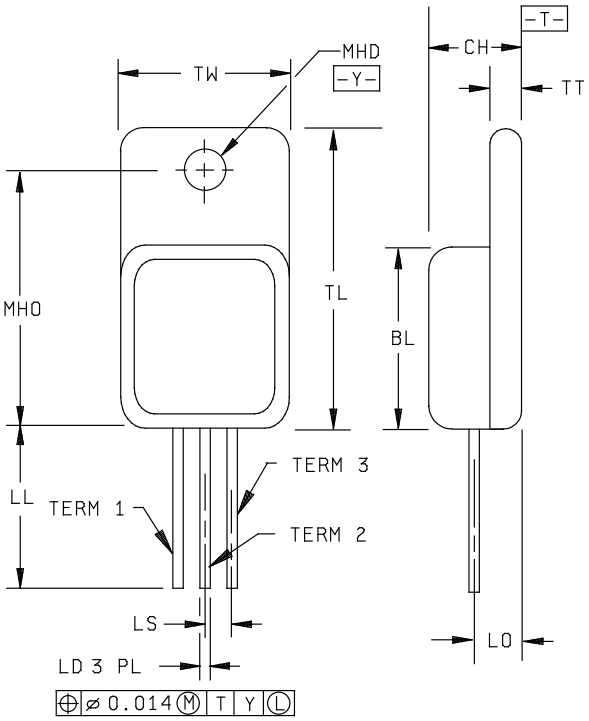
* 1.5.4 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.4.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

* 1.5.4.2 Second number symbols. The second number symbols for the transistor covered by this specification sheet are as follows: "7475", “7476”, and “7477”.

* 1.5.4.3 Suffix letters. The suffix letters "T1" are used on devices that are packaged in the TO-254AA package of figure 1.

* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.570	12.95	14.48	5
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.78	4
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	
TT	.040	.050	1.02	1.27	
TW	.535	.545	13.59	13.84	
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from case.
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
5. Protrusion thickness of ceramic eyelets included in dimension LL.

FIGURE 1. Dimensions and configuration (TO-254AA).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500- Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and figure 1 (TO-254AA) herein. Methods used for electrical isolation of the terminals shall employ materials that contain a minimum of 90 percent Al_2O_3 (ceramic).

3.4.1 Lead formation and finish. Lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500 and herein. Where a choice of finish is desired, it shall be specified in the acquisition document (see 6.2). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of MIL-PRF-19500 and 100 percent dc testing in accordance with table I, subgroup 2 herein.

3.4.2 Internal construction. Multiple chip construction shall not be permitted.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking of the country of origin may be omitted from the body, but shall be retained on the initial container.

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.6).

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, R $\leq$ or 100 kΩ, whenever bias voltage is applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.8 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

* 4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 SEE. SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with table II. SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

* 4.3 Screening (JANS and JANTXV). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS	JANTXV
(3)	Gate stress test (see 4.3.1).	Gate stress test (see 4.3.1).
(3)	Method 3470 of MIL-STD-750, (see 4.3.2), E_{AS} test.	Method 3470 of MIL-STD-750, (see 4.3.2), E_{AS} test.
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3).	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3).
9	Subgroup 2 of table I herein I_{DSS1}, I_{GSSF1}, I_{GSSR1}, as a minimum.	Not applicable.
10	Method 1042 of MIL-STD-750, test condition B.	Method 1042 of MIL-STD-750, test condition B.
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein. ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 µA dc or ±100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A.	Method 1042 of MIL-STD-750, test condition A.
* 13	Subgroups 2 and 3 of table I herein. ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 µA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.	Subgroup 2 of table I herein. ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 µA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.
17	Method 1081 of MIL-STD-750 (see 4.3.4). End-points: Subgroup 2 of table I herein.	Method 1081 of MIL-STD-750 (see 4.3.4). End-points: Subgroup 2 of table I herein.

(1) At the end of the test program, I_{GSSF1} I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $V_{GS(th)1}$, and $r_{DS(ON)}$ shall be invoked.
* (3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV level does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = -24 V minimum for t = 250 µs minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current ..... $I_{AS} = I_{D1}$.

b. Gate voltage (V_{GS}) ..... 12 V.

c. Gate to source resistor (R_{GS}) ..... $25\Omega \leq R_{GS} \leq 200\Omega$.

d. Initial case temperature (T_C) ..... +25°C, +10°C, -5°C.

e. Inductance (L)..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

f. Number of pulses to be applied ..... 1 pulse minimum.

g. Supply voltage (V_{DD}) ..... V_{DD} = 50 V dc.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 µs max. See table III, group E, subgroup 4 herein.

4.3.4 Dielectric withstanding voltage.

a. Magnitude of test voltage……900 V dc.

b. Duration of application of test voltage……..15 seconds (min).

c. Points of application of test voltage……All leads to case (bunch connection).

d. Method of connection……Mechanical.

e. Kilovolt-ampere rating of high voltage source……..1,200 V/1.0 mA (min).

f. Maximum leakage current……1.0 mA.

g. Voltage ramp up time……500 V/second.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and as follows.

4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1051	Test condition G, 100 cycles.
B3	2077	SEM.
B4	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated; T_A = +175°C, t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.
B5	2037	Bond strength, test condition D.

* 4.4.2.2 Group B inspection, table E-VIB (JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles.
* B3	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.
B3	2037	Test condition D. All internal bond wires for each device shall be pulled separately.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

Subgroup	Method	Condition
C2	2036	Test condition A; weight = 10 pounds, t = 10 s.
C5	3161	See 4.3.3, $R_{\theta JC}$ = 0.60°C/W.
C6	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

* 4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source	3407	V_{GS} = 0, I_D = 1 mA dc, bias condition C	$V_{(BR)DSS}$			
2N7475T1				130		V dc
2N7476T1				200		V dc
2N7477T1				250		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)1}$	2.5	4.5	V dc
Gate current	3411	V_{GS} = +20 V dc, bias condition C, V_{DS} = 0	I_{GSSF1}		+100	nA dc
Gate current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		-100	nA dc
Drain current	3413	V_{GS} = 0, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS1}		10	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), I_D = I_{D2}	$r_{DS(ON)1}$			
* 2N7475T1					0.0155	Ω
2N7476T1					0.044	Ω
2N7477T1					0.061	Ω
* Forward voltage	4011	V_{GS} = 0, condition A, I_S = rated I_S	V_{SD}			
2N7475T1					1.2	V dc
2N7476T1					1.2	V dc
2N7477T1					1.2	V dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 3						
High temperature operation		$T_C = T_J = +125°C$				
Gate current	3411	$V_{GS} = \pm 20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSS2}		±200	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		25	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)3}$			
2N7475T1					0.029	Ω
2N7476T1					0.088	Ω
2N7477T1					0.134	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)2}$	1.5		V dc
Low temperature operation		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$, I_D = 1 mA dc	$V_{GS(TH)3}$		5.5	V dc
Subgroup 4						
Forward transconductance	3475	$I_D = I_{D2}$, V_{DD} = 15 V dc (see 4.5.1)	g_{FS}			
2N7475T1				36		S
2N7476T1				35		S
2N7477T1				27		S
Switching time test	3472	$I_D = I_{D1}$, V_{GS} = 12 V dc; R_G = 2.35 Ω, V_{DD} = 50 percent of rated V_{DS}				
Turn-on delay time			$t_{D(on)}$		35	ns
Rise time			t_r		125	ns
Turn-off delay time			$t_{D(off)}$		80	ns
Fall time			t_f			
2N7475T1					50	ns
2N7476T1					50	ns
2N7477T1					65	ns

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 5						
Safe operating area test (high voltage)	3474	See figure 4, t_p = 10 ms min. V_{DS} = 80 percent of max. rated V_{DS}				
Electrical measurements		See table I, subgroup 2				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B; $I_D = I_{D1}$				
On-state gate charge			$Q_{G(ON)}$			
2N7475T1					160	nC
2N7476T1					165	nC
2N7477T1					165	nC
Gate to source charge			Q_{GS}			
2N7475T1					55	nC
2N7476T1					45	nC
2N7477T1					45	nC
Gate to drain charge			Q_{GD}			
2N7475T1					75	nC
2N7476T1					75	nC
2N7477T1					75	nC
Reverse recovery time	3473	di/dt = -100 A/µs, $V_{DD} \leq 50$ V $I_D = I_{D1}$	t_{rr}			
2N7475T1					300	ns
2N7476T1					450	ns
2N7477T1					560	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ This test required for the following end-point measurements only:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

* TABLE II. Group D inspection.

Inspection 1/ 2/ 3/ 4/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Unit
				R		R		
	Method	Conditions		Min	Max	Min	Max	
Subgroup 1								
Not applicable								
Subgroup 2		T_C = + 25°C						
Steady-state total dose irradiation (V_{GS} bias) 5/	1019	V_{GS} = 12 V; V_{DS} = 0						
Steady-state total dose irradiation (V_{DS} bias) 5/	1019	V_{GS} = 0; V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)						
End-point electricals:								
Breakdown voltage, drain to source	3407	V_{GS} = 0; I_D = 1 mA; bias condition C	$V_{(BR)DSS}$					
2N7475T1				130		130		V dc
2N7476T1				200		200		V dc
2N7477T1				250		250		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$; I_D = 1 mA	$V_{GS(th)1}$	2.5	4.5	2.0	4.5	V dc
Gate current	3411	V_{GS} = +20 V, V_{DS} = 0; bias condition C	I_{GSSF1}		100		100	nA dc
Gate current	3411	V_{GS} = -20 V, V_{DS} = 0; bias condition C	I_{GSSR1}		-100		-100	nA dc
Drain current	3413	V_{GS} = 0, V_{DS} = 80 percent of rated V_{DS} (pre-irradiation); bias condition C	I_{DSS}		10		10	µA dc
Static drain to source on-state voltage	3405	V_{GS} = 12 V; condition A, pulsed (see 4.5.1)	$V_{DS(on)}$					
2N7475T1		I_D = 45 A dc			0.630		0.630	V dc
2N7476T1		I_D = 35 A dc			1.715		1.715	V dc
2N7477T1		I_D = 23.5 A dc			1.434		1.434	V dc
* Forward voltage source drain diode	4011	V_{GS} = 0, $I_D = I_{D1}$, condition A	V_{SD}					
2N7475T1		I_S = 45 A dc			1.2		1.2	V dc
2N7476T1		I_S = 45 A dc			1.2		1.2	V dc
2N7477T1		I_S = 37 A dc			1.2		1.2	V dc

1/ For sampling plan see MIL-PRF-19500.
2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheets utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
4/ The R designation represents devices which pass end-points at 100K rads (Si).
5/ Separate samples shall be pulled for each bias.

TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycle	1051	Condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071	As applicable	
Electrical measurements		See table I, subgroup 2	
Subgroup 2 1/			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500	
Subgroup 5			3 devices c = 0
Barometric pressure 2N7477T1 only	1001	Condition C, $V_{(ISO)} = V_{DS}$; V_{DS} = 250 V dc	
Subgroup 10			
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	22 devices c = 0
Subgroup 11			
SEE 2/ 3/	1080	See MIL-STD-750 method 1080 and 6.2.	3 devices

1/ A separate sample may be pulled for each test condition.
2/ Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

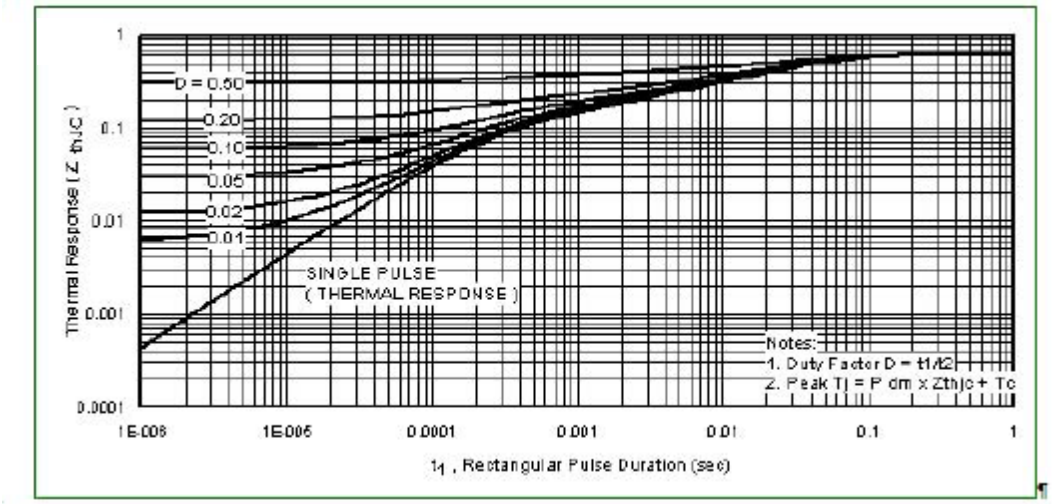
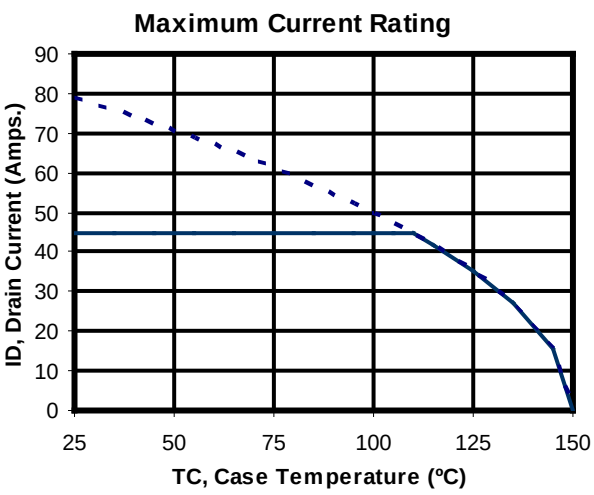
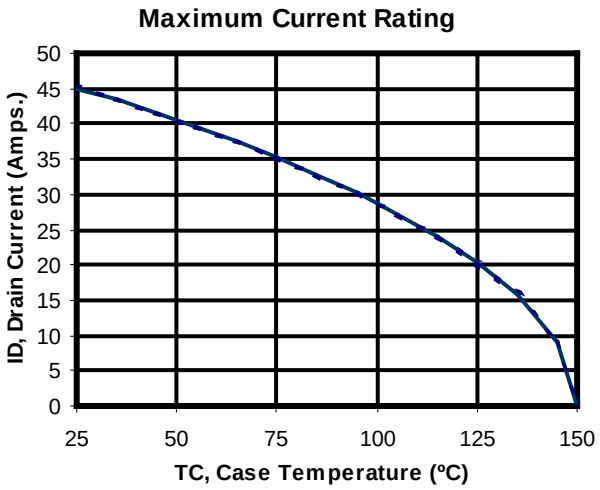


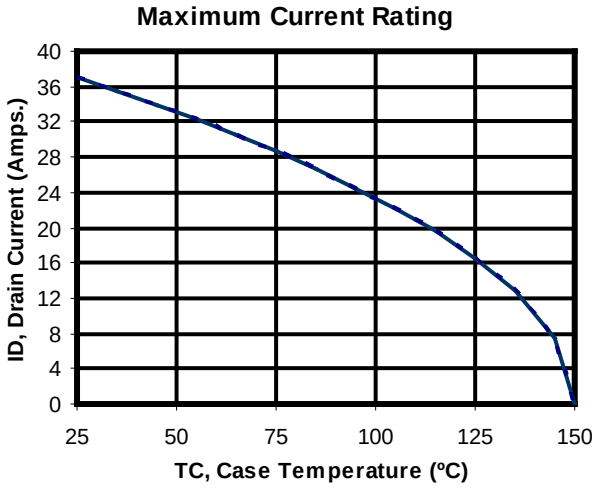
FIGURE 2. Thermal impedance curve.



2N7475T1

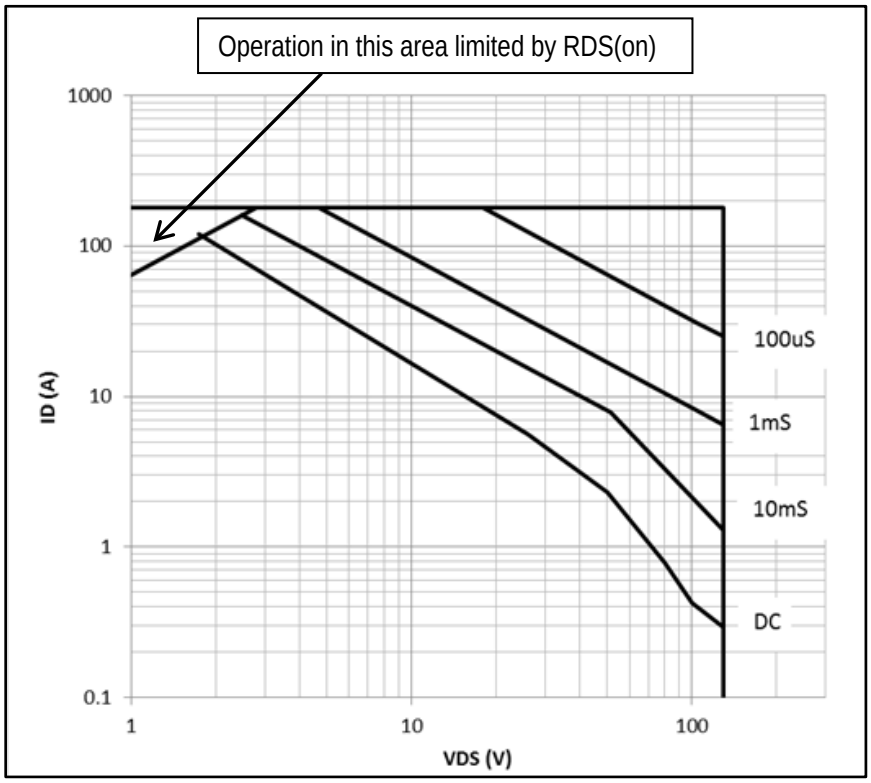


2N7476T1



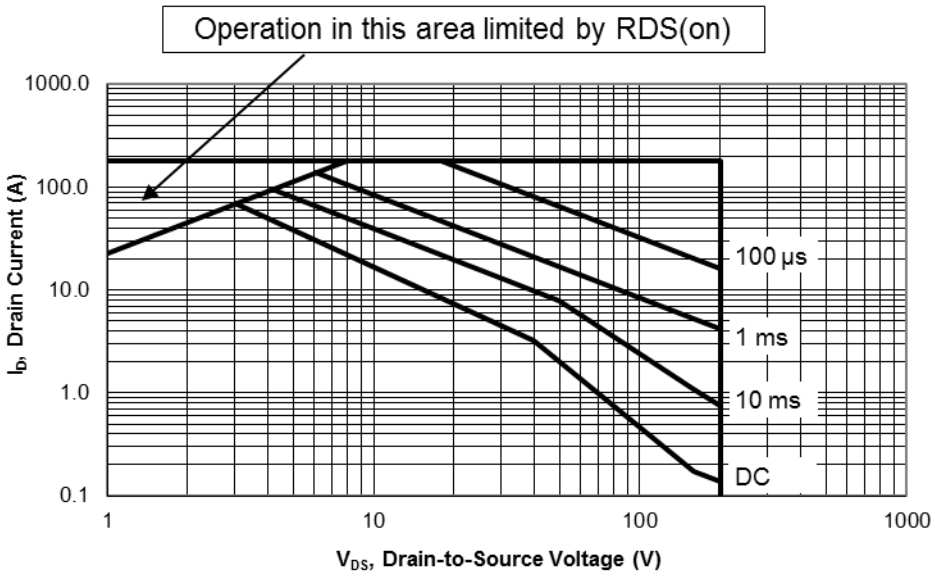
2N7477T1

FIGURE 3. Maximum drain current versus case temperature graphs.

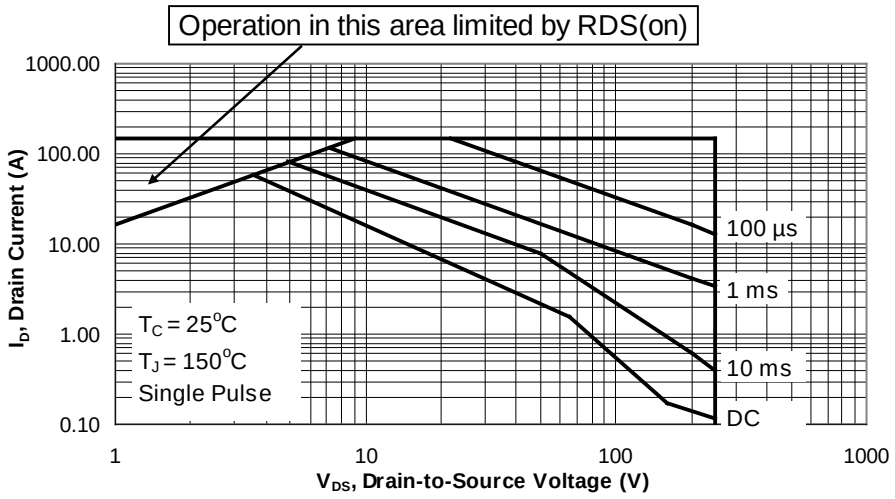


2N7475T1

* FIGURE 4. Safe operating area graphs.



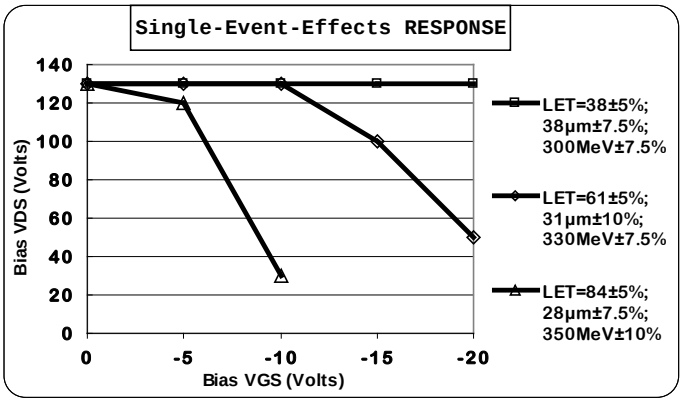
2N7476T1



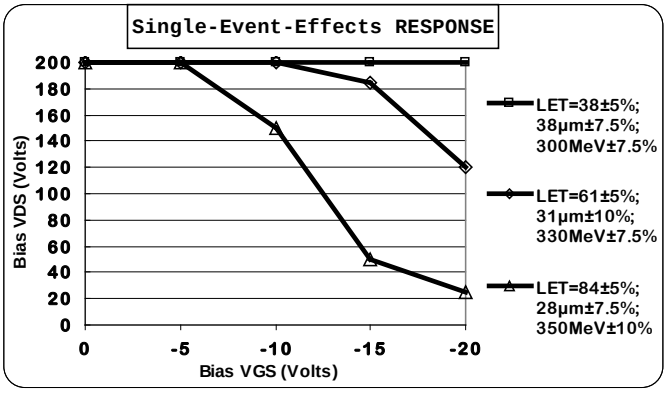
2N7477T1

* FIGURE 4. Safe operating area graphs - Continued.

2N7475T1



2N7476T1



2N7477T1

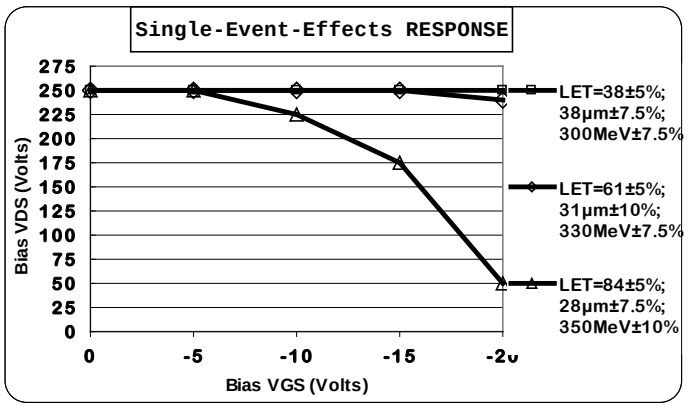


FIGURE 5. Typical SEE safe operating area graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead formation and finish (see 3.4.1).

d. Product assurance level and type designator.

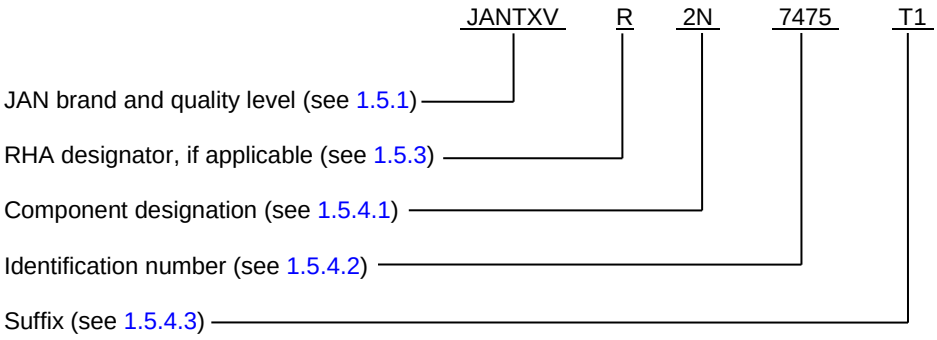
e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.

f. If specific SEE characterization conditions are desired (see 6.8 and table IV), manufacturer's cage code should be specified in the contract or order.

g. If SEE testing data is desired, it should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

* 6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



* 6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7475T1	JANTXV#2N7475T1	JANS2N7475T1	JANS#2N7475T1
JANTXV2N7476T1	JANTXV#2N7476T1	JANS2N7476T1	JANS#2N7476T1
JANTXV2N7477T1	JANTXV#2N7477T1	JANS2N7477T1	JANS#2N7477T1

(1) The number sign (#) represent one of five RHA designators available (M, D, P, L, or R).

6.6 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N
IRHMS57163SE	2N7475T1
IRHMS57260SE	2N7476T1
IRHMS57264SE	2N7477T1

6.7 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/741.

6.8 Application data.

6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see table IV) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

* TABLE IV. Manufacturers characterization conditions.

Manufactures cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of 30 October 2008 and older)	SEE 1/	1080	See MIL-STD-750E method 1080.0 dated 20 November 2006. See figure 5.	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	3 devices
	SEE Irradiation:		Fluence = 3E5 ±20 percent ions/cm^2, flux = 2E3 to 2E4 ions/cm^2/sec, temperature = 25 ±5°C	
			Surface LET = 38 MeV-cm^2/mg ±5% range = 38 µm ±7.5%, energy = 300 MeV ±7.5%	
	2N7475T1		In situ bias conditions: V_{DS} = 130 V and V_{GS} = -20 V, (typical 3.75 MeV/nucleon at Texas A & M Cyclotron)	
	2N7476T1		In situ bias conditions: V_{DS} = 200 V and V_{GS} = -20 V, (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7477T1		In situ bias conditions: V_{DS} = 250 V and V_{GS} = -20 V, (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator)	
			Surface LET = 61 MeV-cm^2/mg ±5%, range = 31 µm ±10%, energy = 330 MeV ±7.5%	
	2N7475T1		In situ bias conditions: V_{DS} = 130 V and V_{GS} = -10 V, V_{DS} = 100 V and V_{GS} = -15 V, V_{DS} = 50 V and V_{GS} = -20 V, (typical 2.70 MeV/nucleon at Texas A & M Cyclotron)	
	2N7476T1		In situ bias conditions: V_{DS} = 200 V and V_{GS} = -10 V, V_{DS} = 185 V and V_{GS} = -15 V, V_{DS} = 120 V and V_{GS} = -20 V, (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7477T1		In situ bias conditions: V_{DS} = 250 V and V_{GS} = -15 V, V_{DS} = 240 V and V_{GS} = -20 V, (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator)	

See footnotes at end of table.

* TABLE IV. Manufacturers characterization conditions – Continued.

Manufactures cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
			Surface LET = 84 MeV-cm^2/mg ±5%, range = 28 µm ±7.5%, energy = 350 MeV ±7.5%	
	2N7475T1		In situ bias conditions: V_{DS} = 130 V and V_{GS} = 0 V, V_{DS} = 120 V and V_{GS} = -5 V, V_{DS} = 30 V and V_{GS} = -10 V, (typical 1.89 MeV/nucleon at Texas A & M Cyclotron)	
*	2N7476T1		In situ bias conditions: V_{DS} = 200 V and V_{GS} = -5V, V_{DS} = 150 V and V_{GS} = -10 V, V_{DS} = 50 V and V_{GS} = -15 V, V_{DS} = 25 V and V_{GS} = -20 V, (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7477T1		In situ bias conditions: V_{DS} = 250 V and V_{GS} = -5V, V_{DS} = 225 V and V_{GS} = -10 V, V_{DS} = 175 V and V_{GS} = -15 V, V_{DS} = 50 V and V_{GS} = -20 V, (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator)	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	

Upon qualification, all manufacturers will provide the verification test conditions to be added to this table.

1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

6.9 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Review activity:
Air Force - 99

Preparing activity:
DLA - CC

(Project 5961-2014-140)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/ .