

N-Channel JFET Monolithic Dual



SST440 / SST441

FEATURES

- High Gain $g_{fs} > 6 \text{ mS}$ typical
- Low Leakage $I_g < 1 \text{ pA}$ typical
- Low Noise
- Surface Mount Package

APPLICATIONS

- Differential Wideband Amplifiers
- VHF/UHF Amplifiers
- Test and Measurement

DESCRIPTION

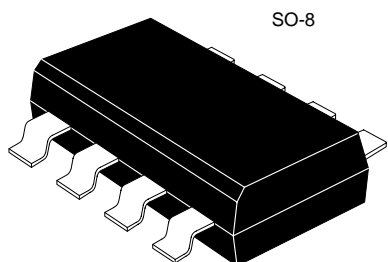
Calogic's SST440 Series is a high speed N-Channel Monolithic Dual JFET in a surface mount SO-8 package. This device is well suited for use as wideband differential amplifiers in test and measurement applications. The combination of high gain, low leakage and low noise make it an excellent performer.

ORDERING INFORMATION

Part	Package	Temperature Range
SST440-1	Plastic SO-8	-55°C to +150°C

NOTE: For Sorted Chips in Carriers, See U440 Series

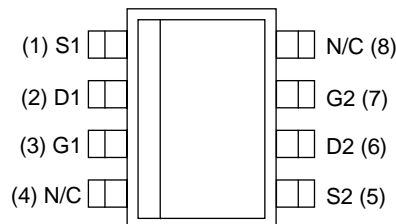
PIN CONFIGURATION



SO-8

CJ1

TOP VIEW



PRODUCT MARKING

SST440	SST440
SST441	SST441

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter/Test Condition	Symbol	Limit	Unit
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	V
Forward Gate Current	I_G	50	mA
Power Dissipation (per side)	P_D	300	mW
(total)		500	mW
Power Derating (per side)		2.4	mW/ $^\circ\text{C}$
(total)		4	mW/ $^\circ\text{C}$
Operating Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to 150	$^\circ\text{C}$
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

SYMBOL	CHARACTERISTICS	TYP ¹	SST440		SST441		UNIT	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
STATIC								
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	-35	-25		-25		V	$I_G = -1\mu\text{A}, V_{DS} = 0\text{V}$
$V_{GS(OFF)}$	Gate-Source Cut off Voltage	-3.5	-1	-6	-1	-6		$V_{DS} = 10\text{V}, I_D = 1\text{nA}$
I_{DSS}	Saturation Drain Current ²	15	6	30	6	30	mA	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}$
I_{GSS}	Gate Reverse Current	-1		-500		-500	pA	$V_{GS} = -15\text{V}, V_{DS} = 0\text{V}$
		-0.2					nA	$T_A = 125^\circ\text{C}$
I_G	Gate Operating Current	-1		-500		-500	pA	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$
		-0.2					nA	$T_A = 125^\circ\text{C}$
$V_{GS(F)}$	Gate-Source Forward Voltage	0.7					V	$I_G = 1\text{mA}, V_{DS} = 0\text{V}$
DYNAMIC								
g_{fs}	Common-Source Forward Transconductance	6	4.5	9	4.5	9	mS	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$ $f = 1\text{kHz}$
g_{os}	Common-Source Output Conductance	20		200		200	μS	
g_{fs}	Common-Source Forward Transconductance	5.5					mS	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$ $f = 100\text{MHz}$
g_{os}	Common-Source Output Conductance	30					μS	
C_{iss}	Common-Source Input Capacitance	3.5					pF	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$ $f = 1\text{MHz}$
C_{rss}	Common-Source Reverse Transfer Capacitance	1						
\bar{e}_n	Equivalent Input Noise Voltage	4					nV/ $\sqrt{\text{Hz}}$	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$ $f = 10\text{kHz}$
MATCHING								
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage	7		10		20	mV	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$
$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Change with Temperature	10					$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$
		10						
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.98						$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}$
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.98						$V_{DG} = 10\text{V}, I_D = 5\text{mA}$ $f = 1\text{kHz}$
CMRR	Common Mode Rejection Ratio	90					dB	$V_{DD} = 5\text{ to }10\text{V}, I_D = 5\text{mA}$

NOTES: 1. For design aid only, not subject to production testing.
2. Pulse test; $PW = 300\mu\text{s}$, duty cycle $\leq 3\%$.