

# FAST DMOS FET Switches

## N-Channel Enhancement-Mode



### SST211 / SST213 / SST215

#### FEATURES

- High Speed Switching.....  $t_{d(ON)}$  1ns
- Low Capacitance..... 2.4pF typical
- Low ON Resistance..... 50Ω typical
- High Gain
- Surface Mount Package

#### APPLICATIONS

- Ultra High Speed Analog Switching
- Sample and Hold
- Multiplexers
- High Gain Amplifiers

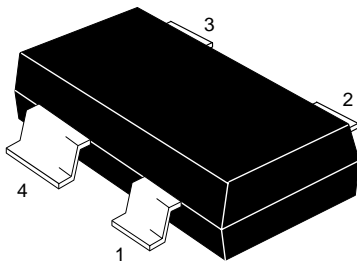
#### DESCRIPTION

Designed for audio, video and high frequency applications, the SST211 Series is a high speed, ultra low capacitance SPST analog switch. Utilizing Calogic's proprietary DMOS processing the SST211 Series features an integrated zener diode designed to protect the gate from electrical over stress.

#### ORDERING INFORMATION

Part	Package	Temperature Range
SST211	SOT-143 Surface Mount	-55°C to +125°C
SST213	SOT-143 Surface Mount	-55°C to +125°C
SST215	SOT-143 Surface Mount	-55°C to +125°C
XSST211	Sorted Chips in Carriers	-55°C to +125°C
XSST213	Sorted Chips in Carriers	-55°C to +125°C
XSST215	Sorted Chips in Carriers	-55°C to +125°C

#### PIN CONFIGURATION

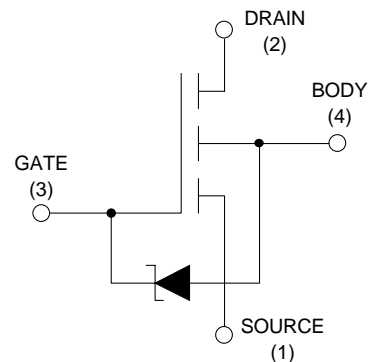


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#### PRODUCT MARKING

PRODUCT MARKING	
SST211	211
SST213	213
SST215	215

#### SCHEMATIC DIAGRAM





**ABSOLUTE MAXIMUM RATINGS** ( $T_c = +25^{\circ}\text{C}$  unless otherwise noted)

Parameter	SST211	SST213	SST215	Unit
<b>Breakdown Voltages</b>				
$V_{DS}$	+30	+10	+20	V
$V_{SD}$	+10	+10	+20	V
$V_{DB}$	+30	+15	+25	V
$V_{SB}$	+15	+15	+25	V
$V_{GS}$	-15	-15	-25	V
	+25	+25	+30	V
$V_{GB}$	-0.3	-0.3	-0.3	V
	+25	+25	+30	V
$V_{GD}$	-30	-15	-25	V
	+25	+25	+30	V

$I_D$  Continous Drain Current . . . . . 50mA       $T_j$  Operating Junction Temperature Range . . -55 to +125°C  
 $P_T$  Power Dissipation (at or below  $T_c = +25^{\circ}\text{C}$ ) . . . . 360mW       $T_s$  Storage Temperature Range . . . . . -55 to +150°C  
 Linear Derating Factor 3.6mW/°

**ELECTRICAL CHARACTERISTICS** ( $T_c = +25^{\circ}\text{C}$  unless otherwise noted)

SYMBOL	CHARACTERISTICS	SST211			SST213			SST215			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
<b>STATIC</b>													
$B_{VDS}$	Drain-Source Breakdown Voltage	30	35								V	$I_D = 10\mu\text{A}, V_{GS} = V_{BS} = 0$	
		10	25		10	25		20	25			$I_D = 10\text{nA}, V_{GS} = V_{BS} = -5\text{V}$	
$B_{VSD}$	Source-Drain Breakdown Voltage	10			10			20				$I_S = 10\text{nA}, V_{GD} = V_{BD} = -5\text{V}$	
$B_{VDB}$	Drain-Body Breakdown Voltage	15			15			25				$I_D = 10\text{nA}, V_{GB} = 0$ Source OPEN	
$B_{VSB}$	Source-Body Breakdown Voltage	15			15			25				$I_S = 10\mu\text{A}, V_{GB} = 0$ Drain OPEN	
$I_{D(OFF)}$	Drain-Source OFF Current		0.2	10		0.2	10				nA	$V_{DS} = 10\text{V}$	
									0.2	10		$V_{GS} = V_{BS} = -5\text{V}$	
$I_{S(OFF)}$	Source-Drain OFF Current		0.6	10		0.6	10					V	$V_{SD} = 10\text{V}$
									0.6	10			$V_{GD} = V_{BD} = -5\text{V}$
$I_{GBS}$	Gate-Body Leakage Current			10			10				μA	$V_{GB} = 25\text{V}$	
										10		$V_{DB} = V_{SB} = 0$	
$V_{GS(th)}$	Gate Threshold Voltage	0.5	1.0	2.0	0.1		2.0	0.1	1.0	2.0	V	$V_{DS} = V_{GS}, I_D = 1\mu\text{A}, V_{SB} = 0$	
$r_{ds(on)}$	Drain-Source <sup>1</sup> ON Resistance		50	70		50	70		50	70	ohms	$V_{GS} = 5\text{V}$	
			30	45		30	45		30	45		$V_{GS} = 10\text{V}$	
<b>DYNAMIC</b>													
$g_{fs}$	Common-Source <sup>1</sup> Foward Transcond.	10	12		10	12		10	12		mS	$V_{DS} = 10\text{V}, I_D = 20\text{mA}$ $f = 1\text{KHz}, V_{SB} = 0$	
$C_{(gs + gd + gb)}$	Gate Node Capacitance		2.4	3.5		2.4	3.5		2.4	3.5	pF	$V_{DS} = 10\text{V}$ $V_{GS} = V_{BS} = -15\text{V}$ $f = 1\text{MHz}$	
$C_{(gd + db)}$	Drain Node Capacitance		1.3	1.5		1.3	1.5		1.3	1.5			
$C_{(gs + sb)}$	Source Node Capacitance		3.5	4.0		3.5	4.0		3.5	4.0			
$C_{(dg)}$	Reverse Transfer Capacitance		0.3	0.5		0.3	0.5		0.3	0.5			
$t_{d(ON)}$	Turn ON Delay Time		0.7	1.0		0.7	1.0		0.7	1.0	ns	$V_{DD} = 5\text{V}, V_{G(ON)} = 10\text{V}$ $R_L = 680, R_G = 51$	
$t_r$	Rise Time		0.8	1.0		0.8	1.0		0.8	1.0			
$t_{(OFF)}$	Turn OFF Time		10			10			10				

NOTE 1: Pulse Test, 80 Sec, 1% Duty Cycle  
 Typical Performance Characteristics: See SD211-215 Series