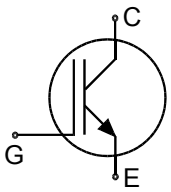
SIGC40T65R3E

IGBT3 Chip

Features:
- 650V Trench & Field Stop technology
- low $V_{CE(sat)}$
- low turn-off losses
- short tail current
- positive temperature coefficient
- easy paralleling
- Qualified according to JEDEC for target applications

Recommended for:
- power modules

Applications:
- drives



Chip Type	V_{CE}	I_{Cn} [1)]	Die Size	Package
SIGC40T65R3E	650V	75A	5.74 x 6.96 mm^2	sawn on foil

[1)] nominal collector current at Tc = 100°C, not subject to production test - verified by design/characterization

Mechanical Parameters

Die size		5.74 x 6.96	mm^2
Emitter pad size (incl. gate pad)		See chip drawing	
Gate pad size		1.615 x 0.817	
Area total		39.95	
Thickness		70	µm
Wafer size		200	mm
Max.possible chips per wafer		666	
Passivation frontside		Photoimide	
Pad metal		3200 nm AlSiCu	
Backside metal		Ni Ag –system	
Die bond		Electrically conductive epoxy glue and soft solder	
Wire bond		Al, <500µm	
Reject ink dot size		∅ 0.65mm ; max 1.2mm	
Storage environment	for original and sealed MBB bags	Ambient atmosphere air, Temperature 17°C – 25°C, < 6 month	
	for open MBB bags	Acc. to IEC62258-3: Atmosphere >99% Nitrogen or inert gas, Humidity <25%RH, Temperature 17°C – 25°C, < 6 month	

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Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-Emitter voltage, T_{vj} =25 °C	V_{CE}	650	V
DC collector current, limited by $T_{vj\,max}$	I_C	1)	A
Pulsed collector current, t_p limited by $T_{vj\,max}$ 2)	$I_{c,puls}$	225	A
Gate emitter voltage	V_{GE}	±20	V
Operating junction temperature	T_{vj}	-40 ... +175	°C
Short circuit data 2)3) V_{GE} = 15V, V_{CC} = 360V, T_{vj} = 150°C	t_{SC}	6	µs

1) depending on thermal properties of assembly

2) not subject to production test - verified by design/characterization

3) allowed number of short circuits: <1000; time between short circuits: >1s.

Static Characteristics (tested on wafer), T_{vj} =25 °C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-Emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V , I_C=4 mA	650			V
Collector-Emitter saturation voltage	V_{CEsat}	V_{GE}=15V, I_C=75A	0.93	1.45	1.77	
Gate-Emitter threshold voltage	$V_{GE(th)}$	I_C=1.2mA , V_{GE}=V_{CE}	5.1	5.8	6.4	
Zero gate voltage collector current	I_{CES}	V_{CE}=650V , V_{GE}=0V			3.8	µA
Gate-Emitter leakage current	I_{GES}	V_{CE}=0V , V_{GE}=20V			600	nA
Integrated gate resistor	r_G			4		Ω

Electrical Characteristics (not subject to production test - verified by design / characterization)

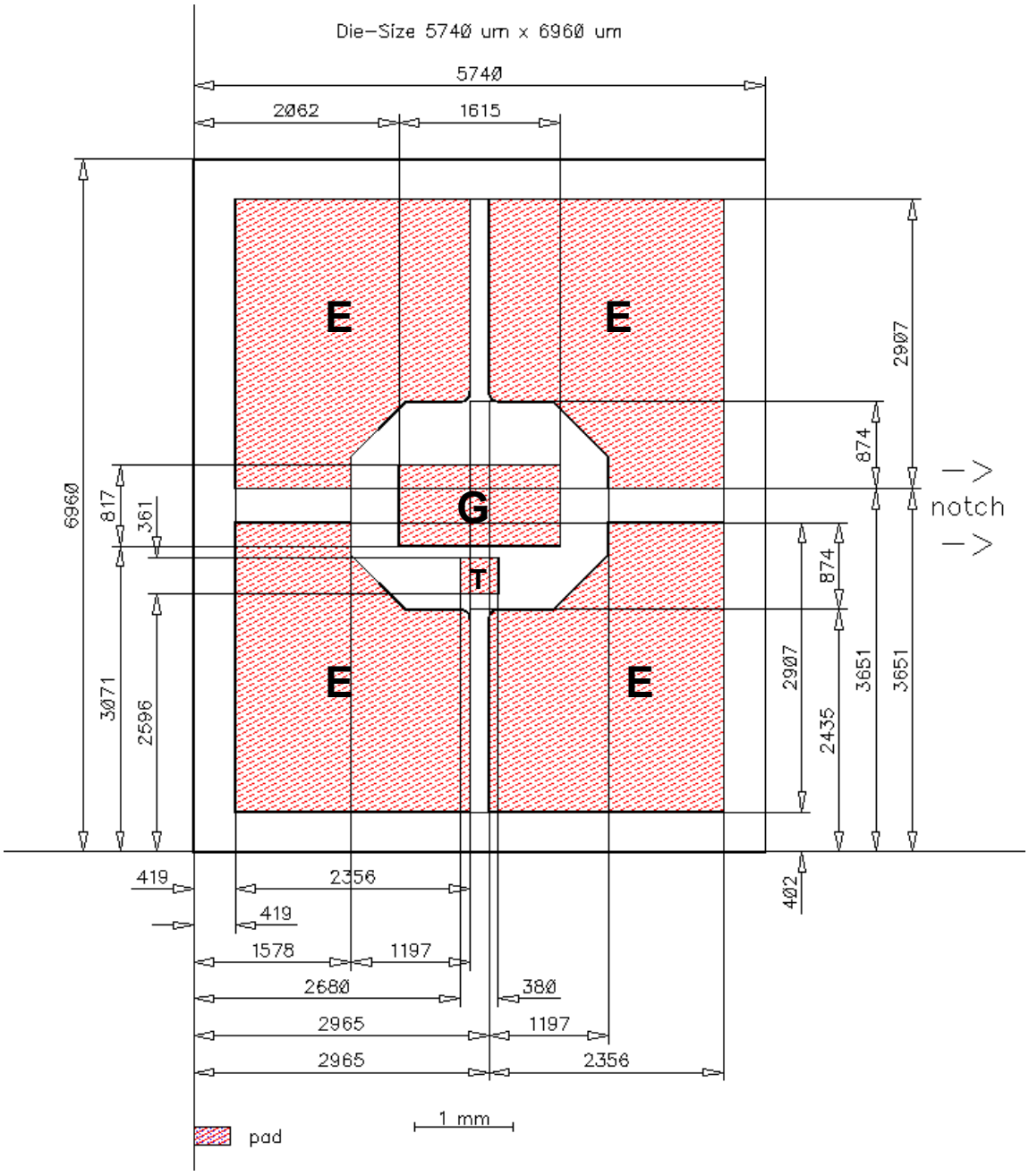
Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-Emitter saturation voltage	V_{CEsat}	V_{GE}=15V, I_C=75A, T_{vj} =175 °C		tbd		V
Input capacitance	C_{ies}	V_{CE}=25V, V_{GE}=0V, f=1MHz T_{vj} =25 °C		4620		pF
Reverse transfer capacitance	C_{res}			137		

Further Electrical Characteristic

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

This chip data sheet refers to the device data sheet	tbd	tbd

Chip Drawing



E = Emitter
G = Gate
T = Test pad do not contact

SIGC40T65R3E

Description

AQL 0,65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

Revision History

Version	Subjects (major changes since last revision)	Date

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