

## IGBT4 Low Power Chip

### Features:

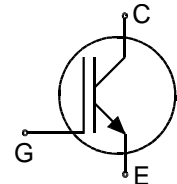
- 1200V Trench & Field stop technology
- low switching losses
- positive temperature coefficient
- easy paralleling
- Qualified according to JEDEC for target applications

### Recommended for:

- low / medium power modules

### Applications:

- low / medium power drives



Chip Type	V <sub>CE</sub>	I <sub>Cn</sub> <sup>1)</sup>	Die Size	Package
IGC50T120T8RL	1200V	50A	7.25 x 6.84 mm <sup>2</sup>	sawn on foil

<sup>1)</sup> nominal collector current at T<sub>c</sub> = 100°C, not subject to production test - verified by design/characterization

### Mechanical Parameters

Die size	7.25 x 6.84	mm <sup>2</sup>
Emitter pad size (incl. gate pad)	See chip drawing	
Gate pad size	0.811 x 1.31	
Area total	49.6	
Thickness	115	µm
Wafer size	200	mm
Max.possible chips per wafer	531	
Passivation frontside	Photoimide	
Pad metal	3200 nm AlSiCu	
Backside metal	Ni Ag –system To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process	
Die bond	Electrically conductive epoxy glue and soft solder	
Wire bond	Al, <500µm	
Reject ink dot size	Ø 0.65mm ; max 1.2mm	
Storage environment	for original and sealed MBB bags	Ambient atmosphere air, Temperature 17°C – 25°C, < 6 month
	for open MBB bags	Acc. to IEC62258-3: Atmosphere >99% Nitrogen or inert gas, Humidity <25%RH, Temperature 17°C – 25°C, < 6 month



# IGC50T120T8RL

## Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-Emitter voltage, $T_{vj} = 25\text{ °C}$	$V_{CE}$	1200	V
DC collector current, limited by $T_{vj\text{ max}}$	$I_C$	<sup>1)</sup>	A
Pulsed collector current, $t_p$ limited by $T_{vj\text{ max}}$ <sup>2)</sup>	$I_{C,puls}$	150	A
Gate emitter voltage	$V_{GE}$	$\pm 20$	V
Operating junction temperature	$T_{vj}$	-40 ... +175	°C
Short circuit data <sup>2)3)</sup> $V_{GE} = 15V, V_{CC} = 800V, T_{vj} = 150\text{ °C}$	$t_{SC}$	10	$\mu s$

<sup>1)</sup> depending on thermal properties of assembly

<sup>2)</sup> not subject to production test - verified by design/characterization

<sup>3)</sup> allowed number of short circuits: <1000; time between short circuits: >1s.

## Static Characteristics (tested on wafer), $T_{vj} = 25\text{ °C}$

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-Emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0V, I_C=1.7\text{ mA}$	1200			V
Collector-Emitter saturation voltage	$V_{CEsat}$	$V_{GE}=15V, I_C=50A$	1.58	1.85	2.07	
Gate-Emitter threshold voltage	$V_{GE(th)}$	$I_C=1.7mA, V_{GE}=V_{CE}$	5.3	5.8	6.3	
Zero gate voltage collector current	$I_{CES}$	$V_{CE}=1200V, V_{GE}=0V$			1	$\mu A$
Gate-Emitter leakage current	$I_{GES}$	$V_{CE}=0V, V_{GE}=20V$			120	nA
Integrated gate resistor	$r_G$			4		$\Omega$

## Electrical Characteristics (not subject to production test - verified by design / characterization)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-Emitter saturation voltage	$V_{CEsat}$	$V_{GE}=15V, I_C=50A,$ $T_{vj}=150\text{ °C}$		2.25		V
Input capacitance	$C_{ies}$	$V_{CE}=25V,$ $V_{GE}=0V, f=1MHz$		2800		pF
Reverse transfer capacitance	$C_{res}$	$T_{vj}=25\text{ °C}$		100		



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## Further Electrical Characteristic

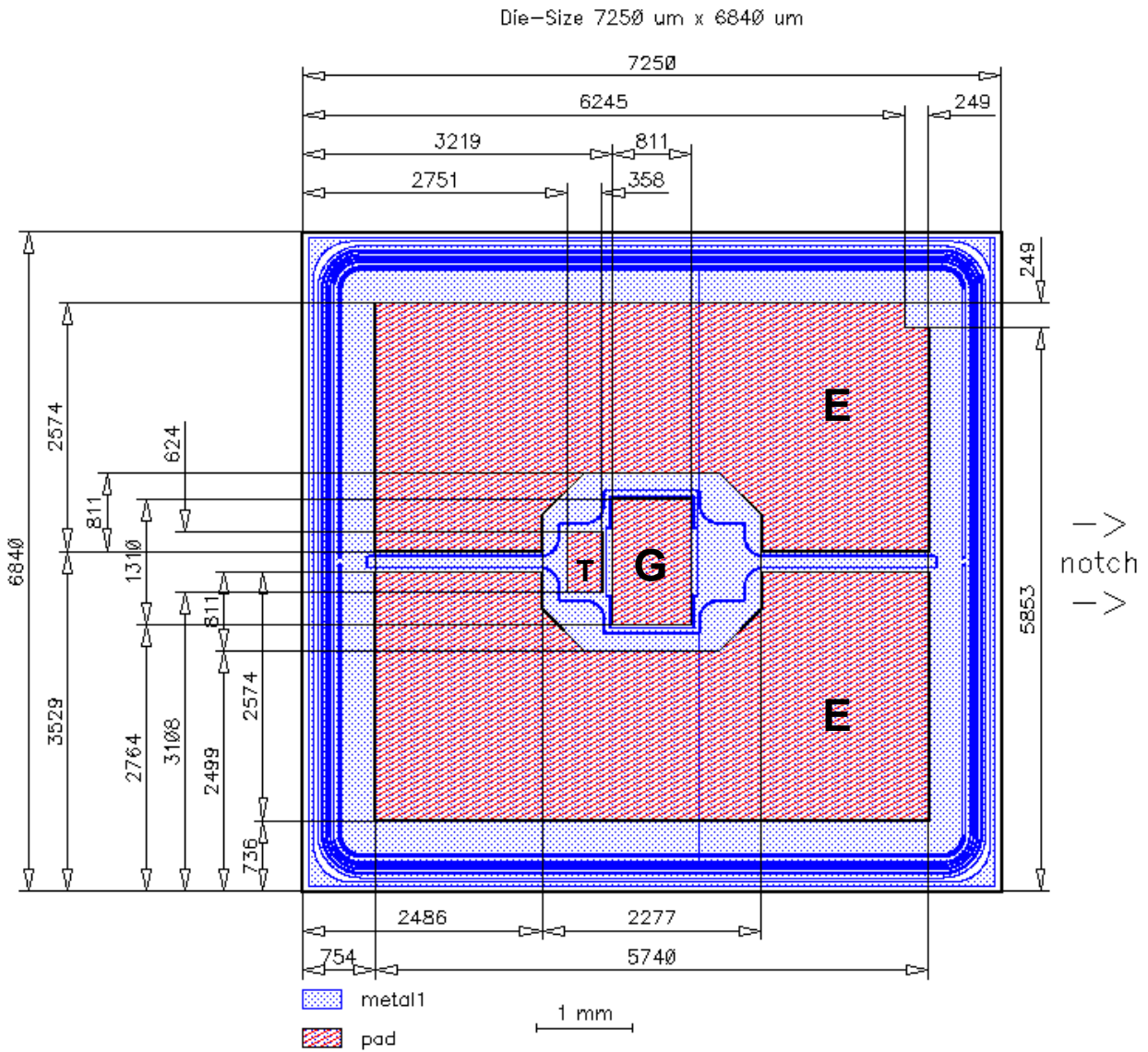
Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

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This chip data sheet refers to the device data sheet	FP50R12KT4_B11	Rev. 3.0
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## Chip Drawing



**E** = Emitter  
**G** = Gate  
**T** = Test pad do not contact



# IGC50T120T8RL

## Description

AQL 0,65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

## Revision History

Version	Subjects (major changes since last revision)	Date

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