TS820-600T(800T)G

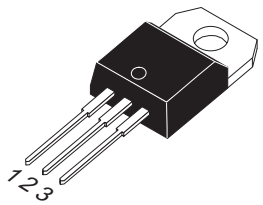
SCRs

Description

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

Simplified outline

TO-220AB



Symbol

Features

- Blocking voltage to 800 V
- On-state RMS current to 8 A
- Ultra low gate trigger current

Applications

- Motor control
- Industrial and domestic lighting
- Heating
- Static switching

Pin	Description
1	cathode
2	anode
3	gate
TAB	anode

SYMBOL	PARAMETER		Value	Unit
V_{DRM}	Repetitive peak off-state voltages	600TG 800TG	600 800	V
$I_{T\ (RMS)}$	RMS on-state current		8	A
I_{TSM}	Non-repetitive peak on-state current		73	A

SYMBOL	PARAMETER	Value	UNIT
Rth j-c	Junction to case (DC)	20	℃/W
Rth j-a	Junction to ambient (DC)	70	℃/W

Limiting values in accordance with the Maximum system(IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state Voltages	600TG 800TG	-	600 800	V
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	8	A
$I_{T(AV)}$	Average on-state current	Half sine wave;<=111℃	-	5	A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; Tj = 25℃ prior to surge t=10ms	-	70	A
		t=8.3ms	-	73	A
I^2t	I^2t for fusing	T=10ms Tj=25℃	-	24.5	A^2S
DI_T/dt	Critical rate of rise of on-state current	I_G=2*I_{GT}, tr≤100ns F=60Hz Tj=125℃	-	50	A/μs
I_{GM}	Peak gate current	Tp=20μs Tj=125℃	-	4	A
V_{RGM}	Peak reverse gate voltage		-	5	V
P_{GM}	Peak gate power		-	5	W
$P_{G(AV)}$	Average gate power	Over any 20 ms period	-	1	W
T_{stg}	Storage temperature		-40	150	℃
T_j	Operating junction Temperature		-	125^2	℃

T_J =25°C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Static characteristics						
I_{GT}	Gate trigger current	V_D=12V; R_L=140Ω	-	-	200	μA
V_{GT}	Gate trigger voltage	V_D=12V; R_L=140Ω	-	-	0.8	V
V_{GD}		V_D=V_{DRM}; R_L=3.3KΩ R_{GK}=220Ω Tj=125℃	-	-	0.1	V
I_L	Latching current	I_G=1mA,R_{GK}=1kΩ	-	-	6	mA
I_H	Holding current	IT=50mA,R_{GK}=1kΩ	-	-	5	mA
V_{TO}	Threshold voltage	Tj=125℃	-	-	0.85	V
Rd	Dynamic resistance	T_J=125℃	-	-	46	mΩ

Dynamic Characteristics

D_V/dt	Critical rate of rise of Off-state voltage	V_D=65% V_{DRM};R_{GK}=220Ω; T_J=125℃	5	-	-	V/μs
V_{RG}		I_{RG}=10μA	8	-	-	V
V_{TM}		I_{TM}=16A tp=380μS	-	-	1.6	V

Description

Fig. 1: Maximum average power dissipation versus average on-state current.

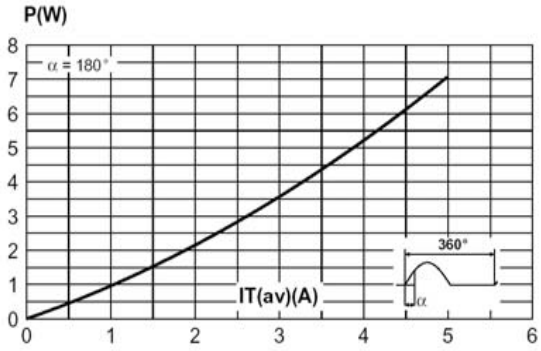


Fig. 2-1: Average and D.C. on-state current versus case temperature.

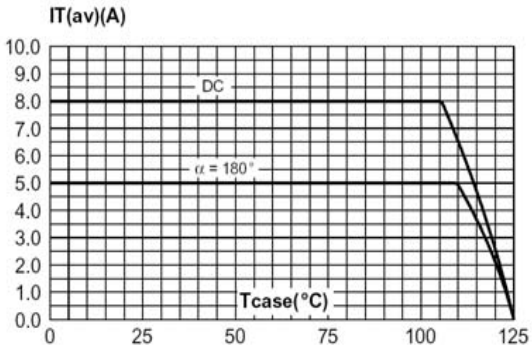


Fig. 2-2: Average and D.C. on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout) (DPAK).

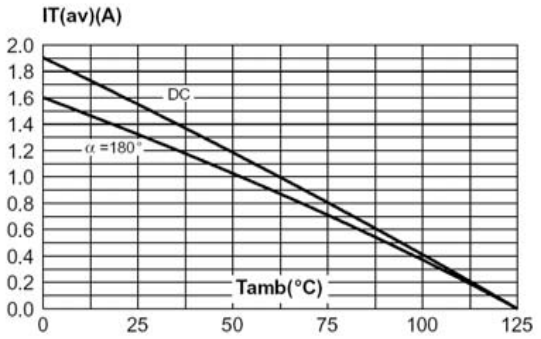


Fig. 3-1: Relative variation of thermal impedance junction to case versus pulse duration.

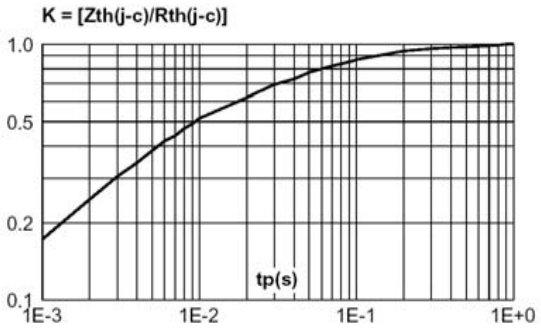


Fig. 3-2: Relative variation of thermal impedance junction to ambient versus pulse duration (recommended pad layout, FR4 PC board for DPAK).

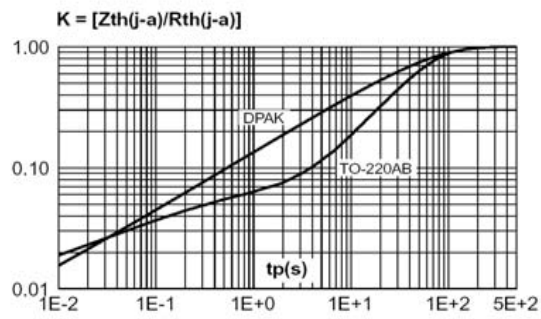
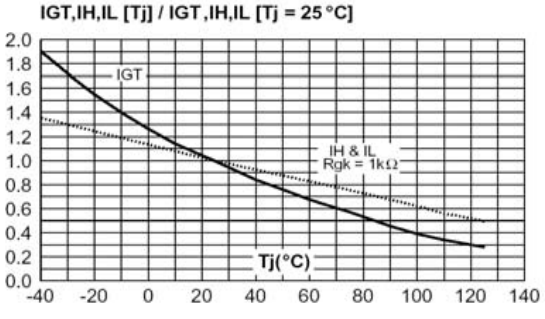


Fig. 4-1: Relative variation of gate trigger current and holding current versus junction temperature for TS8 series.



Description

Fig. 4-2: Relative variation of gate trigger current and holding current versus junction temperature for TN8 & TYN series.

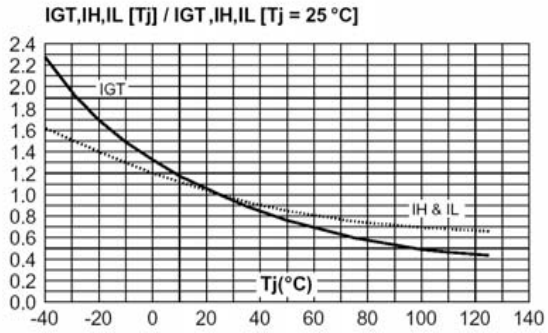


Fig. 5: Relative variation of holding current versus gate-cathode resistance (typical values) for TS8 series.

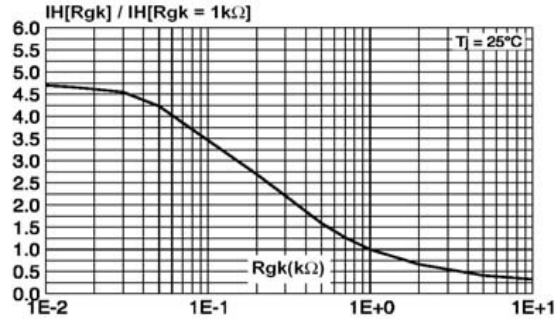


Fig. 6: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values) for TS8 series.

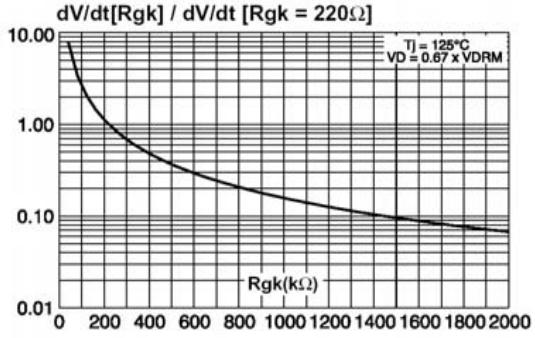


Fig. 7: Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values) for TS8 series.

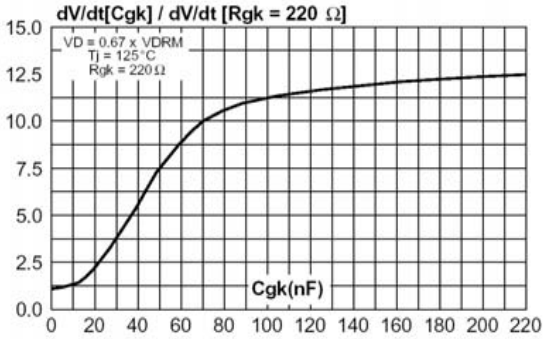


Fig. 8: Surge peak on-state current versus number of cycles. TS8/TN8/TYN.

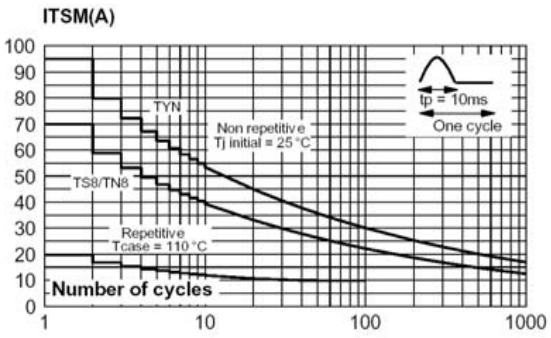
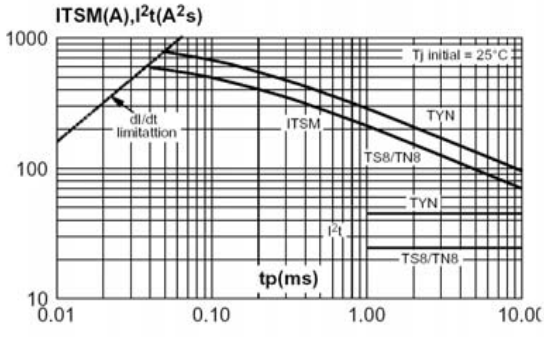
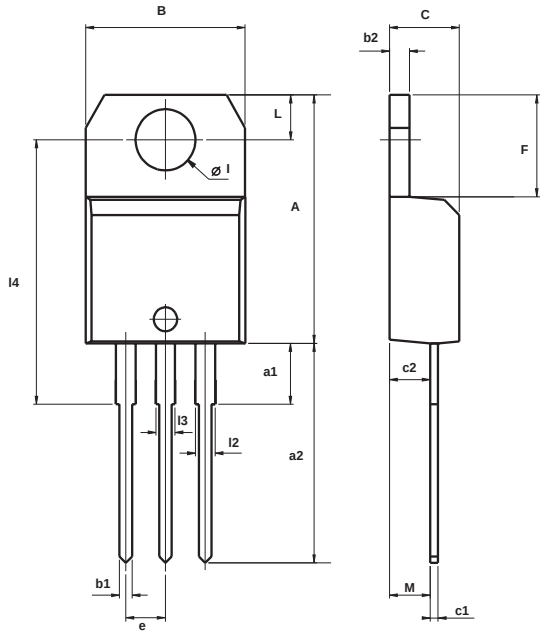


Fig. 9: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10 ms, and corresponding values of I^2t.



Package Mechanical Data

TO-220AB (Plastic)



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	15.20		15.90	0.598		0.625
a1		3.75			0.147	
a2	13.00		14.00	0.511		0.551
B	10.00		10.40	0.393		0.409
b1	0.61		0.88	0.024		0.034
b2	1.23		1.32	0.048		0.051
C	4.40		4.60	0.173		0.181
c1	0.49		0.70	0.019		0.027
c2	2.40		2.72	0.094		0.107
e	2.40		2.70	0.094		0.106
F	6.20		6.60	0.244		0.259
I	3.75		3.85	0.147		0.151
I4	15.80	16.40	16.80	0.622	0.646	0.661
L	2.65		2.95	0.104		0.116
I2	1.14		1.70	0.044		0.066
I3	1.14		1.70	0.044		0.066
M		2.60			0.102	