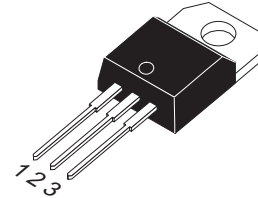


Simplified outline TO-220AB



Description

Standard gate triggering SCR is fully isolated package suitable for the application where requiring high bidirectional blocking voltage capability and also suitable for over voltage protection, motor control circuit in power tool, inrush current limit circuit and heating control system.

Features

- Blocking voltage to 800 V
- On-state RMS current to 12 A
- Ultra low gate trigger current

Symbol



Applications

- Motor control
- Industrial and domestic lighting
- Heating
- Static switching

Pin	Description
1	cathode
2	anode
3	gate
TAB	anode

SYMBOL	PARAMETER	Value	Unit
V_{DRM}	Repetitive peak off-state voltages	500RG	V
V_{RRM}	Voltages	650RG	
		800RG	
$I_{T(RMS)}$	RMS on-state current	12	A
I_{TSM}	Non-repetitive peak on-state current	100	A

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Rth j-mb	Thermal resistance Junction to mounting base		-	-	1.3	K/W
Rth j-a	Thermal resistance Junction to ambient	In free air	-	60	-	K/W

Limiting values in accordance with the Maximum system(IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state Voltages	500RG 650RG 800RG	-	500 650 800	V
I_{TAV}	Average on-state current	Half sine wave; $T_{mb} \leq 109^\circ\text{C}$	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	All conduction angles	-	12	A
I_{TSM}	Non-repetitive peak On-state current	half sine wave; $T_j = 25^\circ\text{C}$ prior to surge	T=10ms	100	A
			T=8.3ms	110	A
I^2t	I^2t for fusing	T=10ms	-	50	A^2S
DI_T/dt	Repetitive rate of rise of on-state current after trigering	$I_{TM}=20\text{A}$; $I_G=50\text{mA}$; $DI_G/dt=50\text{mA}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	Peak gate current		-	2	A
V_{GM}	Peak gate voltage		-	5	V
P_{GM}	Peak gate power		-	5	W
$P_{G(AV)}$	Average gate power	Over any 20 ms period	-	0.5	W
T_{stg}	Storage temperature		-40	150	$^\circ\text{C}$
T_j	Operating junction Temperature		-	125 ²	$^\circ\text{C}$

 $T_j = 25^\circ\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Static characteristics						
I_{GT}	Gate trigger current	$V_D=12\text{V}$; $I_T=0.1\text{A}$	-	2	15	mA
I_L	Latching current	$V_D=12\text{V}$; $I_{GT}=0.1\text{A}$	-	10	40	mA
I_H	Holding current	$V_D=12\text{V}$; $I_{GT}=0.1\text{A}$	-	7	20	mA
V_T	On-state voltage	$I_T=23\text{A}$	-	1.4	1.75	V
V_{GT}	Gate trigger voltage	$V_D=12\text{V}$; $I_T=0.1\text{A}$	-	0.6	1.5	V
		$V_D=V_{DRM(max)}$; $I_T=0.1\text{A}$; $T_j=125^\circ\text{C}$	0.25	0.4	-	V
I_D	Off-state leakage current	$V_D=V_{DRM(max)}$; $V_R=V_{RRM(max)}$; $T_j=125^\circ\text{C}$	-	0.1	0.5	mA

Dynamic Characteristics

D_{VD}/dt	Critical rate of rise of Off-state voltage	$V_{DM}=67\% V_{DRM(max)}$; $T_j=125^\circ\text{C}$; exponential wave form; Gate open circuit $R_{gk}=100\Omega$	50 100	130 1000	-	$\text{V}/\mu\text{s}$
t_{gt}	Gate controlled turn-on time	$I_{TM}=40\text{A}$; $V_D=V_{DRM(max)}$; $I_G=0.1\text{A}$; $DI_G/dt=5\text{A}/\mu\text{s}$	-	2	-	μs
t_g	Crcuit commutated tum- off time	$V_{DM}=67\% V_{DRM(max)}$; $T_j=125^\circ\text{C}$; $I_{TM}=20\text{A}$ $V_R=25\text{V}$; $dI_{TM}/dt=30\text{A}/\mu\text{S}$ $DI_G/dt=50\text{V}/\mu\text{s}$; $R_{gk}=100\Omega$	-	70	-	μs

Description

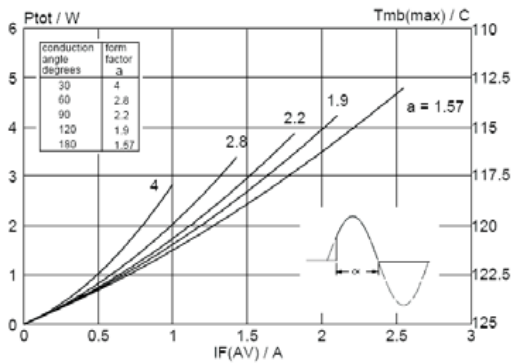


Fig. 1. Maximum on-state dissipation, P_{tot} , versus average on-state current, $I_{T(AV)}$, where $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$.

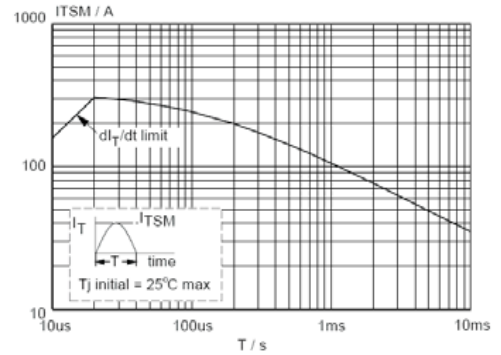


Fig. 2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 10\text{ms}$.

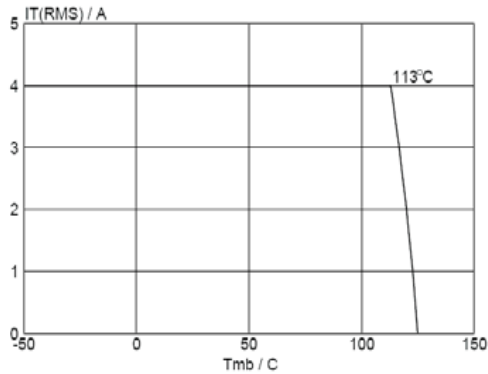


Fig. 3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb} .

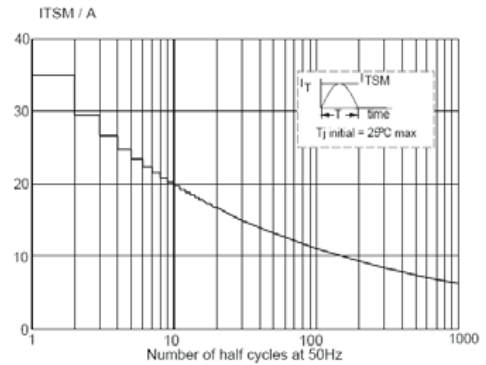


Fig. 4. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50\text{ Hz}$.

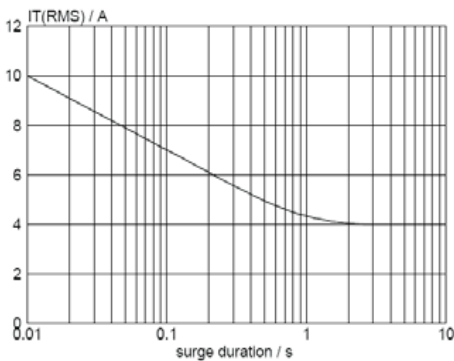


Fig. 5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50\text{ Hz}$; $T_{mb} \leq 113^\circ\text{C}$.

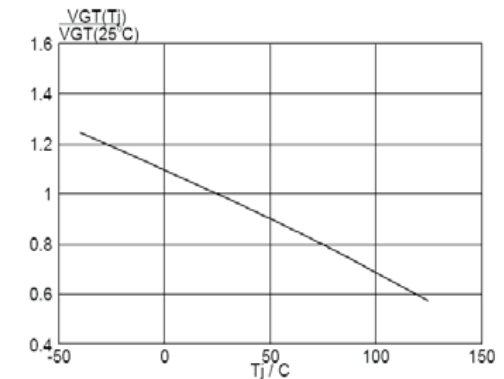


Fig. 6. Normalised gate trigger voltage $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

Description

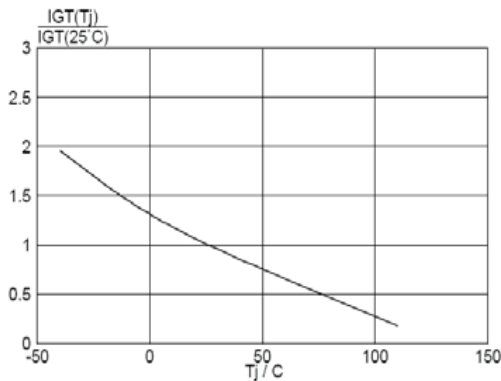


Fig. 7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

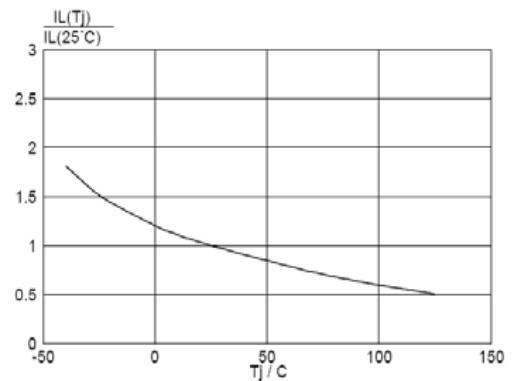


Fig. 8. Normalised latching current $I_L(T_j)/I_L(25^\circ\text{C})$, versus junction temperature T_j .

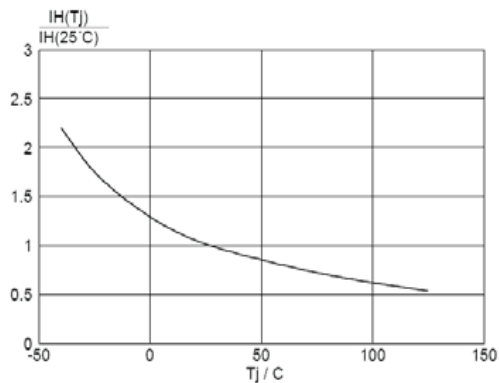


Fig. 9. Normalised holding current $I_H(T_j)/I_H(25^\circ\text{C})$, versus junction temperature T_j .

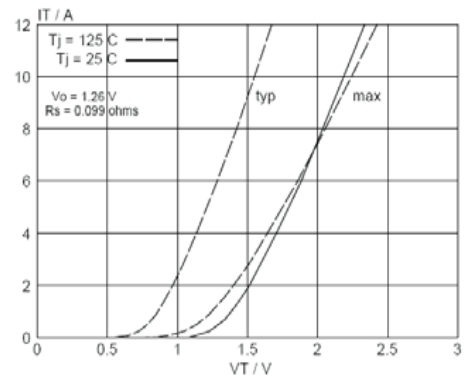


Fig. 10. Typical and maximum on-state characteristic.

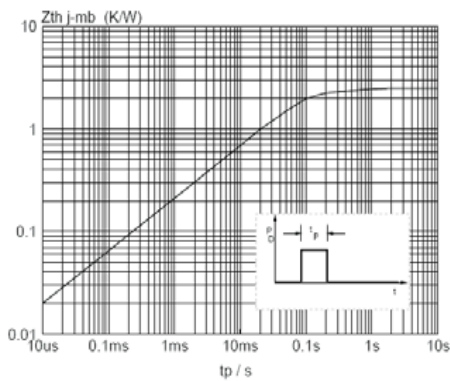


Fig. 11. Transient thermal impedance Z_{thj-mb} , versus pulse width t_p .

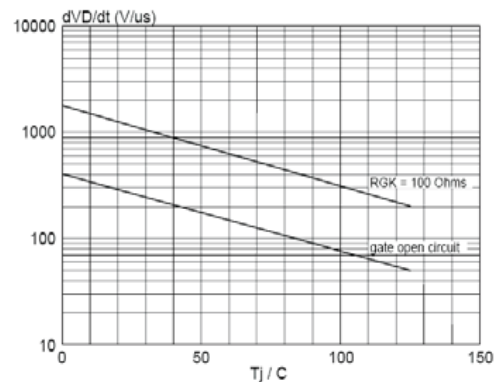
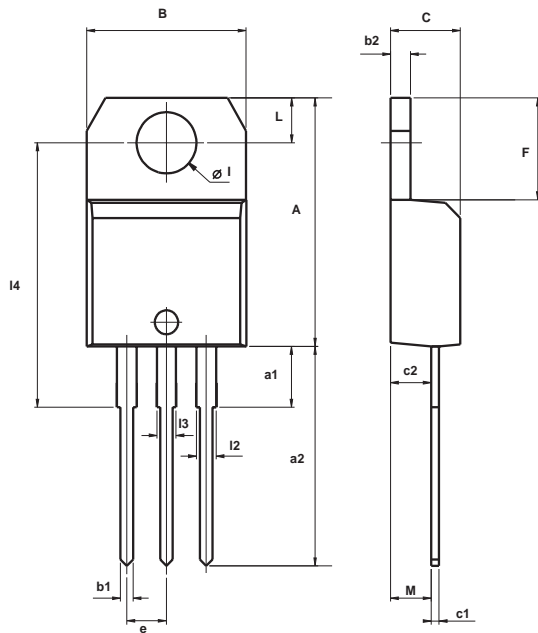


Fig. 12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j .

Package Mechanical Data
TO-220AB (Plastic)


REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	15.20		15.90	0.598		0.625
a1		3.75			0.147	
a2	13.00		14.00	0.511		0.551
B	10.00		10.40	0.393		0.409
b1	0.61		0.88	0.024		0.034
b2	1.23		1.32	0.048		0.051
C	4.40		4.60	0.173		0.181
c1	0.49		0.70	0.019		0.027
c2	2.40		2.72	0.094		0.107
e	2.40		2.70	0.094		0.106
F	6.20		6.60	0.244		0.259
I	3.75		3.85	0.147		0.151
I4	15.80	16.40	16.80	0.622	0.646	0.661
L	2.65		2.95	0.104		0.116
I2	1.14		1.70	0.044		0.066
I3	1.14		1.70	0.044		0.066
M		2.60			0.102	