BT151S-500R(650R,800R)G

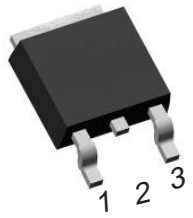
SCRs

Description

Standard gate triggering SCR is fully isolated package suitable for the application where requiring high bidirectional blocking voltage capability and also suitable for over voltage protection , motor control circuit in power tool, inrush current limit circuit and heating control system.

Simplified outline

TO-252



Symbol

Features

- Blocking voltage to 800 V
- On-state RMS current to 12 A

Applications

- Motor control
- Industrial and domestic lighting
- Heating
- Static switching

Pin	Description
1	cathode
2	anode
3	gate
TAB	anode

SYMBOL	PARAMETER		Value	Unit
V_{DRM} V_{RRM}	Repetitive peak off-state voltages Voltages	500RG 650RG 800RG	500 650 800	V
$I_{T\ (RMS)}$	RMS on-state current （full sine wave）		12	A
I_{TSM}	Non-repetitive peak on-state current		100	A

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Rth j-mb	Thermal resistance Junction to mounting base		-	-	1.8	K/W
Rth j-a	Thermal resistance Junction to ambient		-	75	-	K/W

Limiting values in accordance with the Maximum system(IEC 134)

SYMBOL	PARAMETER	CONDITIONS		MIN	MAX	UNIT
V_{DRM},V_{RRM}	Repetitive peak off-state Voltages	500R 650R 800R		-	500 650 800	V
$I_{T(RMS)}$	RMS on-state current	all conduction angles		-	12	A
I_{TSM}	Non-repetitive peak On-state current	half sine wave; Tj = 25℃ prior to surge	T=10ms	-	- 100	- A
			T=8.3ms	-	110	A
I^2t	I^2t for fusing	T=10ms		-	50	A^2S
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM}=20A; I_G=50mA; dI_G/dt=50mA/μs		-	50	A/μs
$I_{T(AV)}$	Average on-state current	half sine wave ; Tmb<=103℃		-	7.5	A
I_{GM}	Peak gate current			-	2	A
V_{RGM}	Peak reverse gate voltage			-	5	V
P_{GM}	Peak gate power			-	5	W
$P_{G(AV)}$	Average gate power	Over any 20 ms period		-	0.5	W
T_{stg}	Storage temperature			-40	150	℃
T_j	Operating junction Temperature			-	125	℃

T_J =25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Static characteristics						
I_{GT}	Gate trigger current	V_D=12V; I_T=0.1A	-	2	15	mA
I_L	Latching current	V_D=12V; I_{GT}=0.1A	-	10	40	mA
I_H	Holding current	V_D=12V; I_{GT}=0.1A	-	7	20	mA
V_T	On-state voltage	I_T=23A	-	1.4	1.75	V
V_{GT}	Gate trigger voltage	V_D=12V;I_T=0.1A V_D=$V_{DRM(max)}$;I_T=0.1A;T_J=125℃	- 0.25	0.6 0.4	1.5 -	V V
I_D,I_R	Off-state leakage current	V_D=$V_{DRM(max)}$;V_R=$V_{RRM(max)}$ T_J=125℃	-	0.1	0.5	mA

Dynamic Characteristics

dV_D/dt	Critical rate of rise of Off-state voltage	V_{DM}=67% $V_{DRM(max)}$;Tj=125℃; exponential waveform; Gate open circuit R_{GK}=100Ω	50 200	130 1000	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM}=40A;V_D=$V_{DRM(max)}$; I_G=0.1A; dI_G/dt=5A/μs	-	2	-	μs
tq	Crcuit commutated turn-off time	V_D=67% $V_{DRM(max)}$;Tj=125°C;I_{TM}=20A V_R=25V;dI_{TM}/dt=30A/μs dV_D/dt=50V/μs;R_{GK}=100Ω	-	70	-	μs

Description

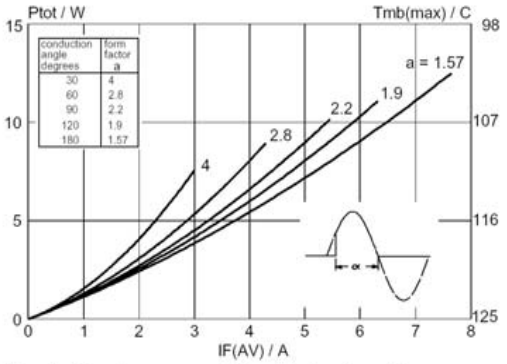


Fig.1. Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a = form factor = $I_{T(RMS)}$/ $I_{T(AV)}$.

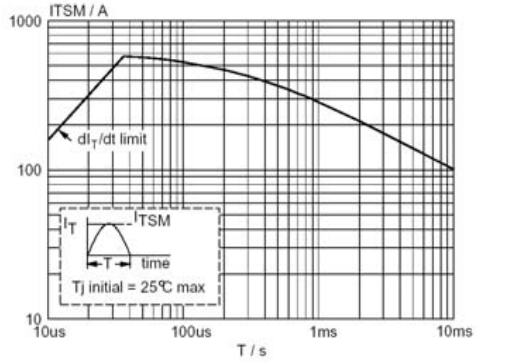


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 10ms$.

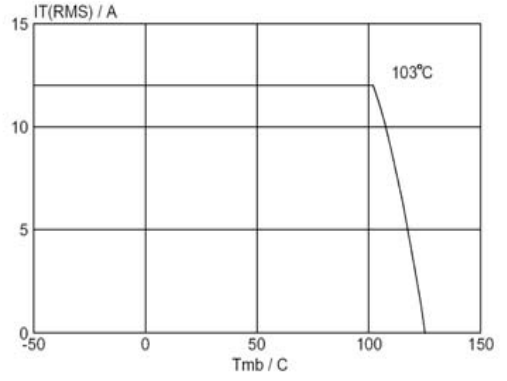


Fig.3. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

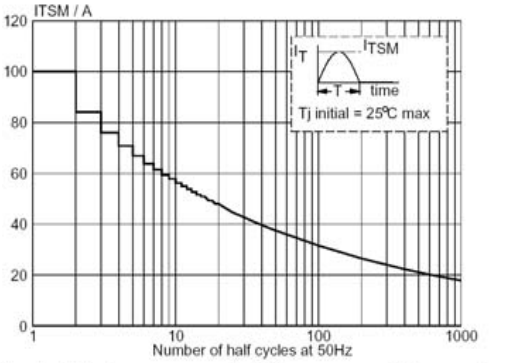


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

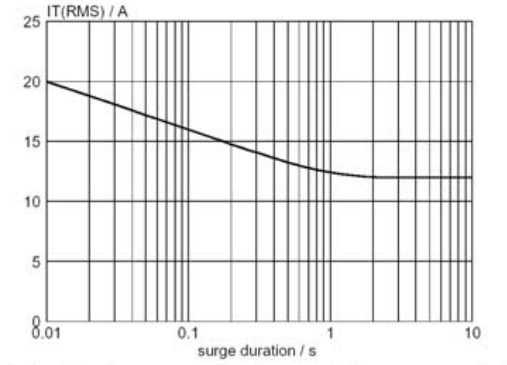


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 103^{\circ}C$.

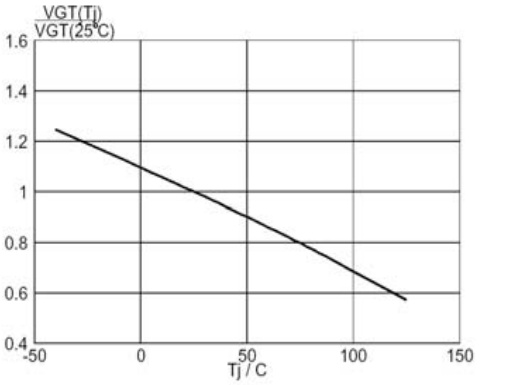


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)$/ $V_{GT}(25^{\circ}C)$, versus junction temperature T_j.

Description

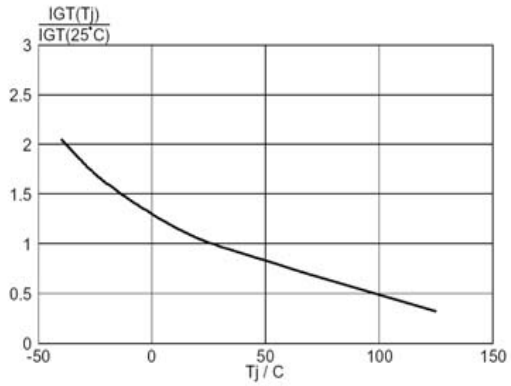


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

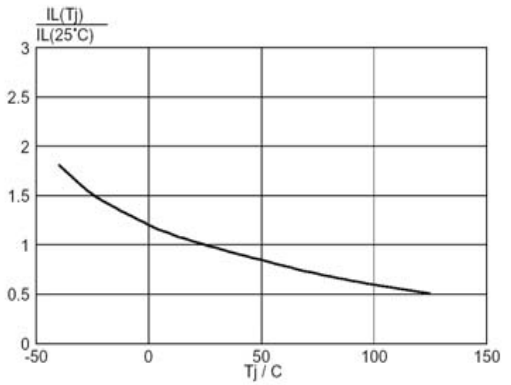


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature T_j.

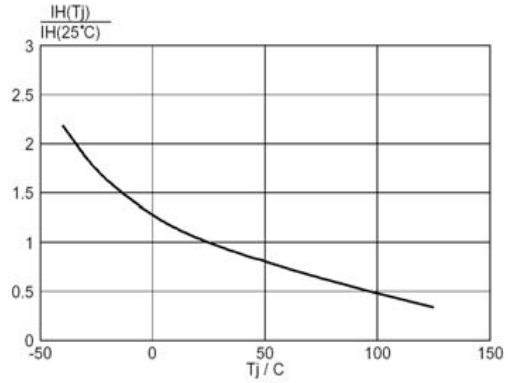


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature T_j.

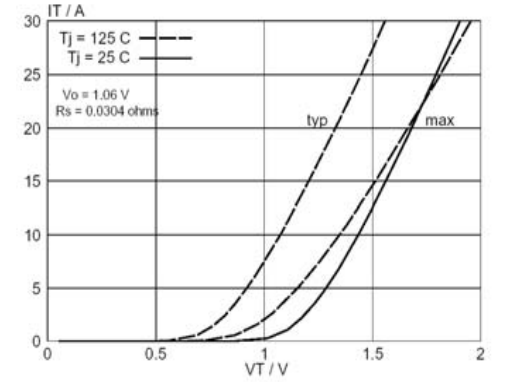


Fig.10. Typical and maximum on-state characteristic.

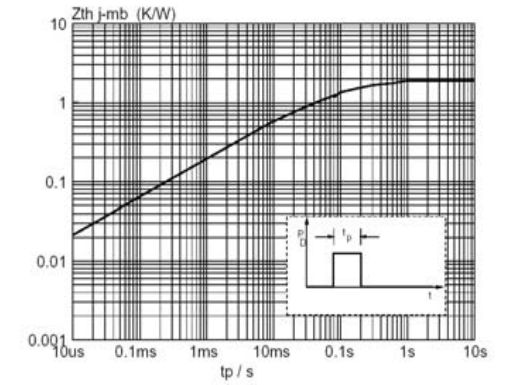


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

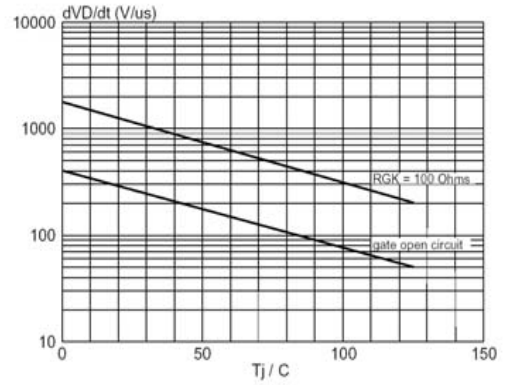
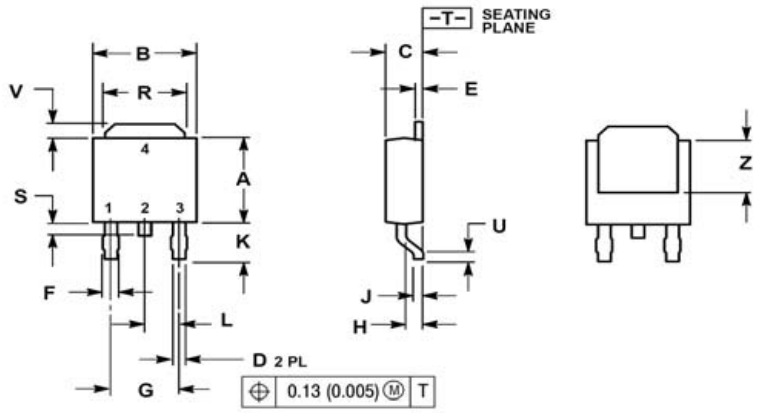


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

Mechanical Data

TO-252

Dimensions in mm
Net Mass: 0.45 g



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

SOLDERING FOOTPRINT