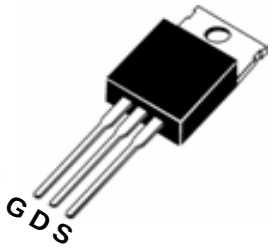
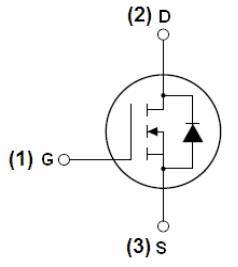
N-Channel Enhancement Mode Power Mosfet

Description

The FIR75N075G is a new generation of middle voltage and high current N–Channel enhancement mode trench power MOSFET. This new technology increases the cell density and reduces the on-resistance; its typical Rdson can reduce to 7.0mohm.

PIN Connection TO-220





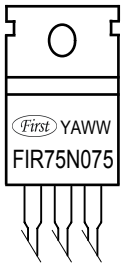
Features

- Advanced trench process technology
- Special designed for Convertors and power controls
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Avalanche Energy 100% test

Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

Marking Diagram



Y = Year
A = Assembly Location
WW = Work Week
FIR75N075 = Specific Device Code

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR75N075	FIR75N075G	TO-220	-	-	-

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D@T_c=25℃	Continuous drain current,VGS@10V	78	A
I_D@T_c=100℃	Continuous drain current,VGS@10V	55	
I_{DM}	Pulsed drain current ①	300	
P_D@T_C=25℃	Power dissipation	160	W
	Linear derating factor	1.05	W/℃
V_{GS}	Gate-to-Source voltage	±20	V
dv/dt	Peak diode recovery voltage	310	v/ns
E_{AS}	Single pulse avalanche energy ②	550	mJ
E_{AR}	Repetitive avalanche energy	TBD	
T_J T_{STG}	Operating Junction and Storage Temperature Range	–55 to +175	℃

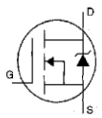
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	0.94	—	℃/W
$R_{\theta JA}$	Junction-to-ambient	—	—	62	

Electrical Characteristics @TJ=25 ℃ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source breakdown voltage	75	84	—	V	V_{GS}=0V,I_D=250μA
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	7	8.5	mΩ	V_{GS}=10V,I_D=40A
$V_{GS(th)}$	Gate threshold voltage	2.0	2.9	4.0	V	V_{DS}=V_{GS},I_D=250μA
g_{fs}	Forward transconductance	—	58	—	S	V_{DS}=5V,I_D=30A
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	V_{DS}=75V,V_{GS}=0V
		—	—	10		V_{DS}=75V, V_{GS}=0V,T_J=150℃
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source reverse leakage	—	—	-100		V_{GS}=-20V
Q_g	Total gate charge	—	94	—	nC	I_D=30A
Q_{gs}	Gate-to-Source charge	—	16	—		V_{DD}=30V
Q_{gd}	Gate-to-Drain("Miller") charge	—	24	—		V_{GS}=10V
$t_{d(on)}$	Turn-on delay time	—	15	—	nS	V_{DD}=30V I_D=2A ,R_L=15Ω R_G=2.5Ω V_{GS}=10V
t_r	Rise time	—	11	—		
$t_{d(off)}$	Turn-Off delay time	—	52	—		
t_f	Fall time	—	13	—		
C_{iss}	Input capacitance	—	3400	—	pF	V_{GS}=0V V_{DS}=25V f=1.0MHZ
C_{oss}	Output capacitance	—	290	—		
C_{rss}	Reverse transfer capacitance	—	221	—		

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current. (Body Diode)	—	—	78	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current . (Body Diode) ①	—	—	312		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J=25℃,I_S=40A,V_{GS}=0V ③
t_{rr}	Reverse Recovery Time	—	—	33	nS	T_J=25℃,I_F=75A di/dt=100A/μs ③
Q_{rr}	Reverse Recovery Charge	—	—	54	nC	
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by Ls + LD)				

Notes:

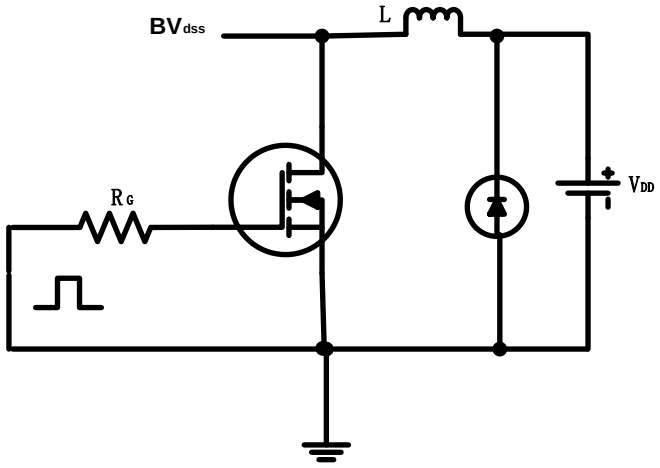
① Repetitive rating; pulse width limited by max junction temperature.

② Test condition: L =0.3mH, ID = 57A, VDD = 47V

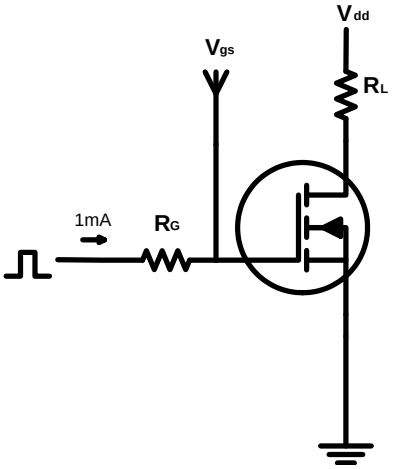
③ Pulse width≤300μS; duty cycle≤1.5% RG = 25Ω,Starting TJ = 25°C

Test circuit

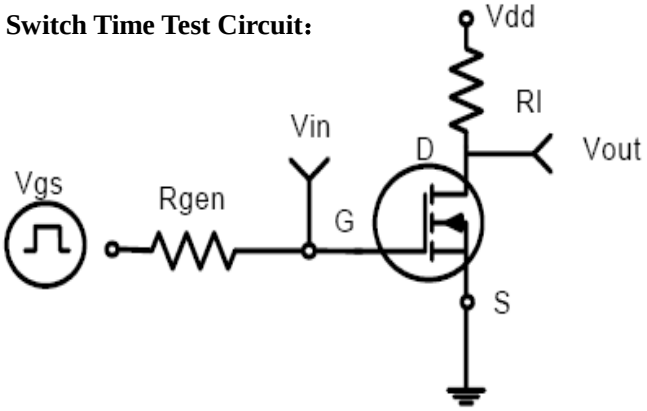
EAS test circuits:



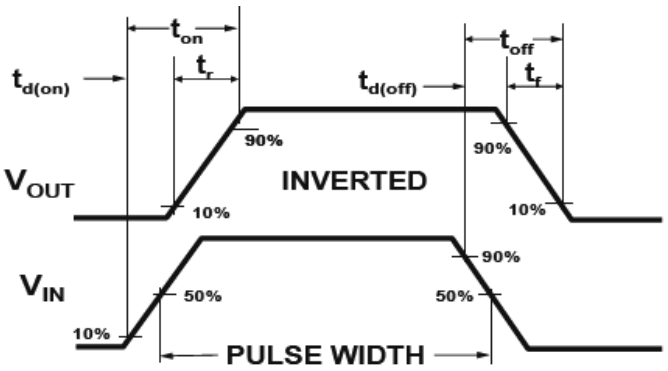
Gate charge test circuit:

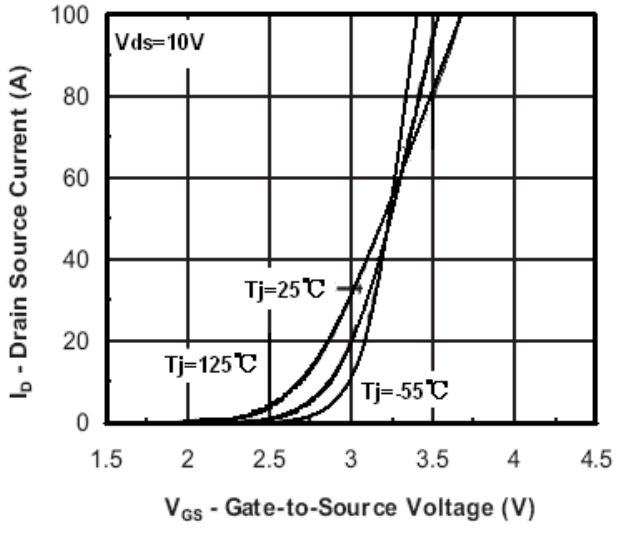


Switch Time Test Circuit:

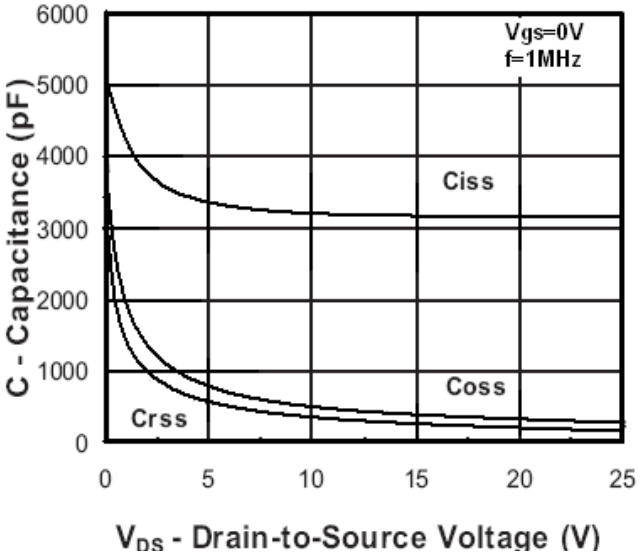


Switch Waveforms:

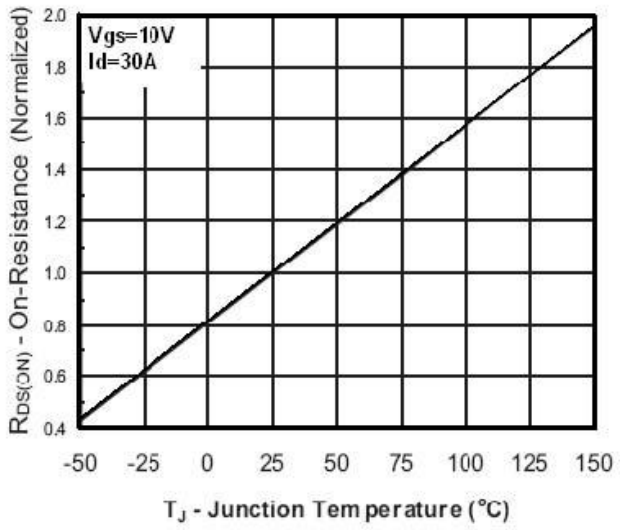




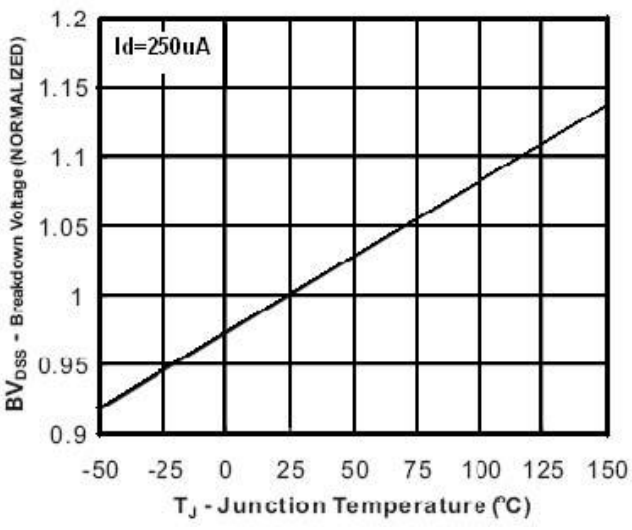
Transfer Characteristic



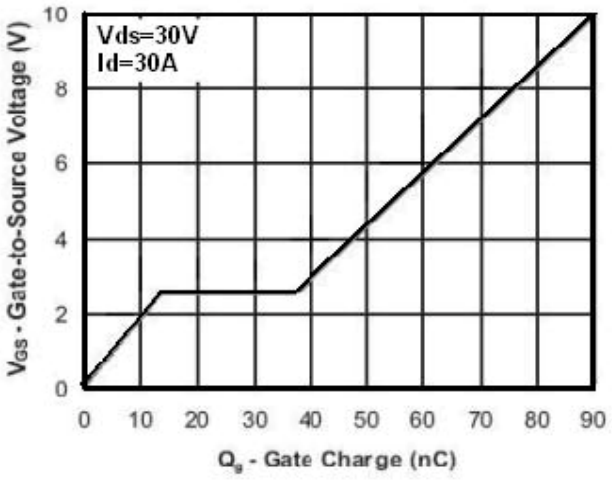
Capacitance



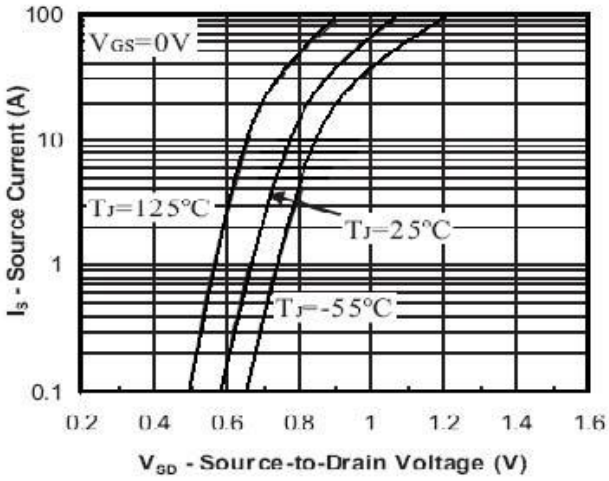
On Resistance vs. Junction Temperature



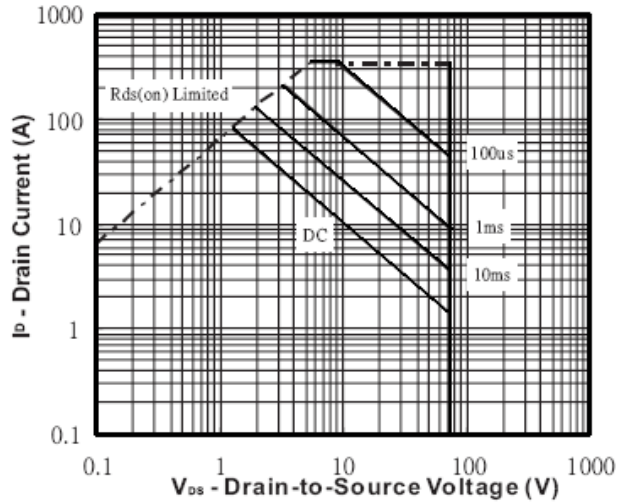
Breakdown Voltage vs. Junction Temperature



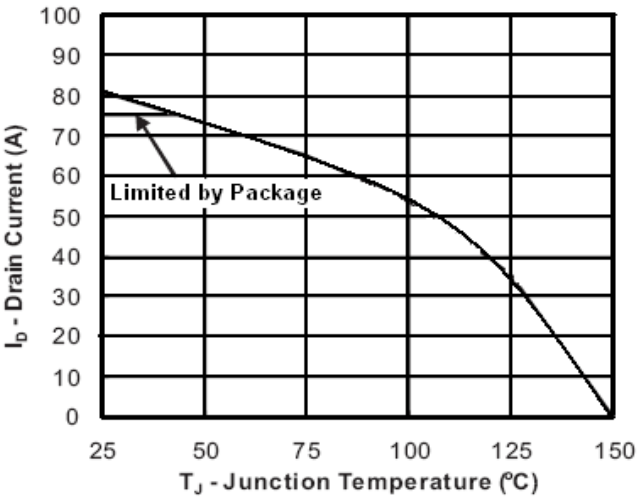
Gate Charge



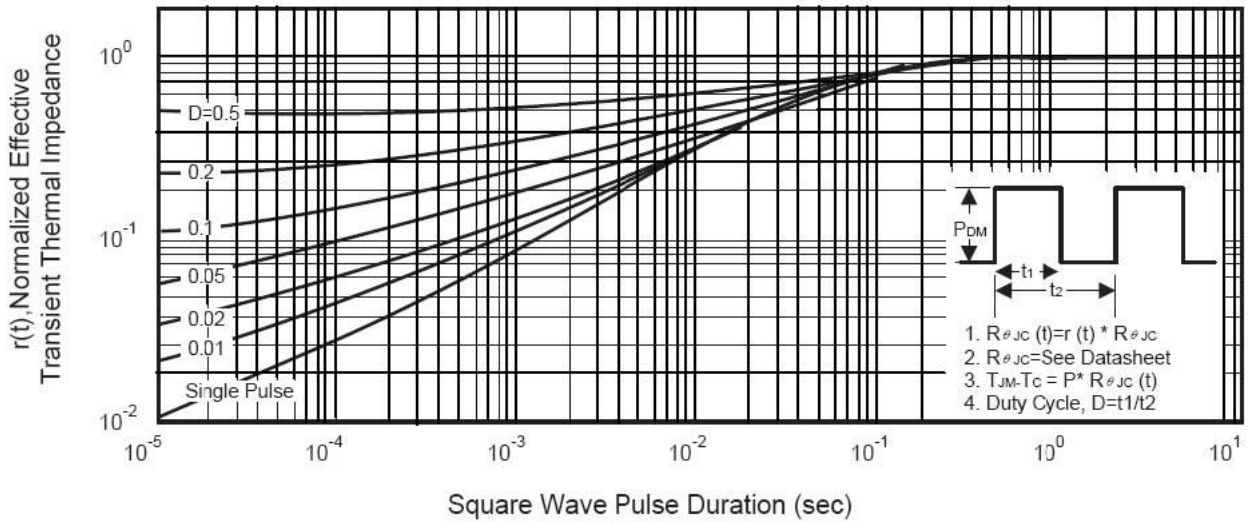
Source-Drain Diode Forward Voltage



Safe Operation Area



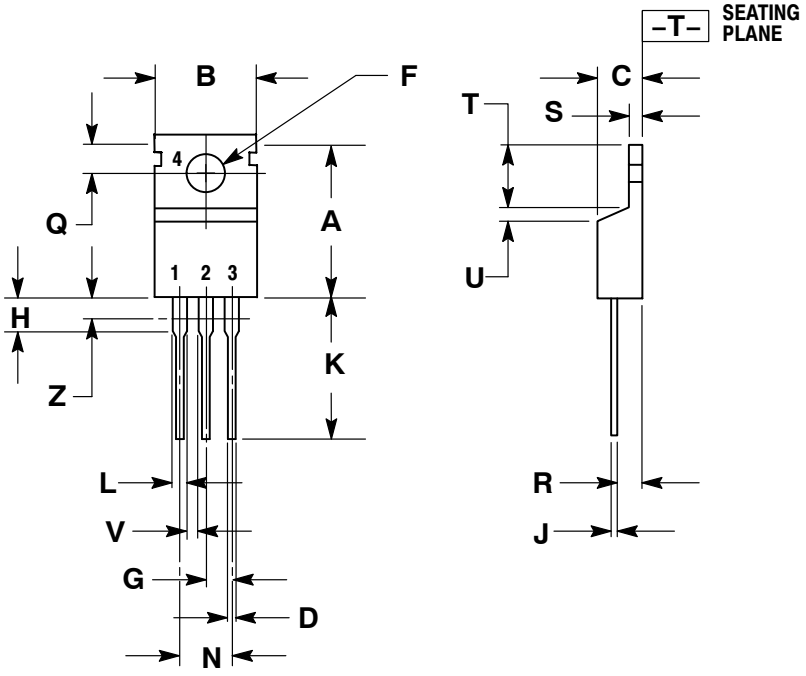
Max Drain Current vs. Junction Temperature



Transient Thermal Impedance Curve

Package Dimensions

TO-220



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE