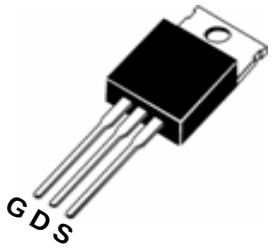
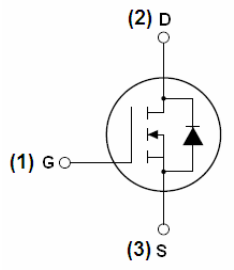
N-Channel Enhancement Mode Power Mosfet

Description

The FIR210N06G uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

PIN Connection TO-220





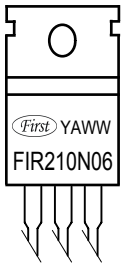
General Features

- V_{DS} =60V ,I_D =210A
  $R_{DS(ON)}$ < 4mΩ @ V_{GS}=10V
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

Marking Diagram



Y = Year
A = Assembly Location
WW = Work Week
FIR210N06 = Specific Device Code

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR210N06	FIR210N06G	TO-220	-	-	-

Absolute Maximum Ratings (TA=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	210	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	148	A
Pulsed Drain Current	I_{DM}	840	A
Maximum Power Dissipation	P_D	330	W
Derating factor		2.2	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	1800	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	0.455	℃/W

Electrical Characteristics (TA=25℃unless otherwise noted)

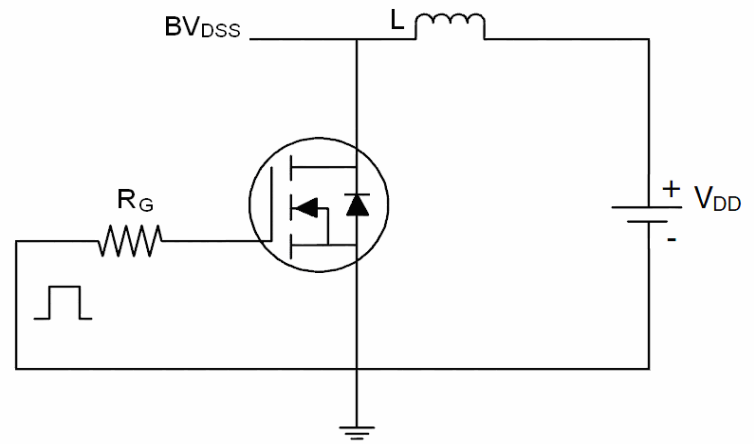
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	68	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=40A	-		4	mΩ
Forward Transconductance	g_{FS}	V_{DS}=24V,I_D=40A	160	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	11000	-	PF
Output Capacitance	C_{oss}		-	1120	-	PF
Reverse Transfer Capacitance	C_{rss}		-	950	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	VDD=30V,ID=2A,RL=15Ω, RG=2.5Ω,VGS=10V	-	40	-	nS
Turn-on Rise Time	t_r		-	38	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	140	-	nS
Turn-Off Fall Time	t_f		-	60	-	nS
Total Gate Charge	Q_g	ID=30A,VDD=30V,VGS=10V	-	250	-	nC
Gate-Source Charge	Q_{gs}		-	48	-	nC
Gate-Drain Charge	Q_{gd}		-	98	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=40A	-	0.85	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	210	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 40A di/dt = 100A/μs(Note3)	-	48		nS
Reverse Recovery Charge	Qrr		-	78		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

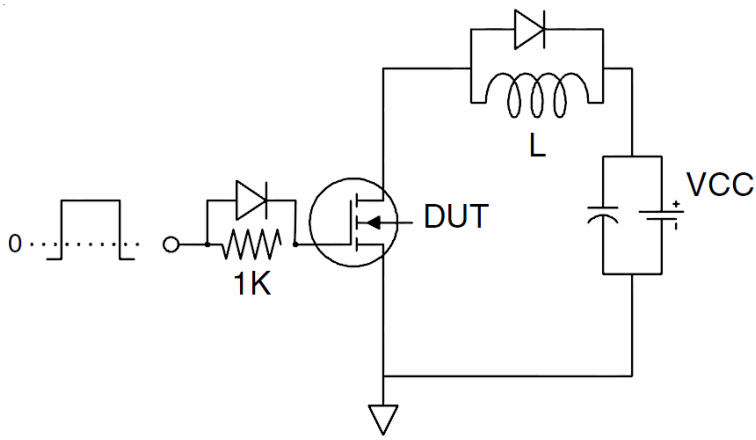
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition：Tj=25℃,V_{DD}=30V,V_G=10V,L=1mH,Rg=25Ω

Test circuit

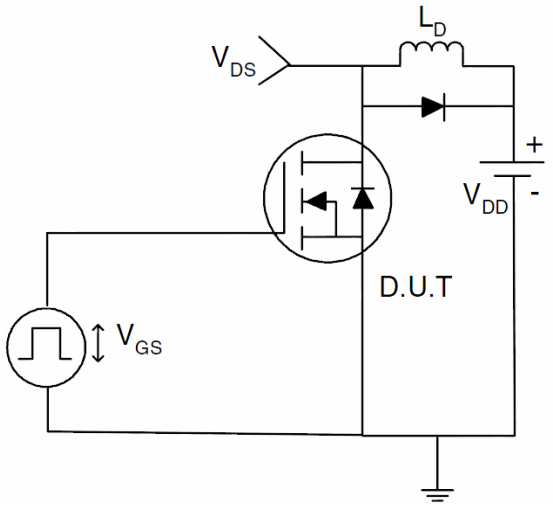
1）E_{AS} test Circuits



2）Gate charge test Circuit:



3）Switch Time Test Circuit：



Typical Electrical And Thermal Characteristics(Curves)

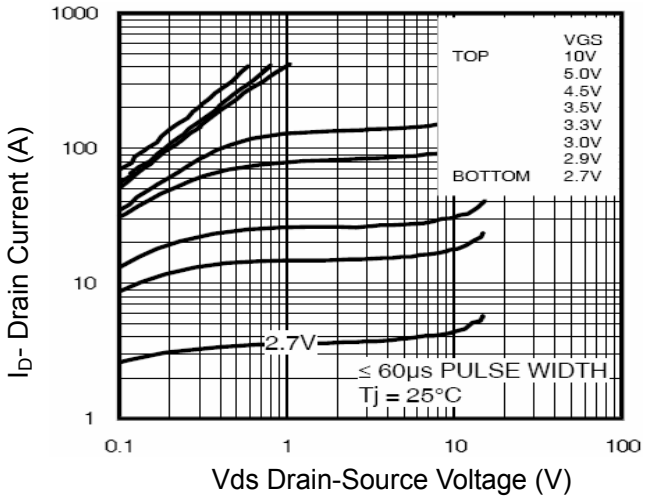


Figure 1 Output Characteristics

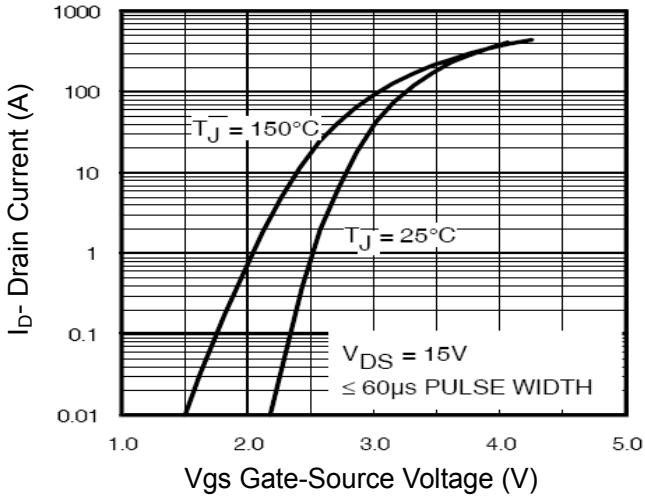


Figure 2 Transfer Characteristics

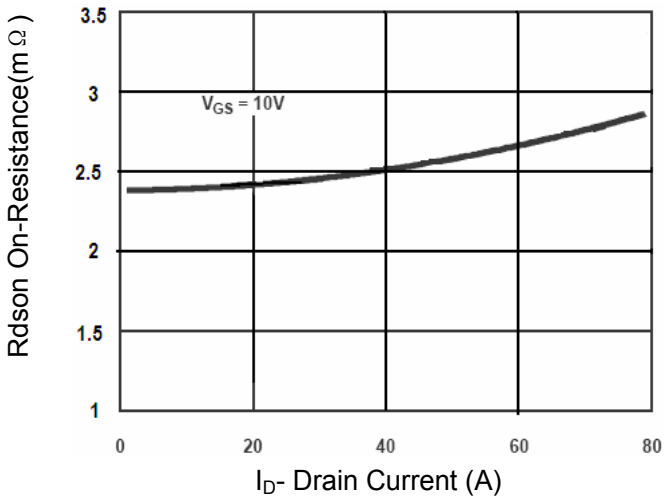


Figure 3 Rdson- Drain Current

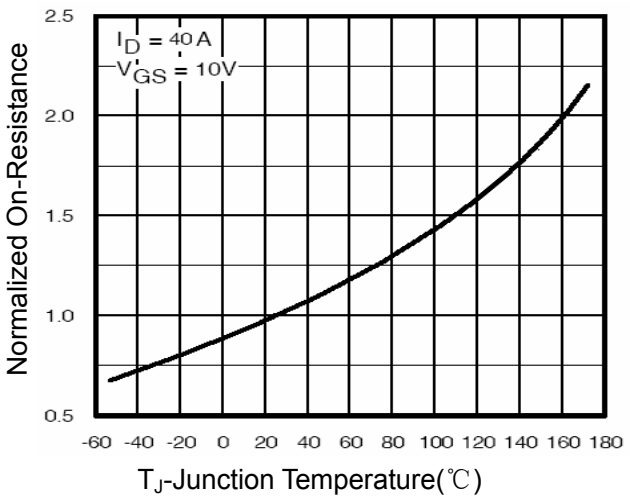


Figure 4 Rdson-JunctionTemperature

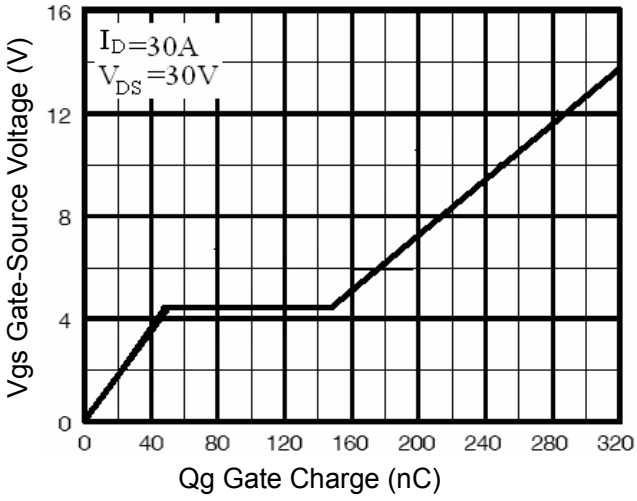


Figure 5 Gate Charge

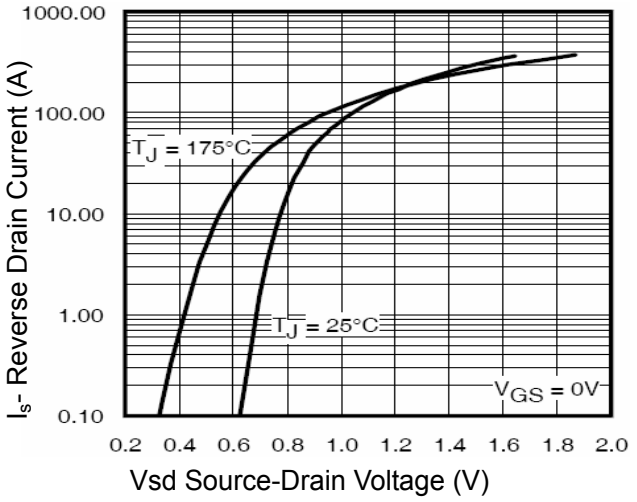


Figure 6 Source- Drain Diode Forward

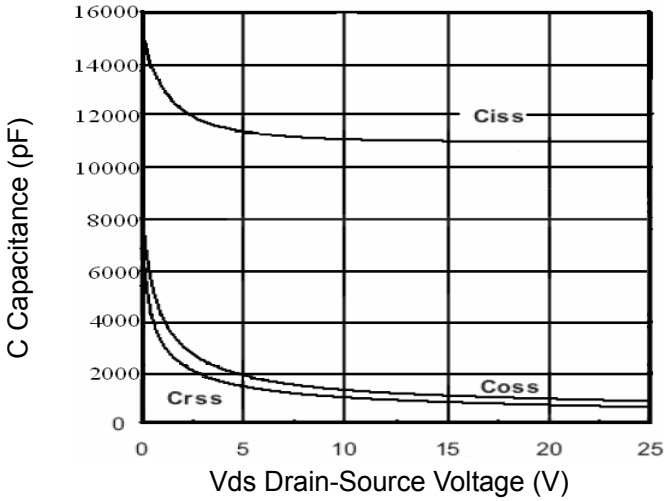


Figure 7 Capacitance vs Vds

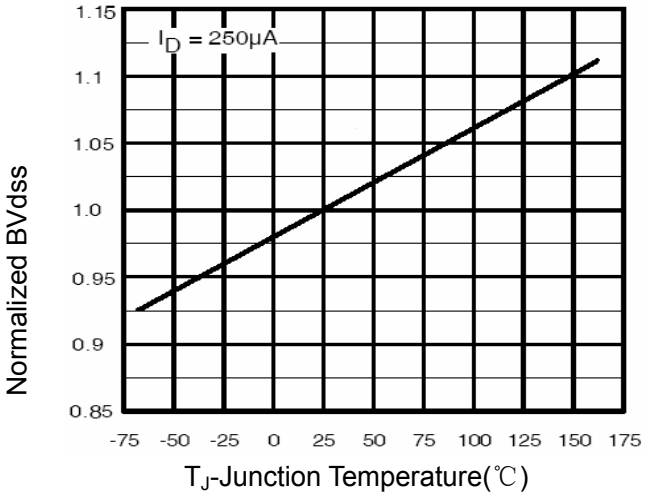


Figure 9 BV_{DSS} vs Junction Temperature

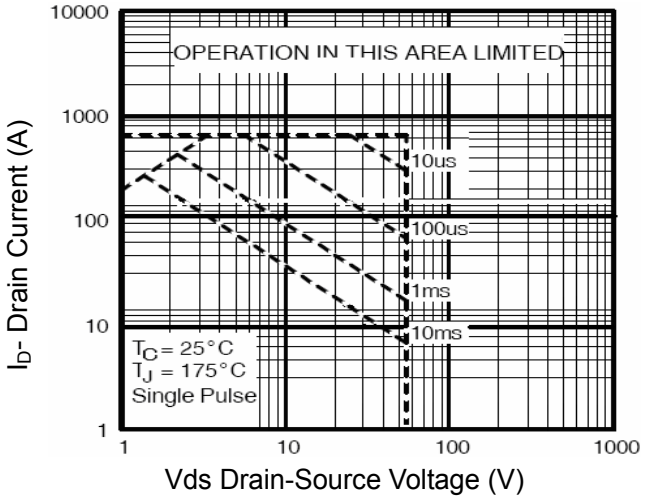


Figure 8 Safe Operation Area

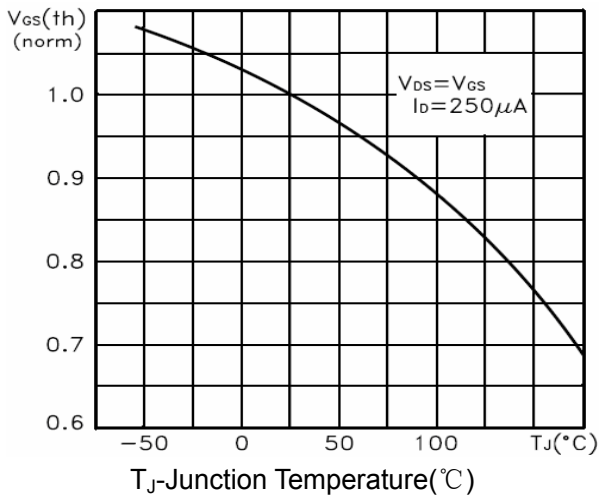


Figure 10 $V_{GS(th)}$ vs Junction Temperatur

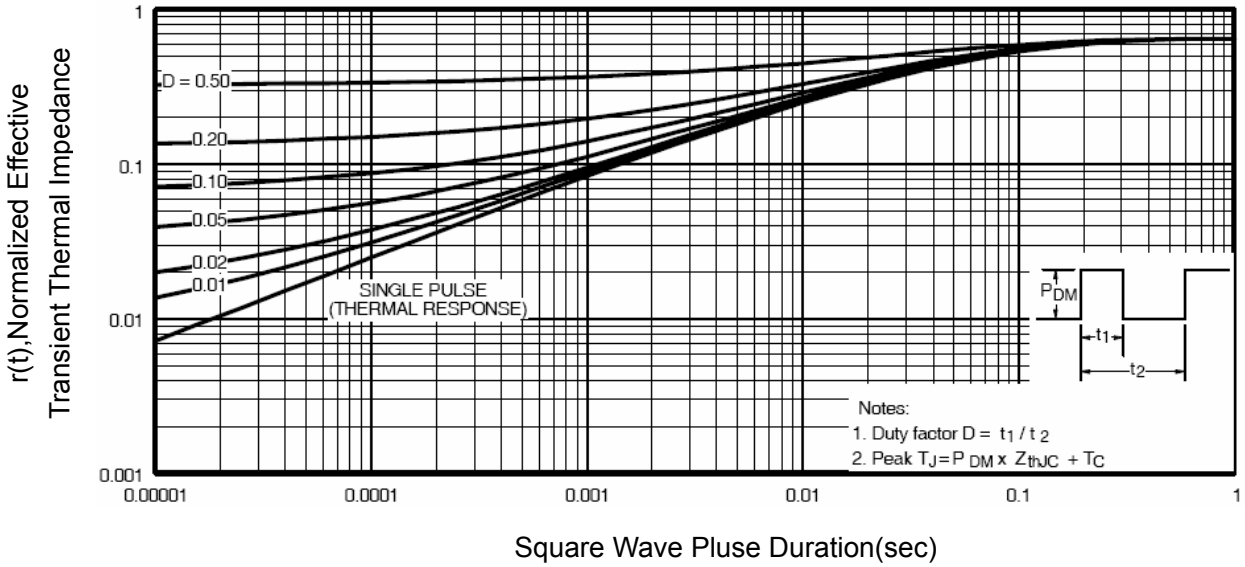
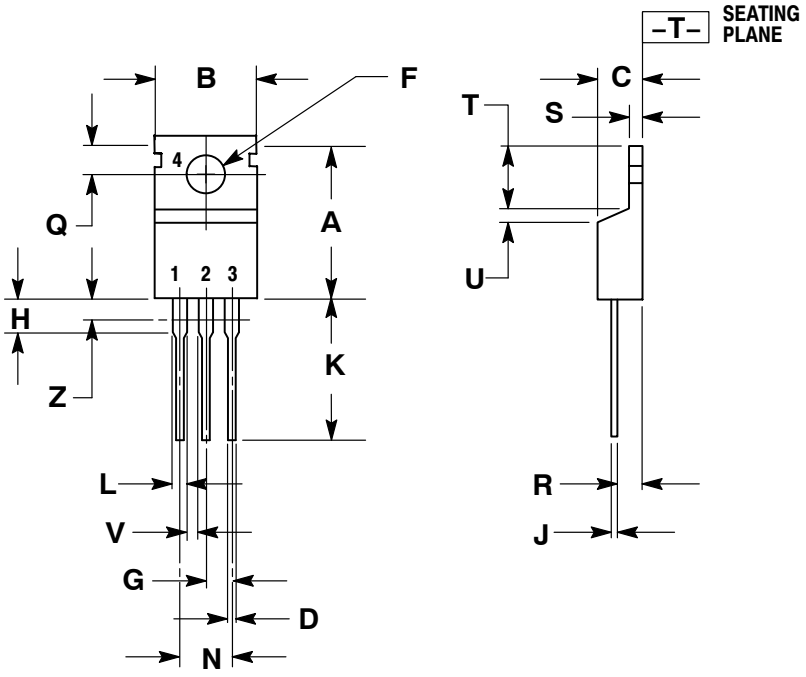


Figure 11 Normalized Maximum Transient Thermal Impedance

Package Dimensions

TO-220



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE