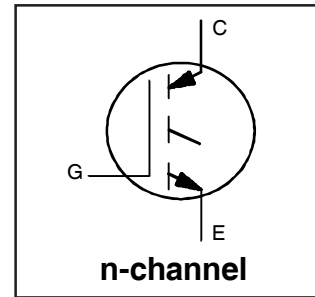


IRGC4271B

Features

- Low $V_{CE(ON)}$ Trench IGBT Technology
- Low Switching Losses
- Maximum Junction Temperature 175 °C
- Short Circuit Rated
- Square RBSOA
- Positive $V_{CE(ON)}$ Temperature Coefficient
- Tight Parameter Distribution
- Integrated Gate Resistor



Benefits

- High Efficiency in a Wide Range of Applications
- Suitable for a Wide Range of Switching Frequencies due to Low $V_{CE(ON)}$ and Low Switching Losses
- Rugged Transient Performance for Increased Reliability
- Excellent Current Sharing in Parallel Operation
- Easier Paralleling with Integrated Gate Resistor

Applications

- Industrial Motor Drive
- Inverters
- UPS
- Welding

Chip Type	V_{CE}	I_{Cn}	Die Size	Package
IRGC4271B	650V	75A	7.03 x 5.92 mm ²	Wafer

Mechanical Parameter

Die Size	7.03 x 5.92	mm ²
Minimum Street Width	75	μm
Emitter Pad Size (Included Gate Pad)	See Die Drawing	
Gate Pad Size	0.7 x 1.7	mm ²
Area Total / Active	41.6 / 30.6	
Thickness	70	μm
Wafer Size	150	mm
Flat Position	0	Degrees
Maximum-Possible Chips per Wafer	350 pcs	
Passivation Frontside	Silicon Nitride	
Front Metal	Al, Si (4μm)	
Backside Metal	Al (0.1μm), Ti (0.1μm), Ni (0.4μm), Ag (0.6μm)	
Die Bond	Electrically conductive epoxy or solder	
Reject Ink Dot Size	0.25 mm diameter minimum black	

Maximum Ratings

	Parameter	Max.	Units
V_{CE}	Collector-Emitter Voltage, $T_J=25^\circ\text{C}$	650	V
I_C	DC Collector Current	①	A
I_{LM}	Clamped Inductive Load Current ②	300	A
V_{GE}	Gate Emitter Voltage	± 20	V
T_J, T_{STG}	Operating Junction and Storage Temperature	-40 to +175	$^\circ\text{C}$

Static Characteristics (Tested on wafers) @ $T_J=25^\circ\text{C}$

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	650	—	—	V	$V_{GE} = 0\text{V}, I_D = 100\mu\text{A}$ ③
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.2	1.5		$V_{GE} = 15\text{V}, I_D = 20\text{A}, T_J=25^\circ\text{C}$
$V_{GE(th)}$	Gate-Emitter Threshold Voltage	5.5	—	7.7		$I_C = 2.5\text{mA}, V_{GE} = V_{CE}$
I_{CES}	Zero Gate Voltage Collector Current	—	1	15	μA	$V_{CE}=650\text{V}, V_{GE} = 0\text{V}$
I_{GES}	Gate Emitter Leakage Current	—	—	± 600	nA	$V_{CE} = 0\text{V}, V_{GE} = \pm 20\text{V}$
$R_{G\text{INTERNAL}}$	Internal Gate Resistance	3.2	4.3	5.3	Ω	

Electrical Characteristics (Not subject to production test- Verified by design/characterization)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.6	1.9	V	$V_{GE} = 15\text{V}, I_D = 75\text{A}, T_J=25^\circ\text{C}$ ④
		—	2.0	—		$V_{GE} = 15\text{V}, I_D = 75\text{A}, T_J=175^\circ\text{C}$ ④
SCSOA	Short Circuit Safe Operating Area	5.5	—	—	μs	$V_{GE}=15\text{V}, V_{CC}=400\text{V},$ ⑤ $R_G=5.0\Omega, V_P \leq 600\text{V}, T_J= 150^\circ\text{C}$
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				$T_J = 175^\circ\text{C}, I_C = 225\text{A}$ $V_{CC} = 480\text{V}, V_P \leq 600\text{V}$ $R_g = 5.0\Omega, V_{GE} = +20\text{V to } 0\text{V}$
C_{iss}	Input Capacitance	—	4990	—	pF	$V_{GE} = 0\text{V}$
C_{oss}	Output Capacitance	—	260	—		$V_{CE} = 30\text{V}$
C_{riss}	Reverse Transfer Capacitance	—	135	—		$f = 1.0\text{MHz}$
Q_g	Total Gate Charge (turn-on)	—	160	—	nC	$I_C = 75\text{A}$
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	50	—		$V_{GE} = 15\text{V}$
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	66	—		$V_{CC} = 400\text{V}$

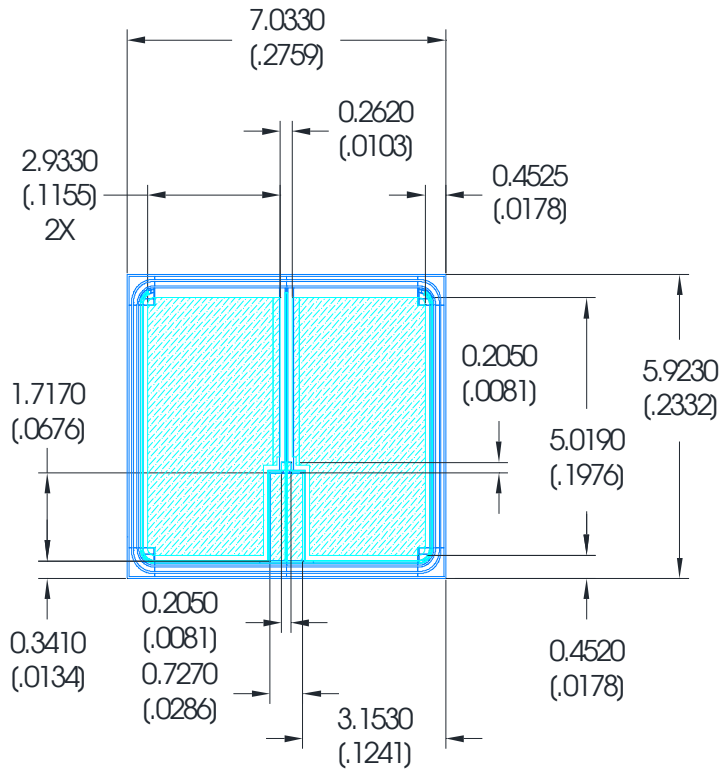
Switching Characteristics (Inductive Load-Not subject to production test-Verified by design/ characterization)

	Parameter	Min.	Typ.	Max.	Units	Conditions ⑥ ⑦
$t_{d(on)}$	Turn-On delay time	—	75	—	ns	$I_C = 75\text{A}, V_{CC} = 400\text{V}$ $R_G = 5.0\Omega, V_{GE}=15\text{V}, L=150\mu\text{H}$ $T_J = 25^\circ\text{C}$
t_r	Rise time	—	65	—		
$t_{d(off)}$	Turn-Off delay time	—	170	—		
t_f	Fall time	—	25	—		
$t_{d(on)}$	Turn-On delay time	—	70	—		$I_C = 75\text{A}, V_{CC} = 400\text{V}$ $R_G = 5.0\Omega, V_{GE}=15\text{V}, L=150\mu\text{H}$ $T_J = 175^\circ\text{C}$
t_r	Rise time	—	65	—		
$t_{d(off)}$	Turn-Off delay time	—	205	—		
t_f	Fall time	—	45	—		

Notes:

- ① The current in the application is limited by T_{JMax} and the thermal properties of the assembly.
- ② $V_{CC} = 80\% (V_{CES}), V_{GE} = 20\text{V}, L = 150\mu\text{H}, R_G = 5.0\Omega$.
- ③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.
- ④ Die level characterization.
- ⑤ Not subject to production test- Verified by design / characterization.
- ⑥ Pulse width limited by max. junction temperature.
- ⑦ Values influenced by parasitic L and C in measurement.

Chip drawing



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
2. CONTROLLING DIMENSION: INCHES
3. DIE WIDTH AND LENGTH TOLERANCE: +0, -0.0508 (+0, -0.0020)
4. DIE THICKNESS = 0.070 (.00276)

REFERENCE: IRGC4271B

Additional Testing and Screening

For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales.

Shipping

Three shipping options are offered.

- Un-sawn wafer
- Die in waffle pack (consult the IR Die Sales team for availability)
- Die on film (consult the IR Die Sales team for availability)

Tape and Reel is also available for some products. Please consult your local IR sales office or email <http://die.irf.com> for additional information.

Please specify your required shipping option when requesting prices and ordering Die product. If not specified, Un-sawn wafer will be assumed.

Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

General Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Un-sawn wafers in the original vacuum sealed packaging can be stored for up to 3 years at a temperature of less than 30° C and less than 30% relative humidity.
- Singulated die and KGD products that have been opened should be kept in their original packaging and transferred to a filtered N2 environment upon immediate opening of packaging in a clean room environment. The storage condition must ensure a less than 30% relative humidity and at a temperature less than 30° C. ESD precautions to EIS-541 should be maintained to ensure safe handling, storage and transportation requirement. Maximum shelf life is 2 years from date of manufacture.
- **Note:** Warning products are sensitive to environmental conditions and should be stored immediately in a N2 filtered environment at <30% relative humidity in original packaging upon receipt of product.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.
- Die in Surf Tape type carrier tape are intended for immediate use and have a limited shelf life. This is primarily due to the nature of the adhesive tape used to hold the product in the carrier tape cavity. This product can be stored for up to 30 days. This applies whether or not the material has remained in its original sealed container.

Further Information

For further information please contact your local IR Sales office or email your enquiry to <http://die.irf.com>

Data and specifications subject to change without notice.
This product has been designed and qualified for Industrial market.
Qualification Standards can be found on IR's Web site.

International
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Visit us at www.irf.com for sales contact information. 03/2012

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