



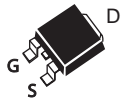
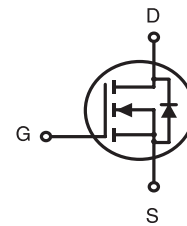
## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### PRODUCT SUMMARY

V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (Ω) Typ
600V	4A	2.1 @ V <sub>GS</sub> =10V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.

SDU SERIES  
TO-252(D-PAK)SDD SERIES  
TO-251S(I-PAK)SDD SERIES  
TO-251L(I-PAK)

### ORDERING INFORMATION

Ordering Code	Package	Marking Code	Delivery Mode	RoHS Status
SDU04N60HZ	TO-252	SDU04N60	Reel	Halogen Free
SDD04N60HS	TO-251S	SDD04N60	Tube	Halogen Free
SDD04N60HL	TO-251L	SDD04N60	Tube	Halogen Free

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units	
V <sub>DS</sub>	Drain-Source Voltage	600	V	
V <sub>GS</sub>	Gate-Source Voltage	±30	V	
I <sub>D</sub>	Drain Current-Continuous <sup>a e</sup>	T <sub>C</sub> =25°C	4	A
		T <sub>C</sub> =100°C	2.8	A
I <sub>DM</sub>	-Pulsed <sup>b</sup>	11.8	A	
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>	51	mJ	
P <sub>D</sub>	Maximum Power Dissipation	T <sub>C</sub> =25°C	83	W
		T <sub>C</sub> =100°C	42	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 175	°C	

### THERMAL CHARACTERISTICS

R <sub>θ JC</sub>	Thermal Resistance, Junction-to-Case	1.8	°C/W
R <sub>θ JA</sub>	Thermal Resistance, Junction-to-Ambient	50	°C/W

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## ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	600			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =480V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±30V , V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2	3	4	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =2A		2.1	2.6	ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =20V , I <sub>D</sub> =2A		3.5		S
<b>DYNAMIC CHARACTERISTICS °</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		500		pF
C <sub>OSS</sub>	Output Capacitance			60		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			12		pF
<b>SWITCHING CHARACTERISTICS °</b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =300V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>GEN</sub> =6 ohm		20		ns
t <sub>r</sub>	Rise Time			17		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			24		ns
t <sub>f</sub>	Fall Time			12		ns
Q <sub>g</sub>	Total Gate Charge		V <sub>DS</sub> =300V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V		11.2	
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =300V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V		2.2		nC
Q <sub>gd</sub>	Gate-Drain Charge			4.9		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =1A		0.78	1.4	V
<b>Notes</b> a.Surface Mounted on FR4 Board, t ≤ 10sec. b.Pulse Test:Pulse Width ≤ 300us, Duty Cycle ≤ 2%. c.Guaranteed by design, not subject to production testing. d.Starting T <sub>J</sub> =25°C, L=5mH, V <sub>DD</sub> = 50V.(See Figure13) e.Drain current limited by maximum junction temperature.						

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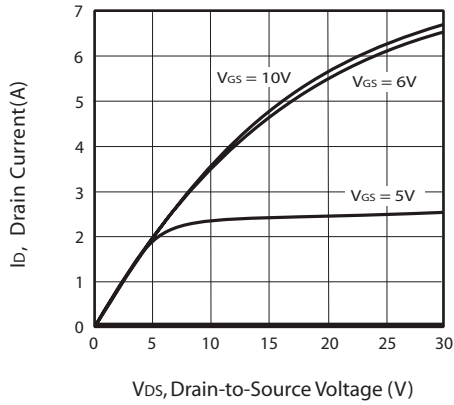


Figure 1. Output Characteristics

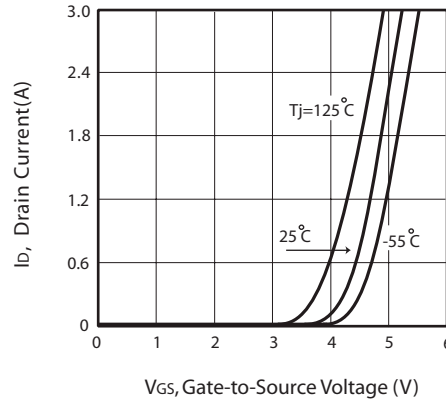


Figure 2. Transfer Characteristics

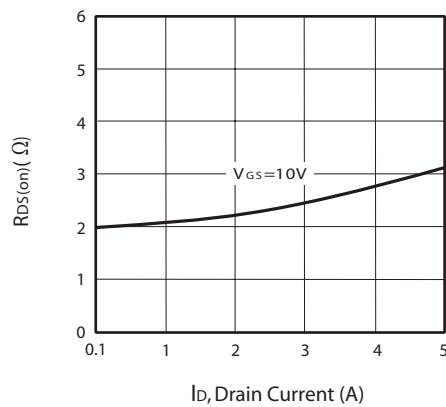


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

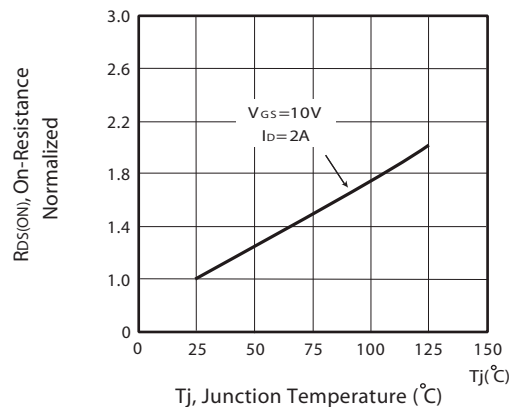


Figure 4. On-Resistance Variation with Drain Current and Temperature

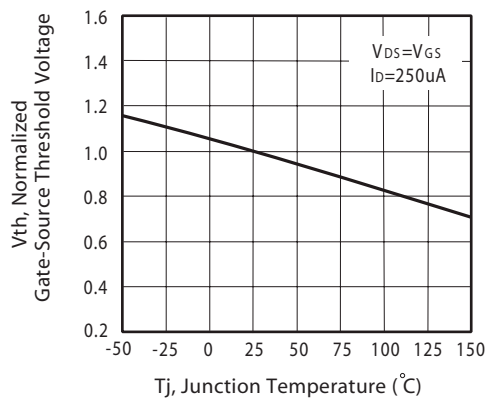


Figure 5. Gate Threshold Variation with Temperature

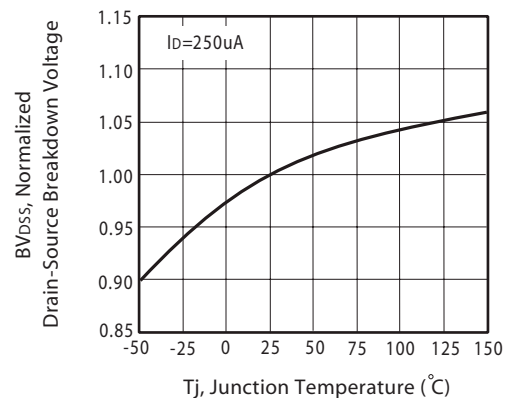


Figure 6. Breakdown Voltage Variation with Temperature

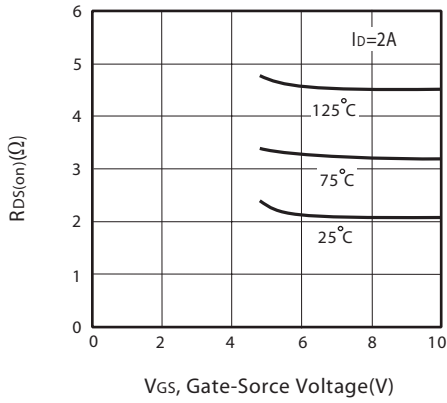


Figure 7. On-Resistance vs. Gate-Source Voltage

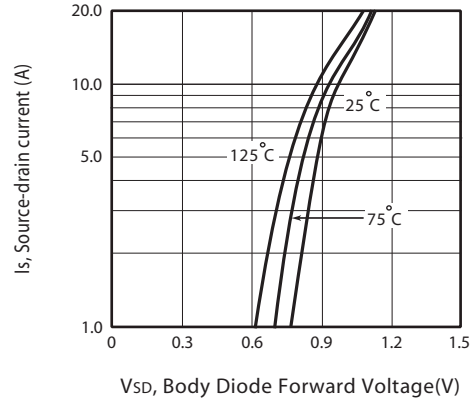


Figure 8. Body Diode Forward Voltage Variation with Source Current

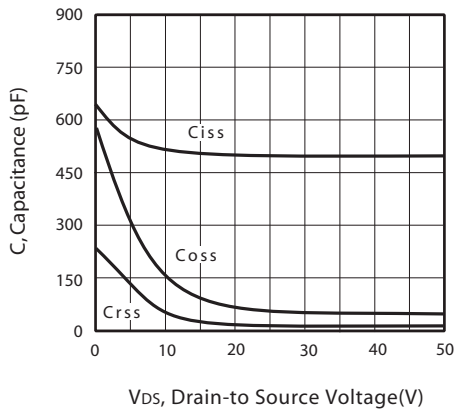


Figure 9. Capacitance

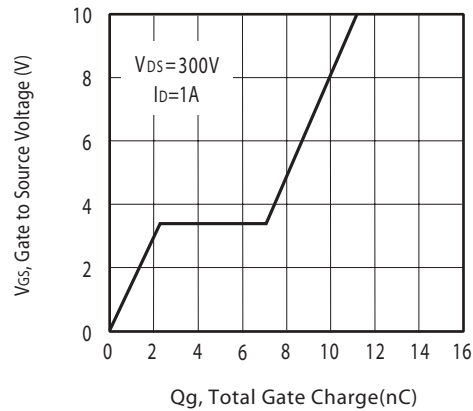


Figure 10. Gate Charge

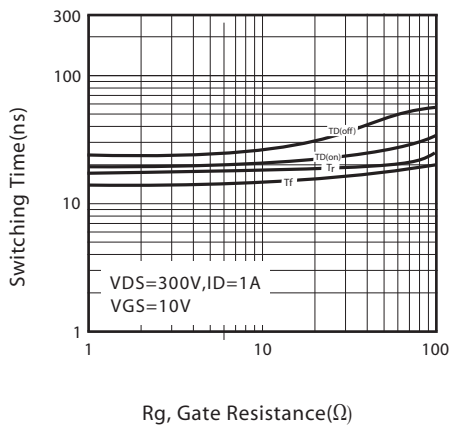


Figure 11. switching characteristics

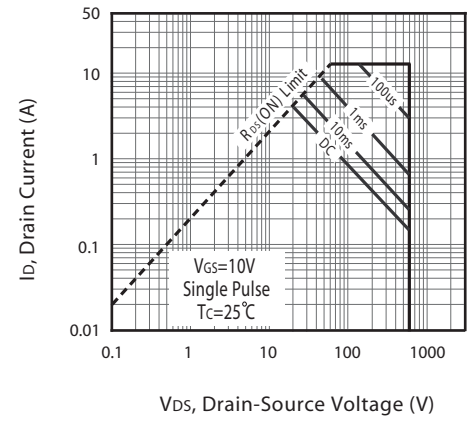
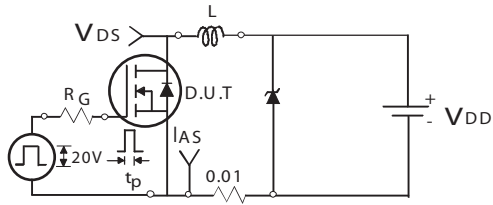
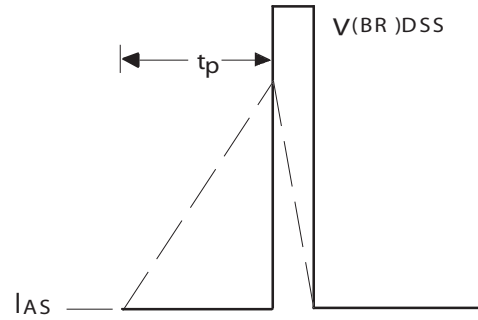


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

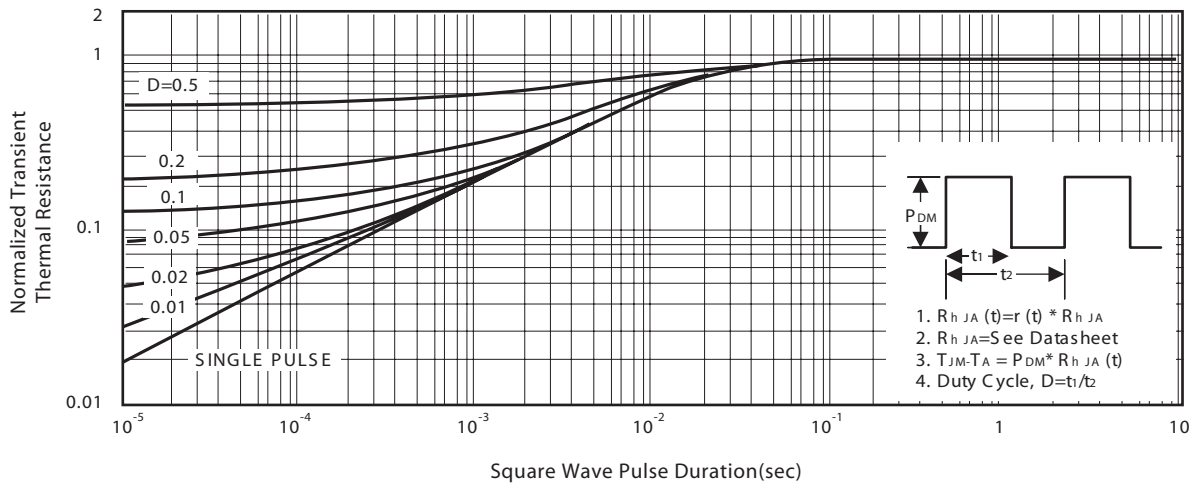
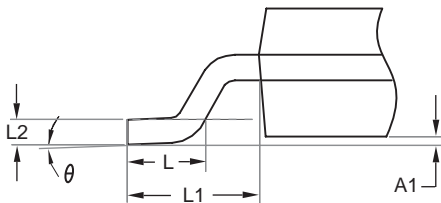
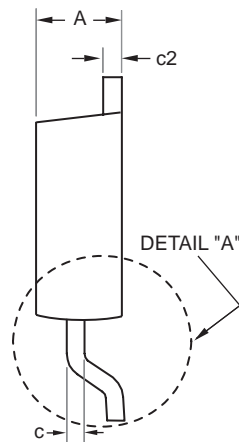
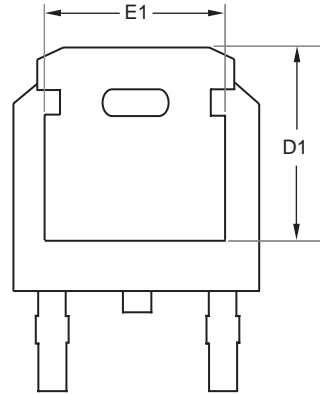
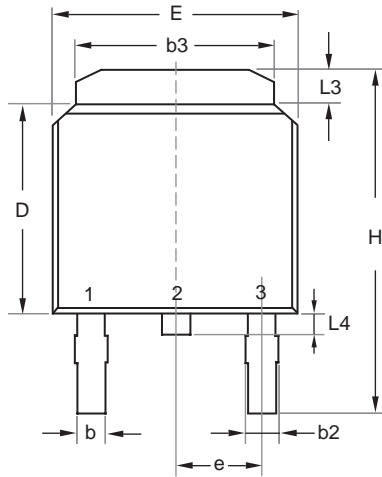


Figure 14. Normalized Thermal Transient Impedance Curve

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## TO-252



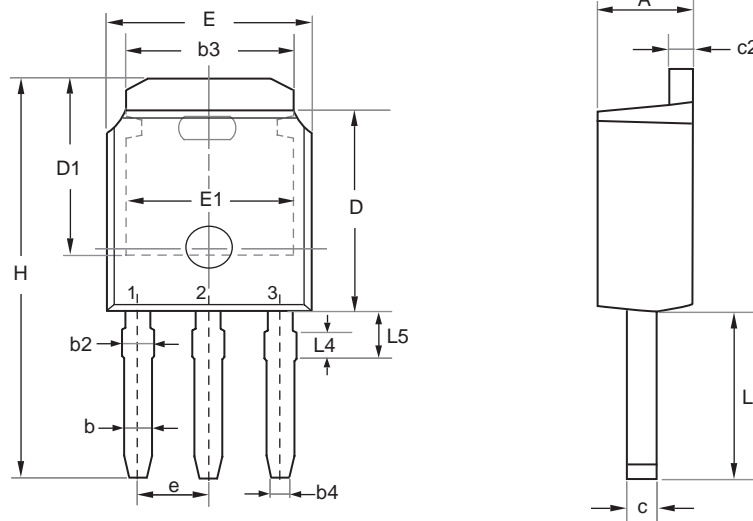
DETAIL "A"

SYMBOLS	MILLIMETERS	
	MIN	MAX
A	2.200	2.380
A1	0.000	0.127
b	0.635	0.889
b2	0.762	1.143
b3	5.200	5.460
c	0.450	0.600
c2	0.450	0.580
D	6.000	6.223
D1	5.210	5.380
e	2.286 BSC	
E	6.400	6.731
E1	4.318	4.900
H	9.400	10.400
L	1.400	1.770
L1	2.743 REF	
L2	0.508 BSC	
L3	0.890	1.270
L4	0.640	1.010
$\theta$	0°	10°

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## PACKAGE OUTLINE DIMENSIONS

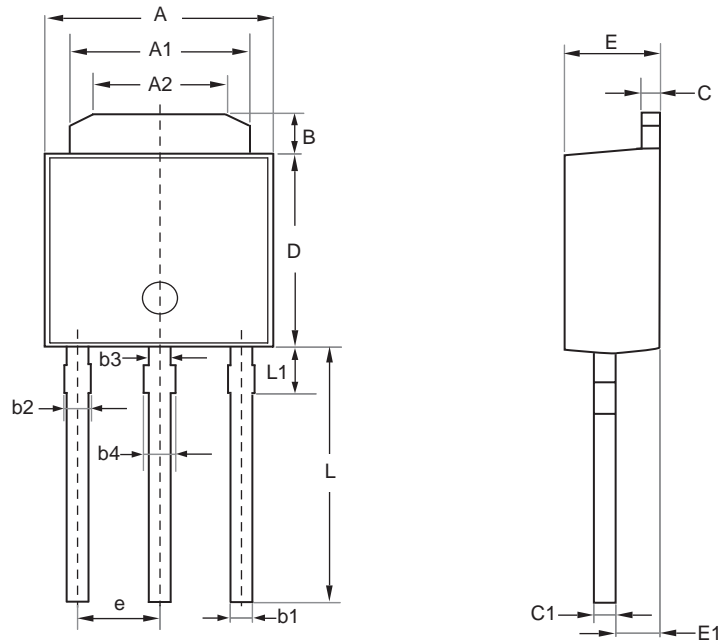
### TO-251S



SYMBOL	MILLIMETERS	
	MIN	MAX
E	6.350	6.731
L	3.700	4.400
L4	0.698 REF	
L5	0.972	1.226
D	5.970	6.223
H	9.670	11.450
b	0.630	0.850
b2	0.760	1.140
b3	4.950	5.460
b4	0.450	0.550
e	2.286 BSC	
A	2.180	2.390
c	0.400	0.610
c2	0.400	0.610
D1	5.100	---
E1	4.318	---

## PACKAGE OUTLINE DIMENSIONS

### TO-251L

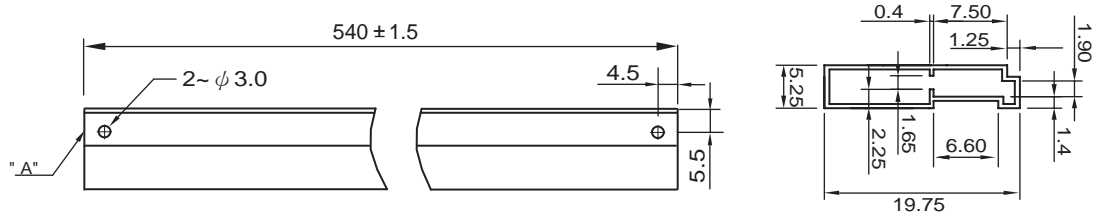


SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	6.40	6.50	6.60
A1	5.30	5.40	5.50
A2	4.30	4.40	4.50
B	1.35	1.50	1.65
L1	1.55 REF		
L	6.50	7.20	7.90
D	5.40	5.55	5.70
C	0.55	0.60	0.65
C1	0.49	0.54	0.59
E1	1.72	1.77	1.82
E	2.20	2.30	2.40
b1	0.60	—	0.75
b2	0.70	—	0.85
b3	0.80		
b4	0.90		
e	2.30		

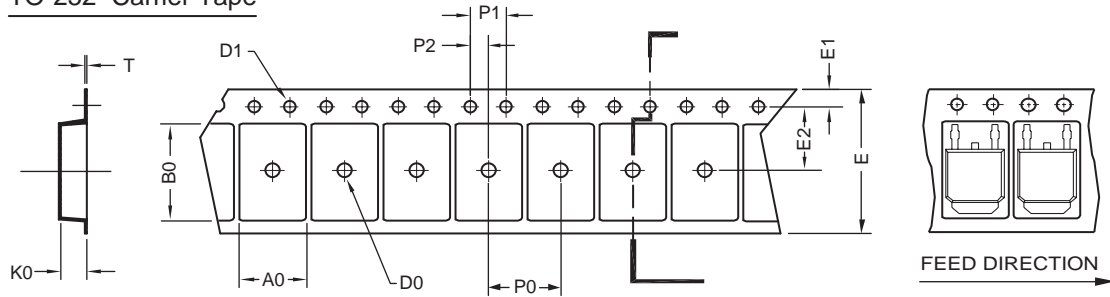


## TO-251 Tube/TO-252 Tape and Reel Data

### TO-251 Tube



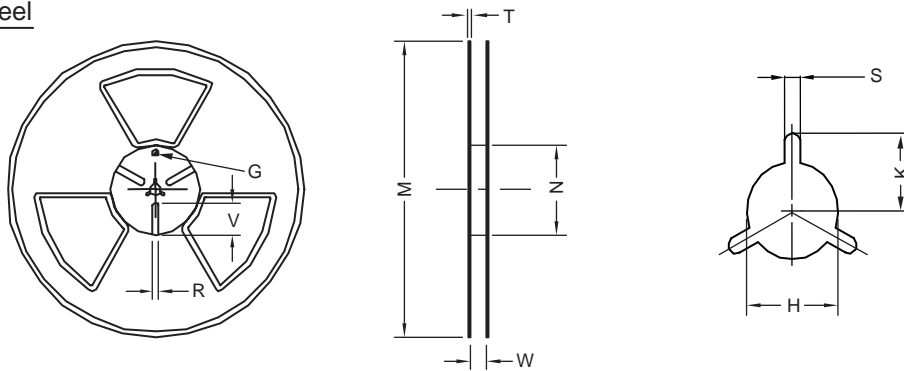
### TO-252 Carrier Tape



UNIT:mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TO-252 (16 mm)	6.96 ±0.1	10.49 ±0.1	2.79 ±0.1	φ 2	φ 1.5 +0.1 - 0	16.0 ±0.3	1.75 ±0.1	7.5 ±0.15	8.0 ±0.1	4.0 ±0.1	2.0 ±0.15	0.3 ±0.05

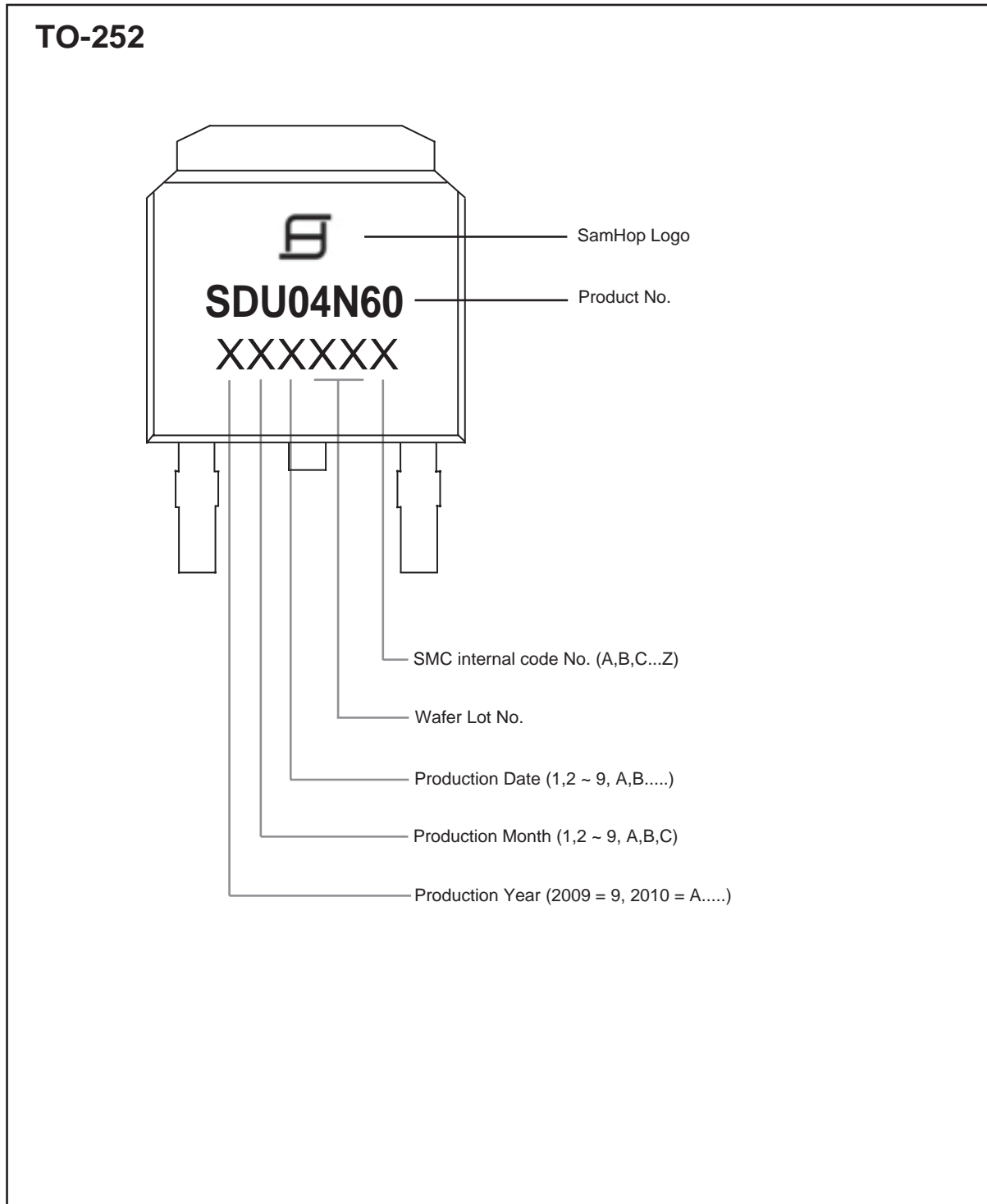
### TO-252 Reel



UNIT:mm

TAPE SIZE	REEL SIZE	M	N	W	T	H	K	S	G	R	V
16 mm	φ 330	φ 330 ± 0.5	φ 97 ± 1.0	17.0 + 1.5 - 0	2.2	φ 13.0 + 0.5 - 0.2	10.6	2.0 ±0.5	---	---	---

## TOP MARKING DEFINITION



## TOP MARKING DEFINITION

