

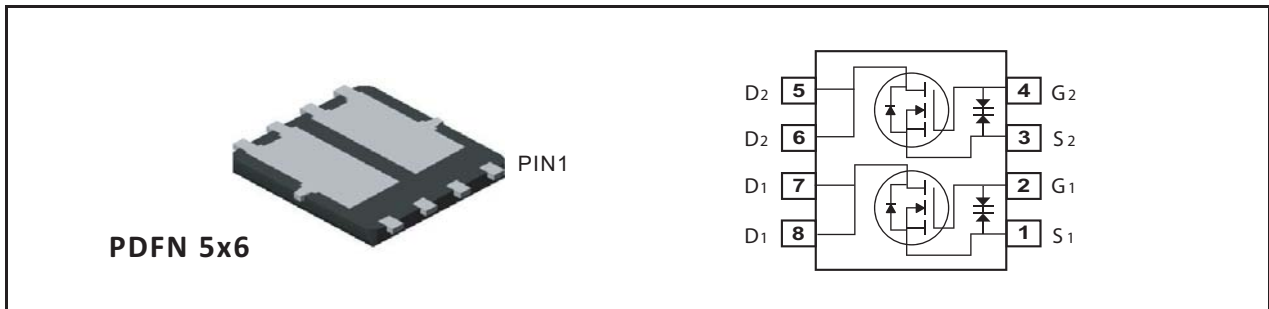


Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V _{DSS}	I _D	R _{DS(ON)} (mΩ) Max
35V	5A	85 @ V _{GS} =10V
		131 @ V _{GS} =4.5V

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units	
V _{DS}	Drain-Source Voltage	35	V	
V _{GS}	Gate-Source Voltage	±20	V	
I _D	Drain Current-Continuous ^c	T _A =25°C	5	A
		T _A =70°C	4	A
I _{DM}	-Pulsed ^{a,c}	21	A	
E _{AS}	Single Pulse Avalanche Energy ^d	6	mJ	
P _D	Maximum Power Dissipation	T _A =25°C	2.5	W
		T _A =70°C	1.6	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C	

THERMAL CHARACTERISTICS

R _{θJA}	Thermal Resistance, Junction-to-Ambient	50	°C/W
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ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	35			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =28V , V _{GS} =0V			1	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20V , V _{DS} =0V			±10	uA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	1.9	3	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V , I _D =2.5A		68	85	m ohm
		V _{GS} =4.5V , I _D =2.0A		97	131	m ohm
g _{FS}	Forward Transconductance	V _{DS} =10V , I _D =2.5A		7.5		S
SWITCHING CHARACTERISTICS ^b						
t _{D(ON)}	Turn-On Delay Time	V _{DD} =17.5V I _D =1A V _{GS} =10V R _{GEN} = 6 ohm		72		ns
t _r	Rise Time			174		ns
t _{D(OFF)}	Turn-Off Delay Time			1258		ns
t _f	Fall Time			666		ns
Q _g	Total Gate Charge	V _{DS} =17.5V, I _D =2.5A, V _{GS} =10V		3		nC
Q _{gs}	Gate-Source Charge	V _{DS} =17.5V, I _D =2.5A, V _{GS} =10V		0.78		nC
Q _{gd}	Gate-Drain Charge			1.3		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1A		0.82	1.2	V
Notes						
a. Pulse Test: Pulse Width ≤ 10us, Duty Cycle ≤ 1%. b. Guaranteed by design, not subject to production testing. c. Drain current limited by maximum junction temperature. d. Starting T _J =25°C, L=0.5mH, V _{DD} = 20V. (See Figure12) e. Mounted on FR4 Board of 1 inch ² , 2oz.						

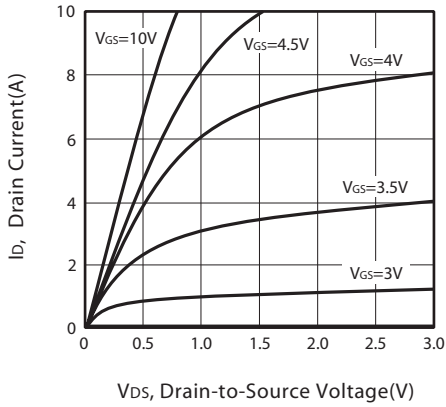


Figure 1. Output Characteristics

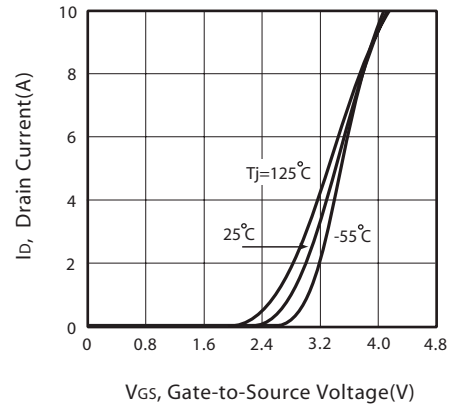


Figure 2. Transfer Characteristics

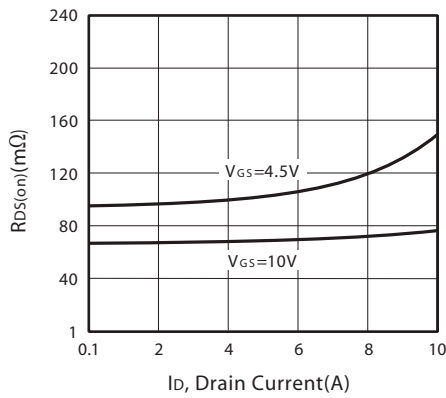


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

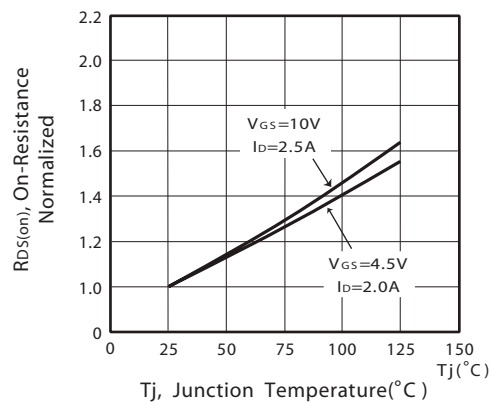


Figure 4. On-Resistance Variation with Drain Current and Temperature

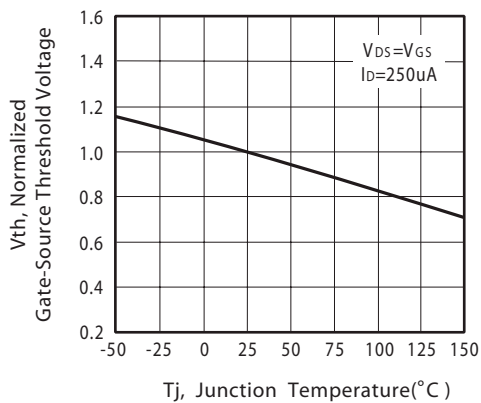


Figure 5. Gate Threshold Variation with Temperature

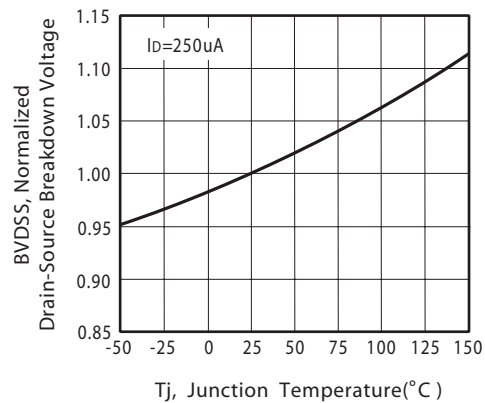


Figure 6. Breakdown Voltage Variation with Temperature

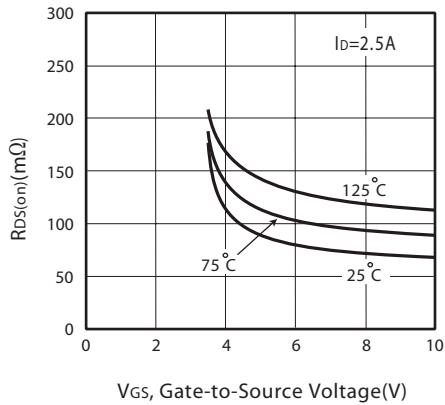


Figure 7. On-Resistance vs. Gate-Source Voltage

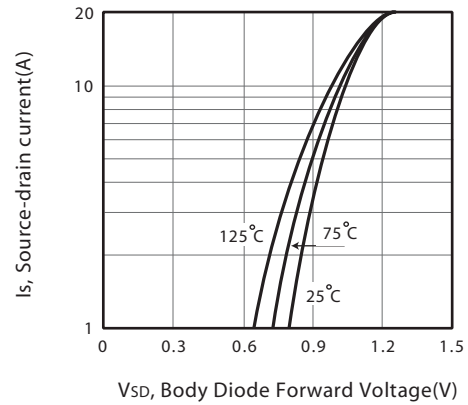


Figure 8. Body Diode Forward Voltage Variation with Source Current

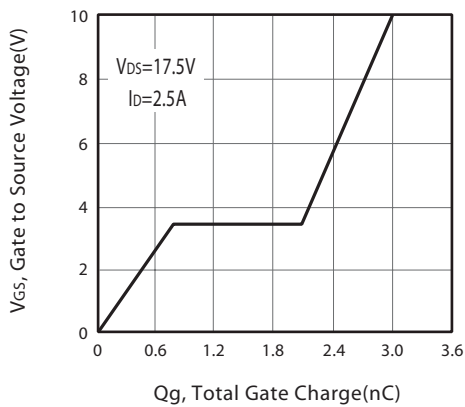


Figure 9. Gate Charge

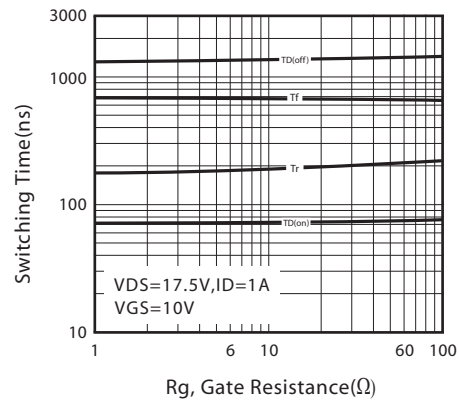


Figure 10. switching characteristics

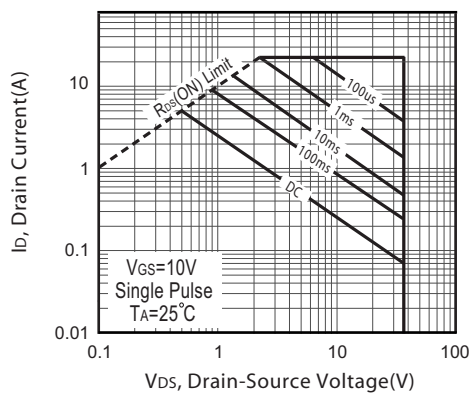
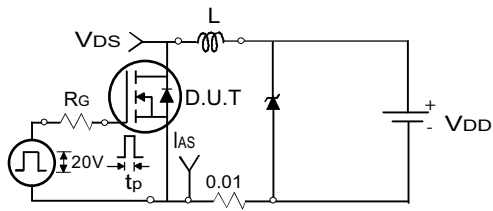
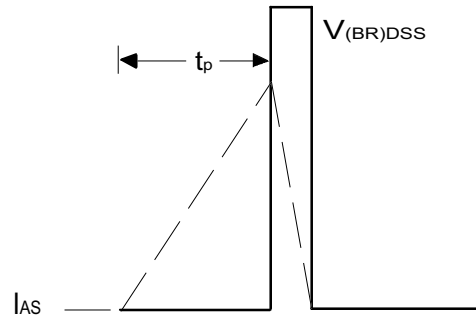


Figure 11. Maximum Safe Operating Area



Uncamped Inductive Test Circuit

Figure 12a.



Unclamped Inductive Waveforms

Figure 12b.

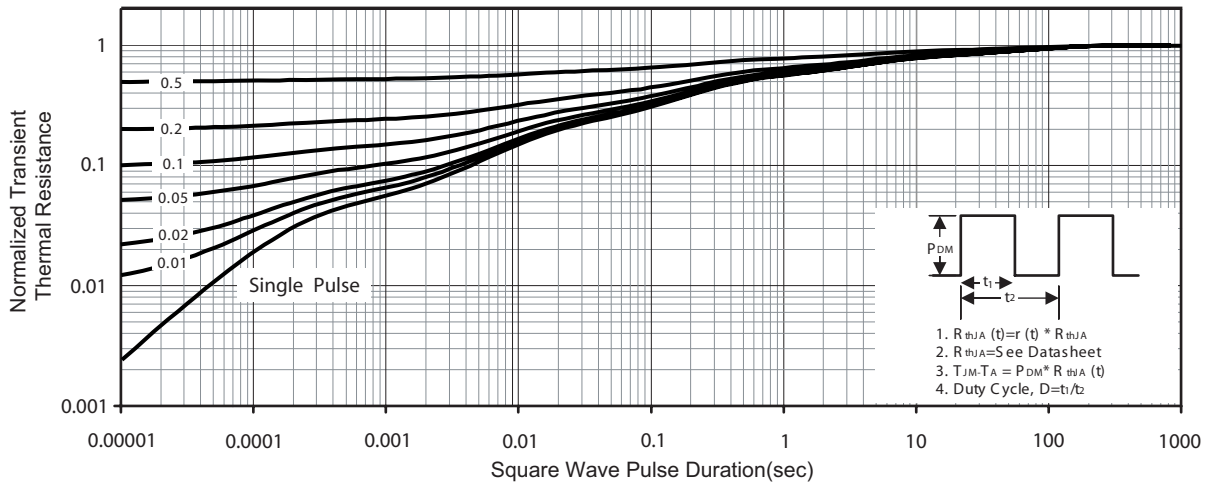
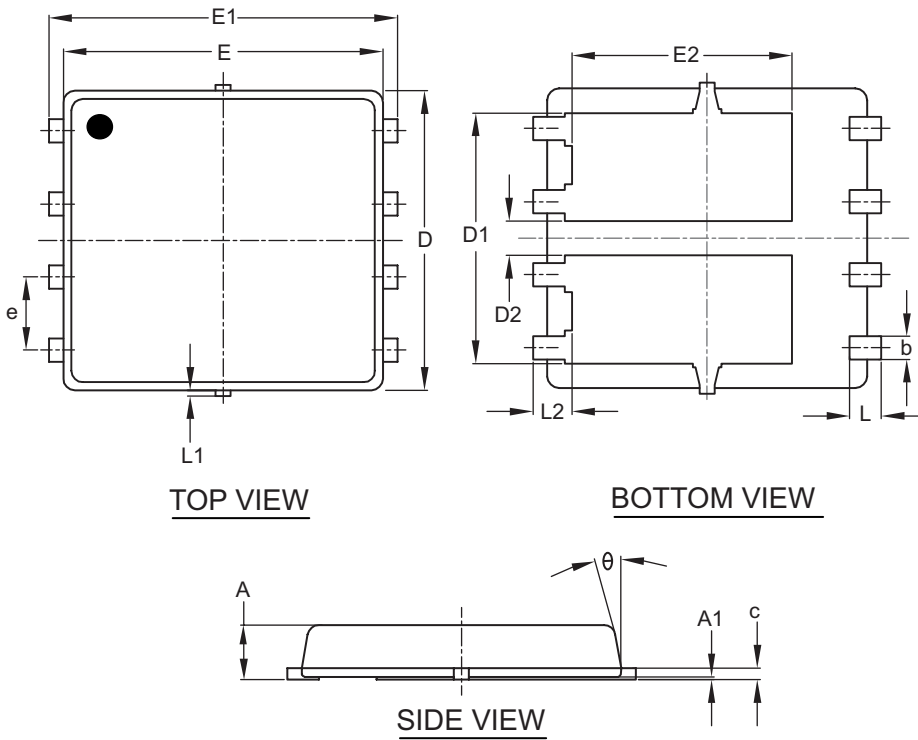


Figure 13. Normalized Thermal Transient Impedance Curve

PACKAGE OUTLINE DIMENSIONS

PDFN 5x6-8L



SYMBOLS	MILLIMETERS		
	MIN	NOM	MAX
A	0.85	0.95	1.00
A1	0.00	—	0.05
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	5.20 BSC		
D1	4.35 BSC		
D2	0.50	0.60	0.75
E	5.55 BSC		
E1	6.05 BSC		
E2	3.82 BSC		
e	1.27 BSC		
L	0.45	0.55	0.65
L1	0.00	—	0.15
L2	0.68 REF		
θ	0°	—	10°

TOP MARKING DEFINITION

