

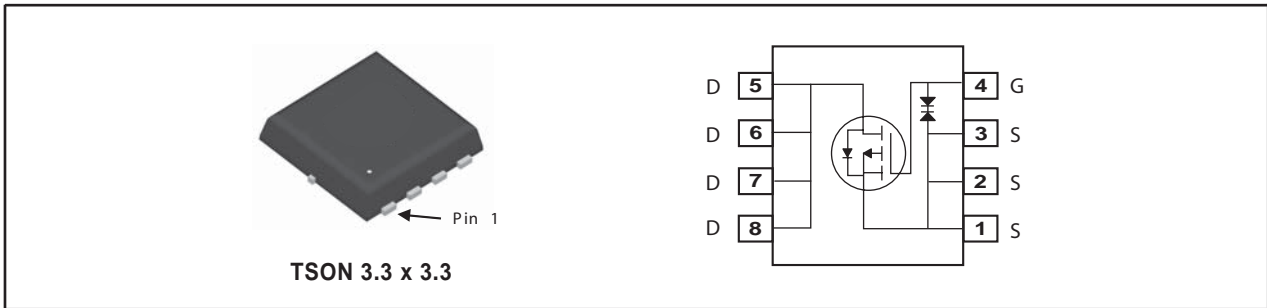


## P-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
-30V	-8A	12.5 @ V <sub>GS</sub> =-10V
		18 @ V <sub>GS</sub> =-4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	-30	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>a,c</sup>	T <sub>A</sub> =25°C	-8
		T <sub>A</sub> =70°C	-6.4
I <sub>DM</sub>	-Pulsed <sup>c</sup>	-46	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>	30	mJ
P <sub>D</sub>	Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> =25°C	1.67
		T <sub>A</sub> =70°C	1.07
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

### THERMAL CHARACTERISTICS

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	75	°C/W
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# SP4401

Ver 1.0

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V			-1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±10	uA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-1.0	-1.6	-3.0	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-4A		10	12.5	m ohm
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A		13	18	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-10V, I <sub>D</sub> =-4A		24		S
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V f=1.0MHz		3545		pF
C <sub>OSS</sub>	Output Capacitance			394		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			289		pF
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-15V I <sub>D</sub> =-1A V <sub>GS</sub> =-10V R <sub>GEN</sub> = 6 ohm		58		ns
t <sub>r</sub>	Rise Time			50		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			176		ns
t <sub>f</sub>	Fall Time			45		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-15V, I <sub>D</sub> =-4A, V <sub>GS</sub> =-10V		59		nC
		V <sub>DS</sub> =-15V, I <sub>D</sub> =-4A, V <sub>GS</sub> =-4.5V		28		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-15V, I <sub>D</sub> =-4A,		5		nC
Q <sub>gd</sub>	Gate-Drain Charge	V <sub>GS</sub> =-10V		14		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A		-0.8	-1.2	V

### Notes

- Surface Mounted on FR4 Board of 1 inch<sup>2</sup>, 1oz.
- Guaranteed by design, not subject to production testing.
- Drain current limited by maximum junction temperature.
- Starting T<sub>J</sub>=25°C, L=0.5mH, V<sub>DD</sub> = 20V. (See Figure13)

Jan,29,2014

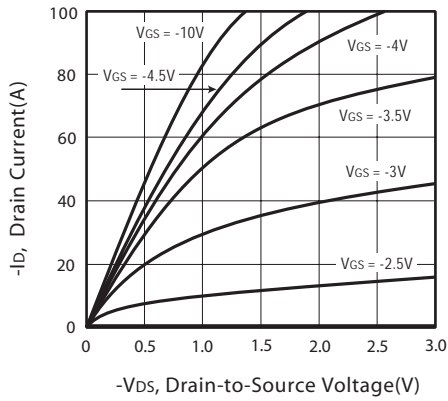


Figure 1. Output Characteristics

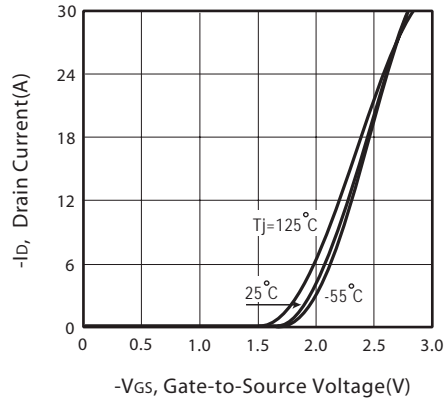


Figure 2. Transfer Characteristics

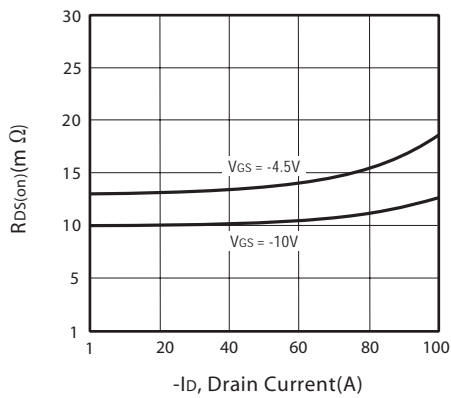


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

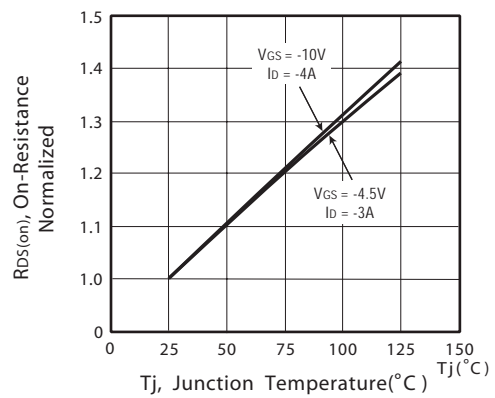


Figure 4. On-Resistance Variation with Drain Current and Temperature

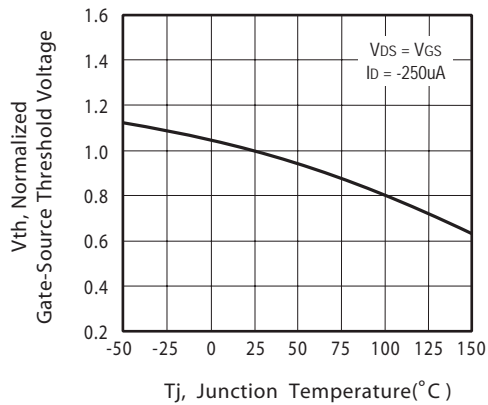


Figure 5. Gate Threshold Variation with Temperature

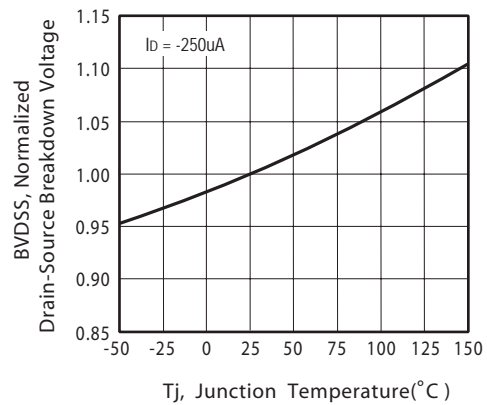


Figure 6. Breakdown Voltage Variation with Temperature

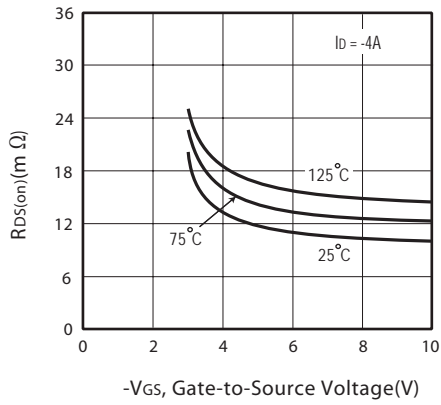


Figure 7. On-Resistance vs. Gate-Source Voltage

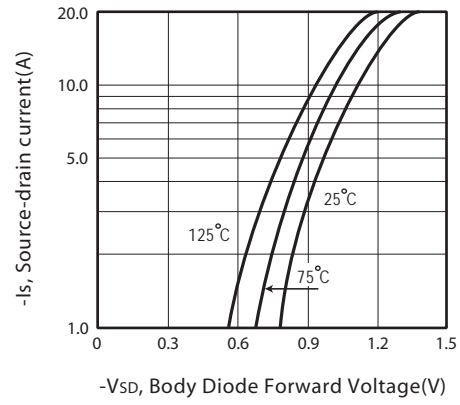


Figure 8. Body Diode Forward Voltage Variation with Source Current

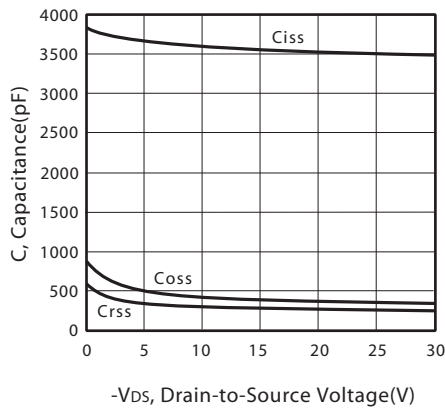


Figure 9. Capacitance

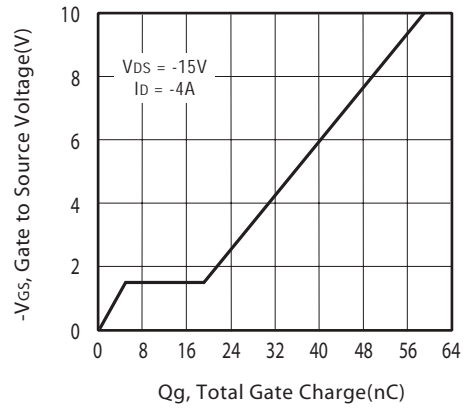


Figure 10. Gate Charge

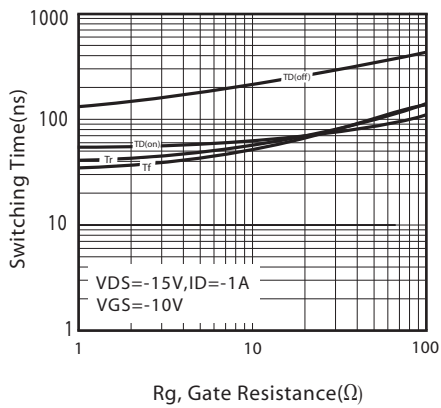


Figure 11. switching characteristics

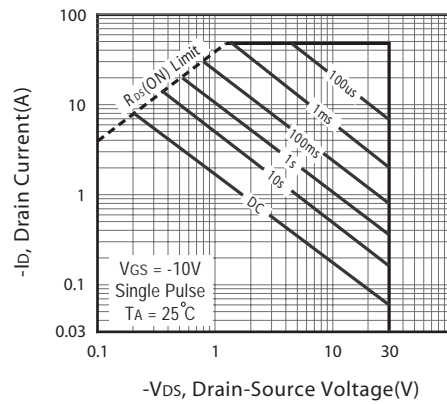
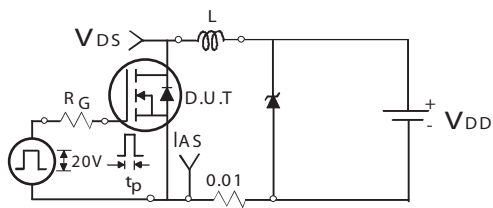
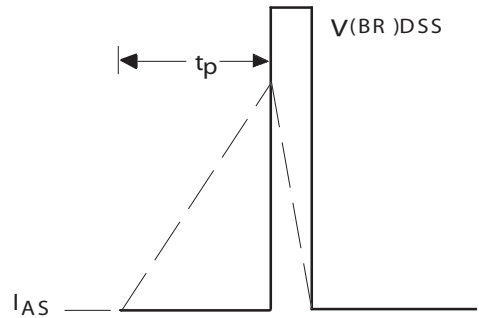


Figure 12. Maximum Safe Operating Area



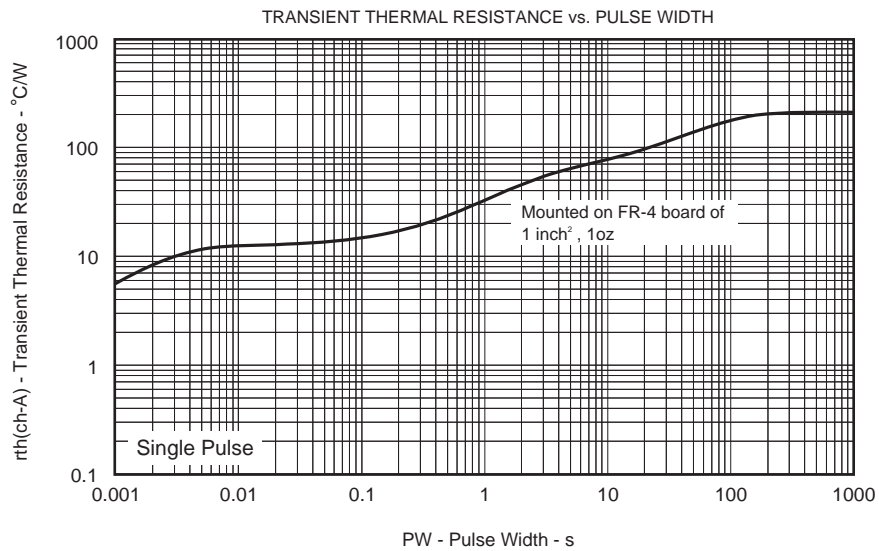
Unclamped Inductive Test Circuit

Figure 13a.



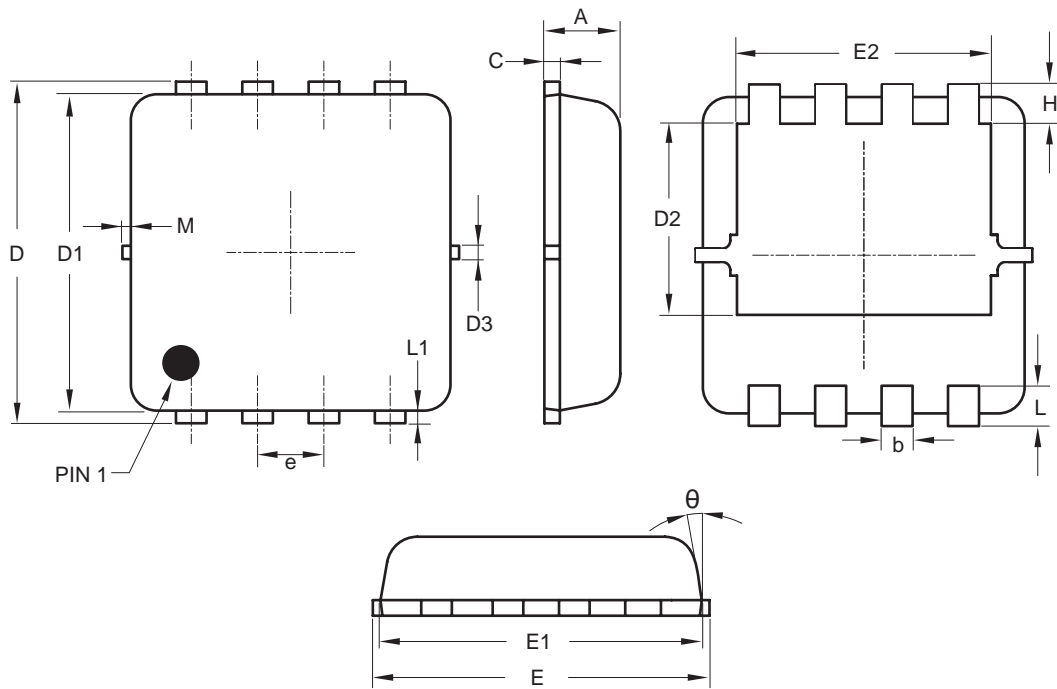
Unclamped Inductive Waveforms

Figure 13b.

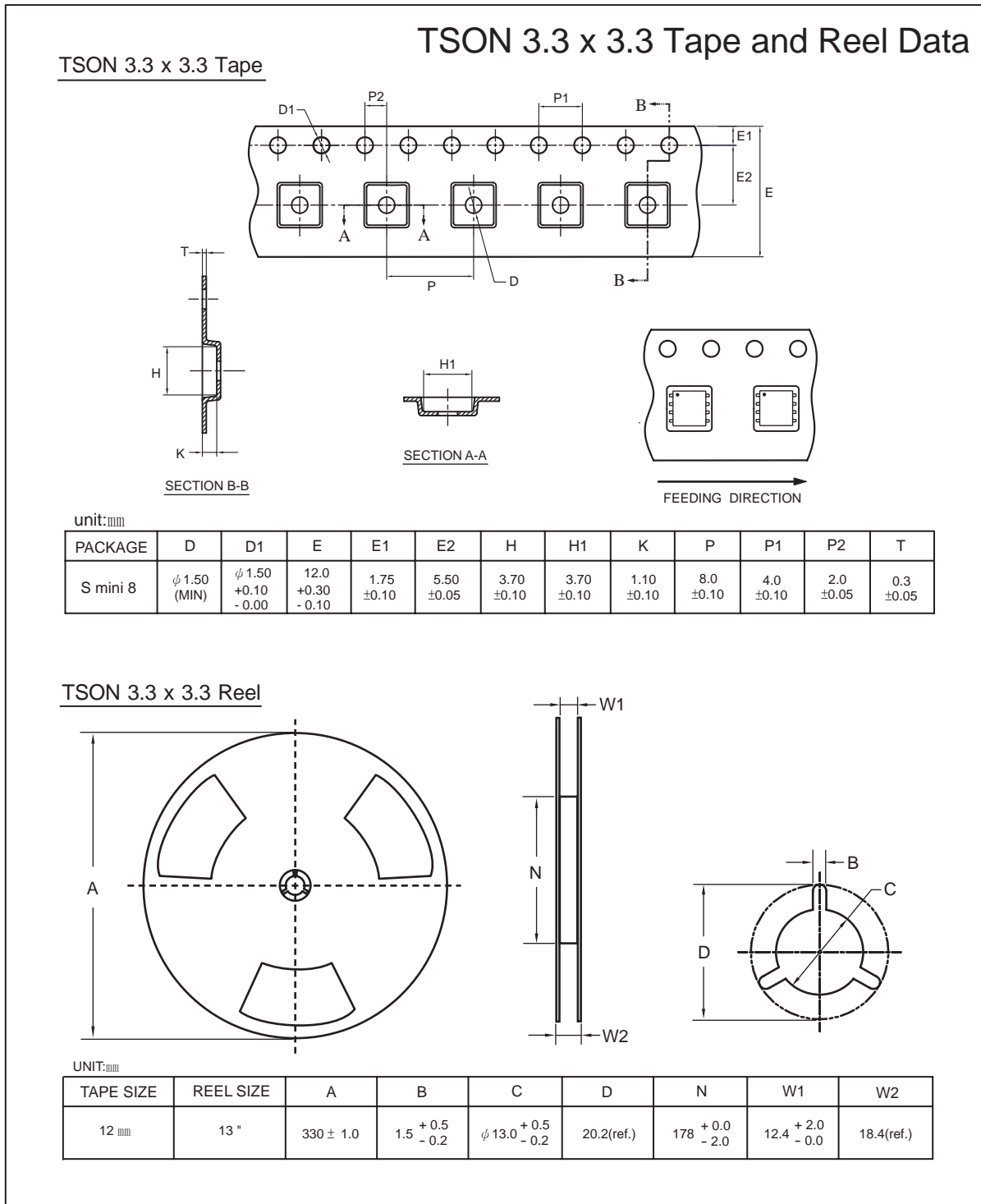


## PACKAGE OUTLINE DIMENSIONS

### TSON 3.3 x 3.3



SYMBOLS	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
C	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	—	0.13	—
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	—	0.13	—
M	—	—	0.15
θ	—	10°	12°



## TOP MARKING DEFINITION

