



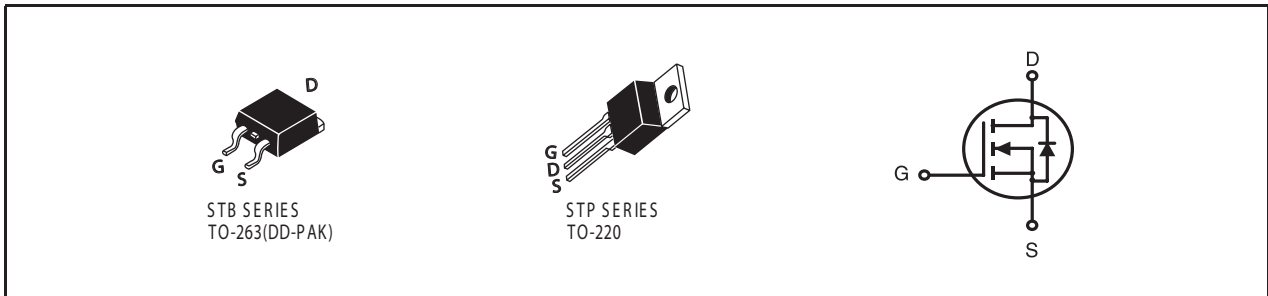
## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### PRODUCT SUMMARY

VDSS	ID	RDS(ON) (mΩ) Max
40V	60A	9 @ VGS=10V
		10 @ VGS=4.5V

### FEATURES

- Super high dense cell design for extremely low RDS(ON).
- High power and current handling capability.
- TO-220 & TO-263 package.



### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	40	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>A</sub> =25°C	60
		T <sub>A</sub> =70°C	50
I <sub>DM</sub>	-Pulsed <sup>b</sup>	240	A
E <sub>AS</sub>	Avalanche Energy <sup>c</sup>	196	mJ
P <sub>D</sub>	Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> =25°C	70
		T <sub>A</sub> =70°C	45
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

### THERMAL CHARACTERISTICS

R <sub>θ JC</sub>	Thermal Resistance, Junction-to-Case	1.8	°C/W
R <sub>θ JA</sub>	Thermal Resistance, Junction-to-Ambient	50	°C/W

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## ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =32V , V <sub>GS</sub> =0V			1	A
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b> <sup>a</sup>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	1.6	3	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =20A		7	9	m ohm
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =12A		8.5	10	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V , I <sub>D</sub> =20A		28.1		S
<b>DYNAMIC CHARACTERISTICS</b> <sup>b</sup>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V f=1.0MHz		1360		pF
C <sub>OSS</sub>	Output Capacitance			248.5		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			143		pF
<b>SWITCHING CHARACTERISTICS</b> <sup>b</sup>						
t <sub>D(ON)</sub>	Turn-On DelayTime	V <sub>DD</sub> =20V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>GEN</sub> =6 ohm		24		ns
t <sub>r</sub>	Rise Time			25		ns
t <sub>D(OFF)</sub>	Turn-Off DelayTime			67		ns
t <sub>f</sub>	Fall Time			32		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =20V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V		26		nC
		V <sub>DS</sub> =20V, I <sub>D</sub> =20A, V <sub>GS</sub> =4.5V		12.5		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =20V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V		2.8		nC
Q <sub>gd</sub>	Gate-Drain Charge			6		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				2	A
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =2A		0.74	1.3	V
<b>Notes</b> a. Pulse Test: Pulse Width ≤ 300us, Duty Cicle ≤ 2%. b. Guaranteed by design, not subject to production testing. c. Starting T <sub>J</sub> =25°C, V <sub>DD</sub> =40V, V <sub>GS</sub> =10V, L=0.5mH. (See Figure13)						

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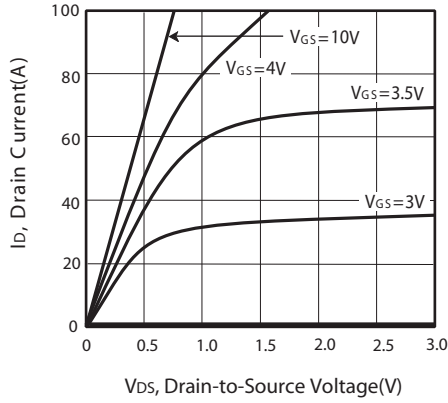


Figure 1. Output Characteristics

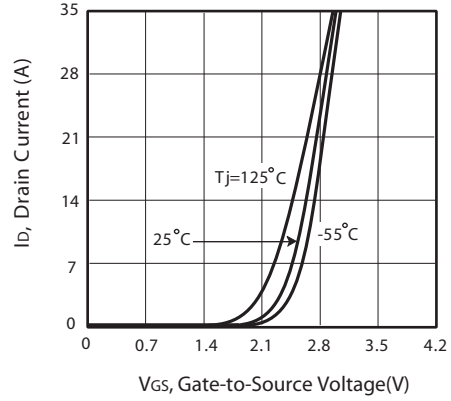


Figure 2. Transfer Characteristics

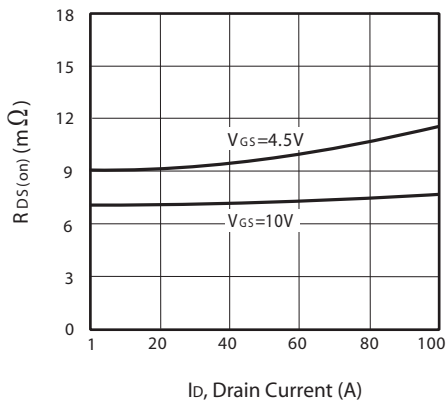


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

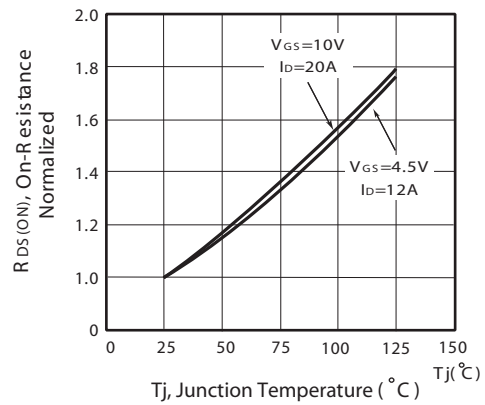


Figure 4. On-Resistance Variation with Drain Current and Temperature

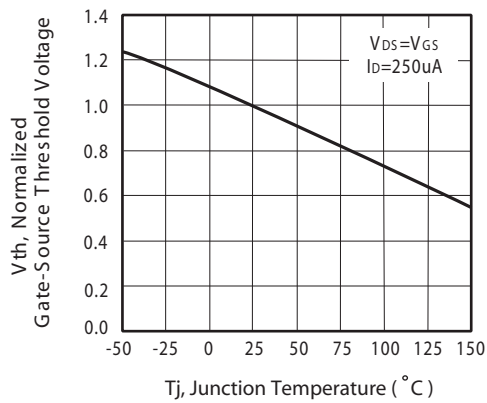


Figure 5. Gate Threshold Variation with Temperature

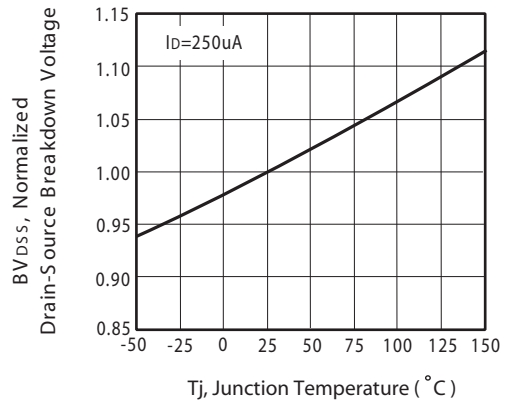


Figure 6. Breakdown Voltage Variation with Temperature

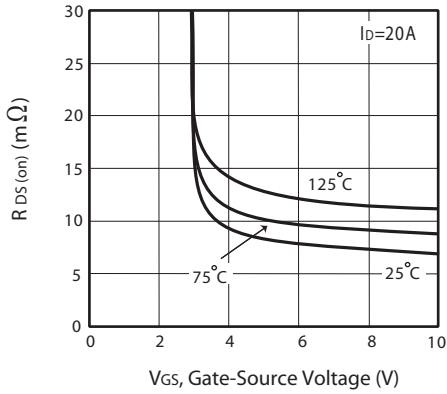


Figure 7. On-Resistance vs. Gate-Source Voltage

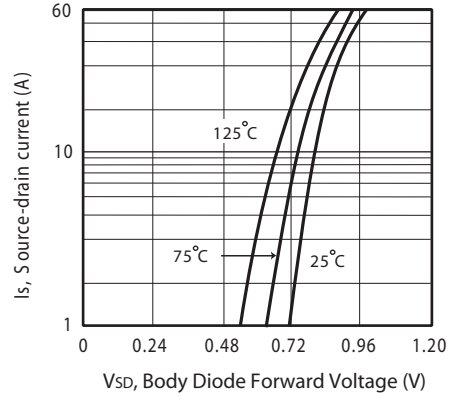


Figure 8. Body Diode Forward Voltage Variation with Source Current

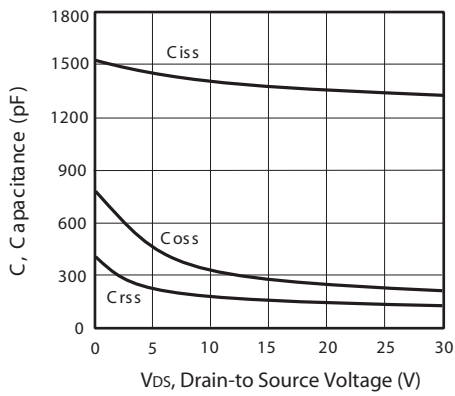


Figure 9. Capacitance

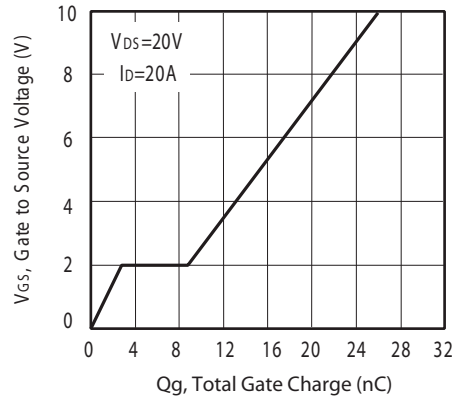


Figure 10. Gate Charge

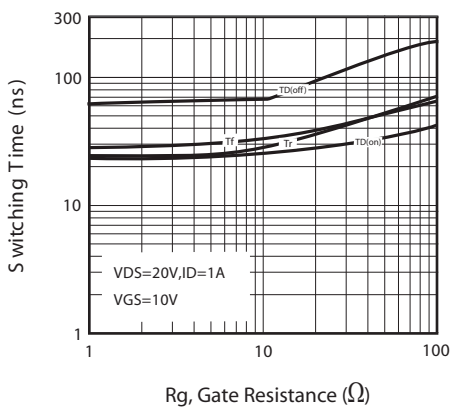


Figure 11. Switching Characteristics

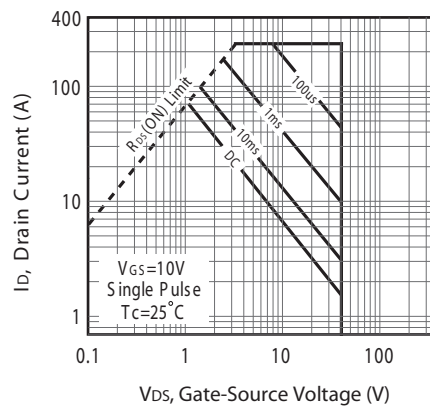
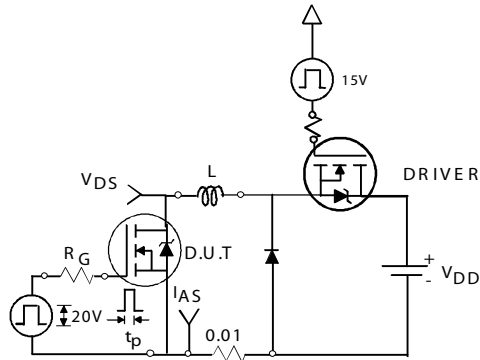
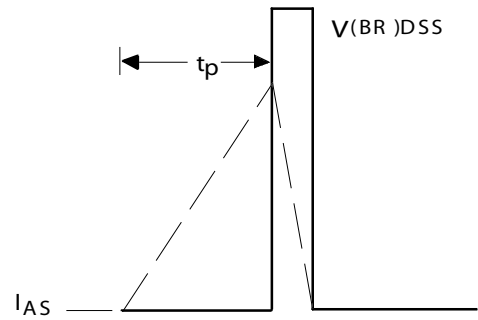


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

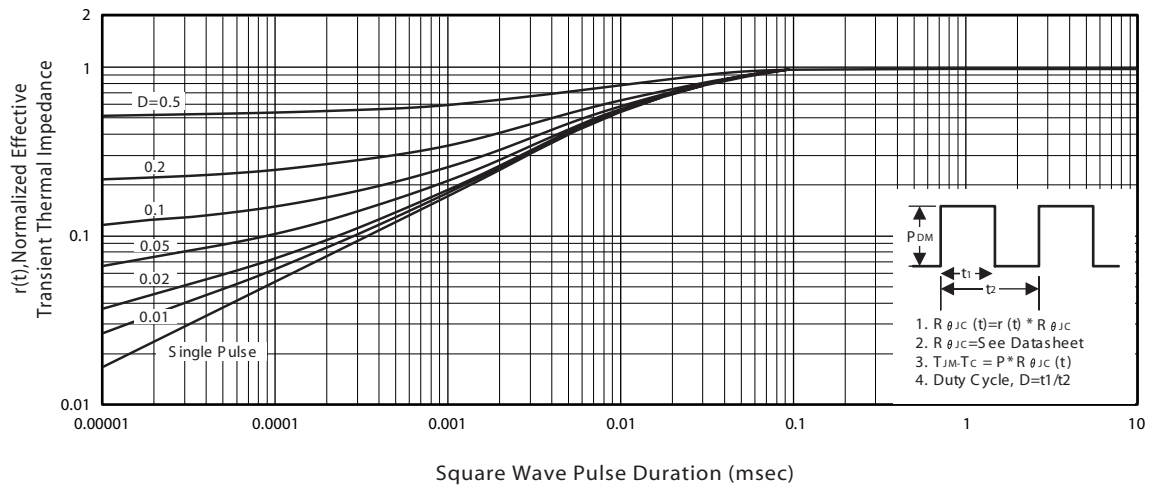


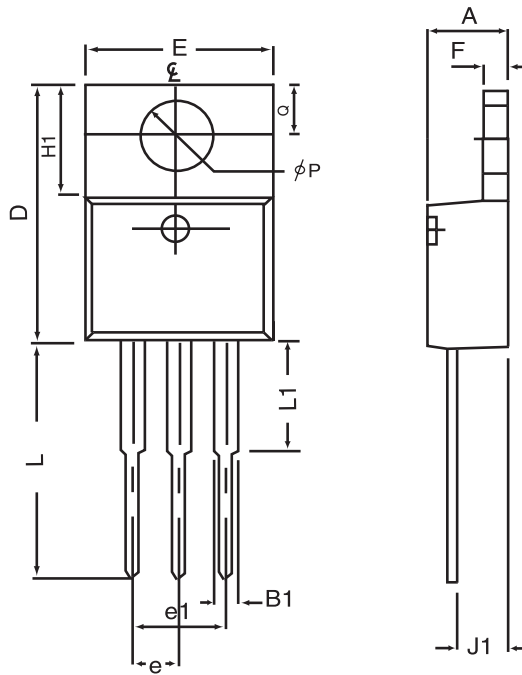
Figure 14. Normalized Thermal Transient Impedance Curve

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## PACKAGE OUTLINE DIMENSIONS

TO-220

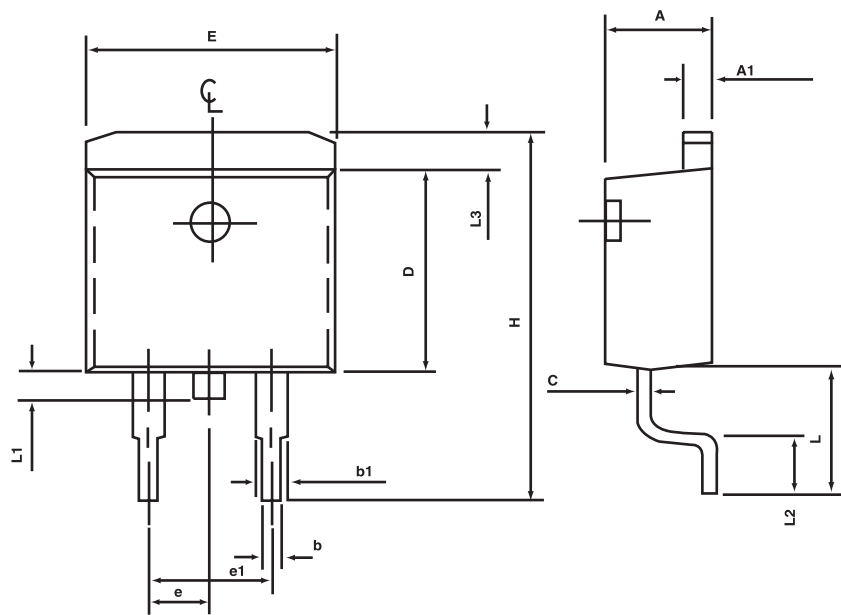


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	4.80	0.170	0.189
B1	1.27	1.65	0.050	0.630
D	14.6	16.00	0.575	0.610
E	9.70	10.41	0.382	0.410
e	2.34	2.74	0.092	0.108
e1	4.68	5.48	0.184	0.216
F	1.14	1.40	0.045	0.055
H1	5.97	6.73	0.235	0.265
J1	2.20	2.79	0.087	0.110
L	12.88	14.22	0.507	0.560
L1	3.00	6.35	0.120	0.250
phi P	3.50	3.94	0.138	0.155
Q	2.54	3.05	0.100	0.120

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## PACKAGE OUTLINE DIMENSIONS

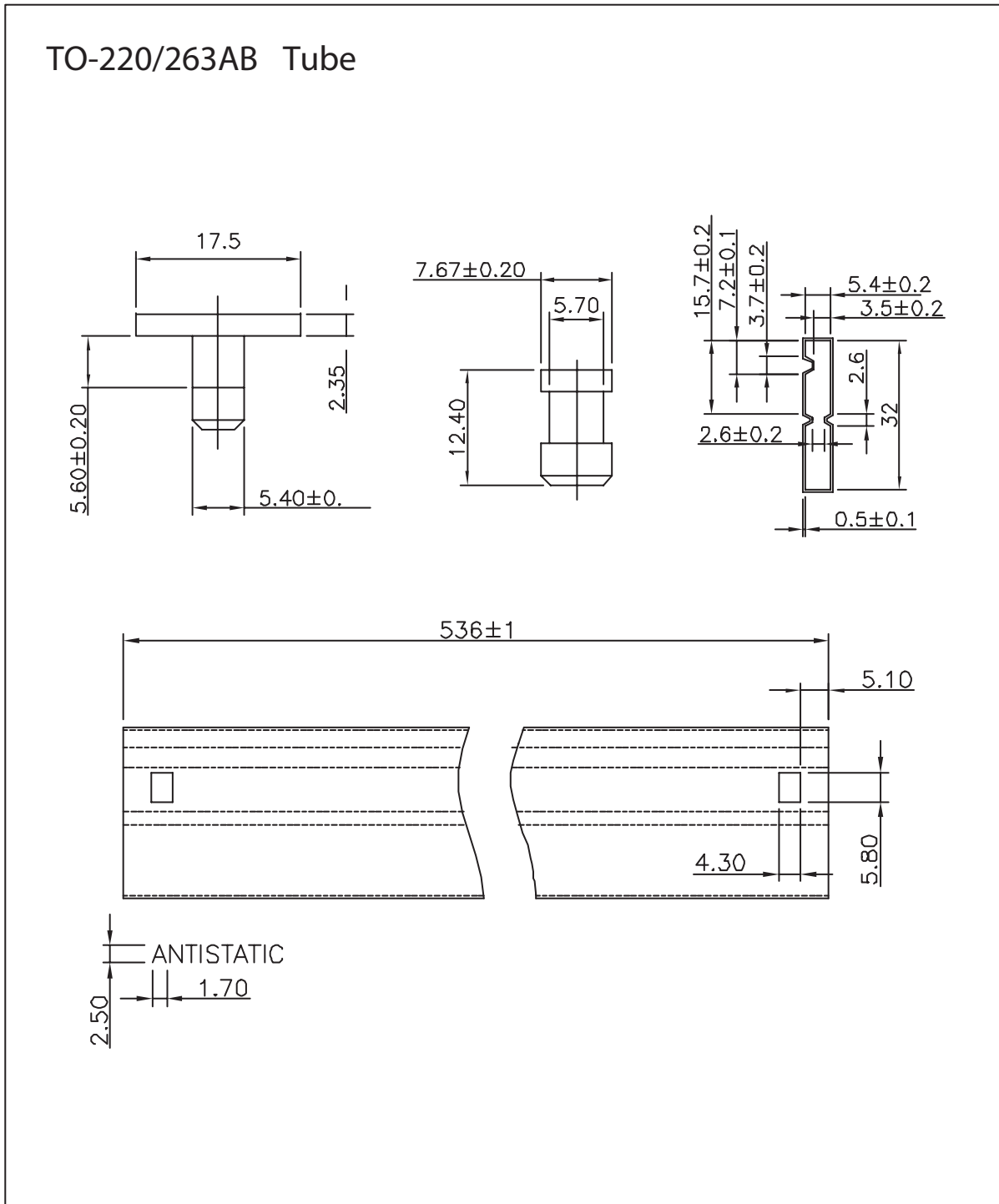
### TO-263AB



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.70	0.169	0.185
A1	1.22	1.32	0.048	0.055
b	0.69	0.94	0.027	0.037
b1	1.22	1.40	0.048	0.055
C	0.36	0.56	0.014	0.022
D	8.64	9.652	0.340	0.380
E	9.70	10.54	0.382	0.415
e	2.29	2.79	0.090	0.110
e1	4.83	5.33	0.190	0.210
H	14.60	15.78	0.575	0.625
L	4.70	5.84	0.185	0.230
L1	1.20	1.778	0.047	0.070
L2	2.24	2.84	0.088	0.111
L3	1.40 MAX		0.055 MAX	

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Feb.05,2009