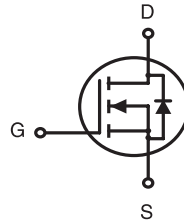


**N-Channel Logic Level Enhancement Mode Field Effect Transistor****PRODUCT SUMMARY**

VDSS	ID	RDS(ON) (mΩ) Max
100V	12A	140 @ VGS=10V
		170 @ VGS=4.5V

FEATURES

- Super high dense cell design for low RDS(ON).
- Rugged and reliable.
- TO-251 Package.

STD SERIES
TO-251(1-PAK)**ABSOLUTE MAXIMUM RATINGS (TA=25°C unless otherwise noted)**

Symbol	Parameter	Limit	Units
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	±20	V
I _D	Drain Current-Continuous ^a	T _C =25°C	12
		T _C =70°C	9.6
I _{DM}	-Pulsed ^b	35	A
E _{AS}	Single Pulse Avalanche Energy ^d	36	mJ
P _D	Maximum Power Dissipation ^a	T _C =25°C	45
		T _C =70°C	29
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C

THERMAL CHARACTERISTICS

R _{θJC}	Thermal Resistance, Junction-to-Case ^a	2.8	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient ^a	50	°C/W

STD12L01A

Ver 2.0

ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V , V _{GS} =0V			1	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20V , V _{DS} =0V			±100	nA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	1.8	3	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V , I _D =6A		112	140	m ohm
		V _{GS} =4.5V , I _D =5.5A		130	170	m ohm
g _{FS}	Forward Transconductance	V _{DS} =10V , I _D =6A		15		S
DYNAMIC CHARACTERISTICS ^c						
C _{ISS}	Input Capacitance	V _{DS} =25V, V _{GS} =0V f=1.0MHz		700		pF
C _{OSS}	Output Capacitance			48		pF
C _{RSS}	Reverse Transfer Capacitance			31		pF
SWITCHING CHARACTERISTICS ^c						
t _{D(ON)}	Turn-On Delay Time	V _{DD} =50V I _D =1A V _{GS} =10V R _{GEN} = 6 ohm		13		ns
t _r	Rise Time			11.5		ns
t _{D(OFF)}	Turn-Off Delay Time			23		ns
t _f	Fall Time			10		ns
Q _g	Total Gate Charge	V _{DS} =50V, I _D =6A, V _{GS} =10V		11.5		nC
		V _{DS} =50V, I _D =6A, V _{GS} =4.5V		6		nC
Q _{gs}	Gate-Source Charge	V _{DS} =50V, I _D =6A, V _{GS} =10V		1.5		nC
Q _{gd}	Gate-Drain Charge			3.3		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1A		0.78	1.3	V

Notes

- Surface Mounted on FR4 Board, t ≤ 10sec.
- Pulse Test: Pulse Width ≤ 300us, Duty Cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.
- Starting T_J=25°C, L=0.5mH, V_{DD} = 50V. (See Figure13)

Oct,15,2010

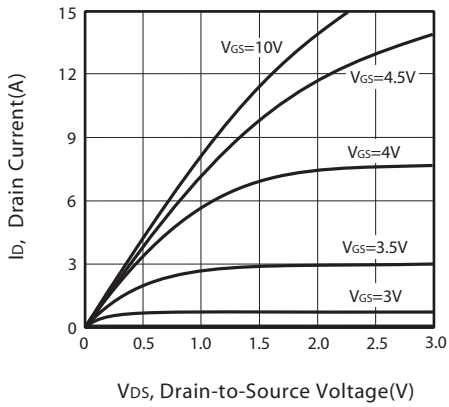


Figure 1. Output Characteristics

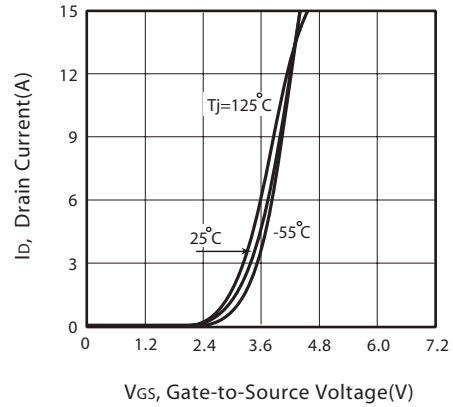


Figure 2. Transfer Characteristics

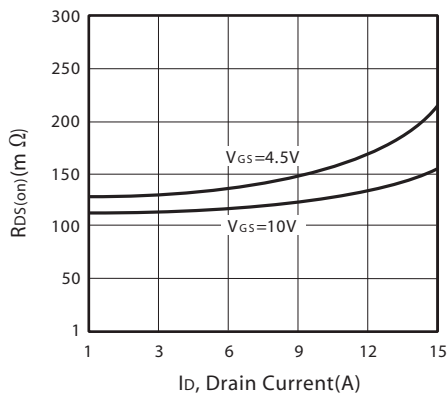


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

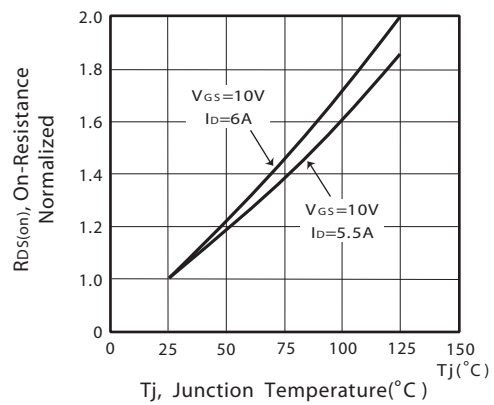


Figure 4. On-Resistance Variation with Drain Current and Temperature

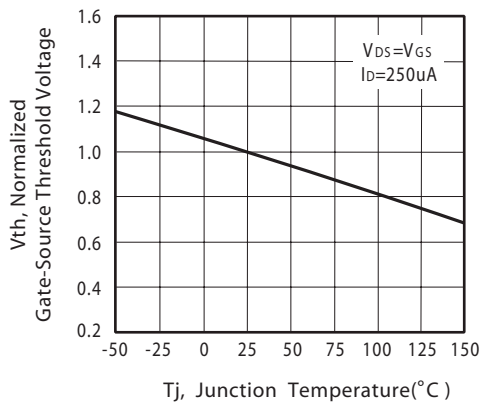


Figure 5. Gate Threshold Variation with Temperature

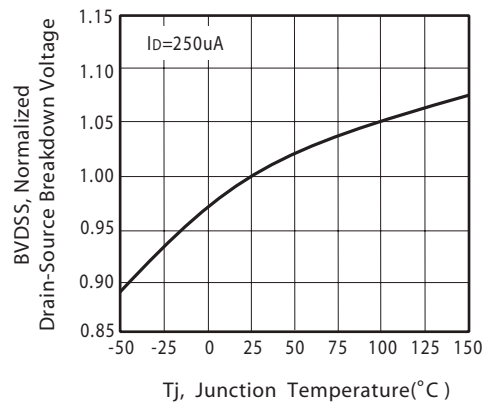
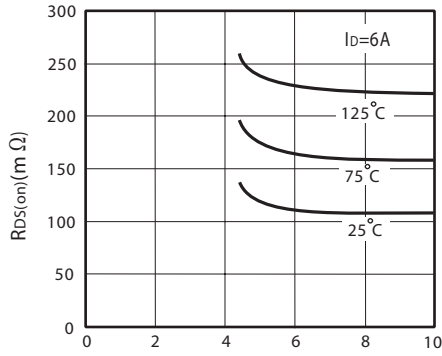
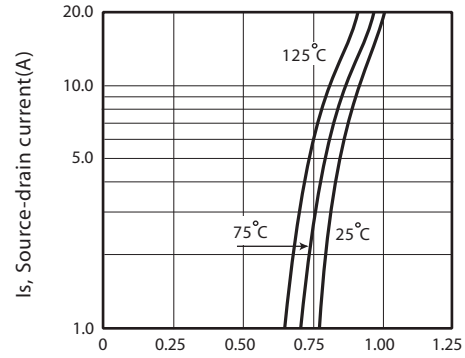


Figure 6. Breakdown Voltage Variation with Temperature



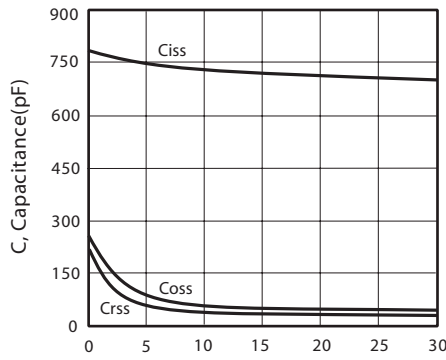
V_{GS} , Gate-to-Source Voltage(V)

Figure 7. On-Resistance vs. Gate-Source Voltage



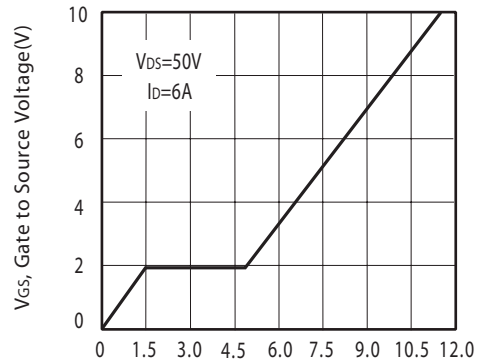
V_{DS} , Body Diode Forward Voltage(V)

Figure 8. Body Diode Forward Voltage Variation with Source Current



V_{DS} , Drain-to-Source Voltage(V)

Figure 9. Capacitance



Q_g , Total Gate Charge(nC)

Figure 10. Gate Charge

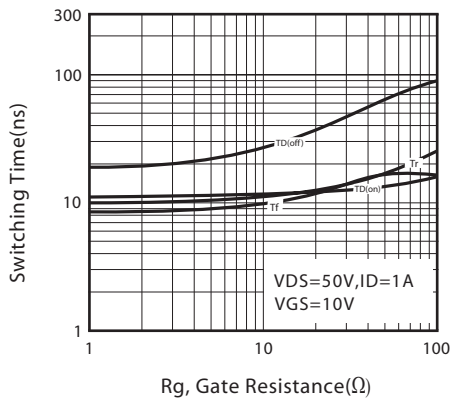


Figure 11. switching characteristics

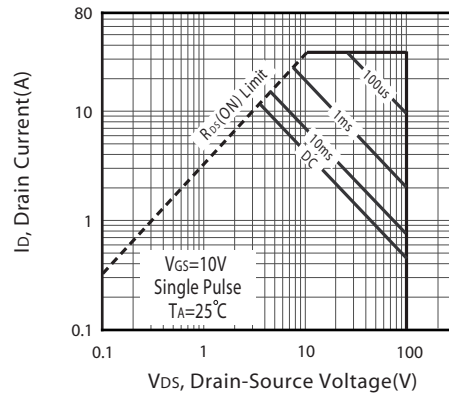
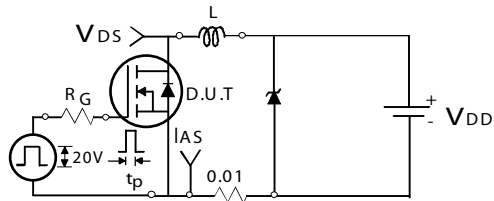


Figure 12. Maximum Safe Operating Area

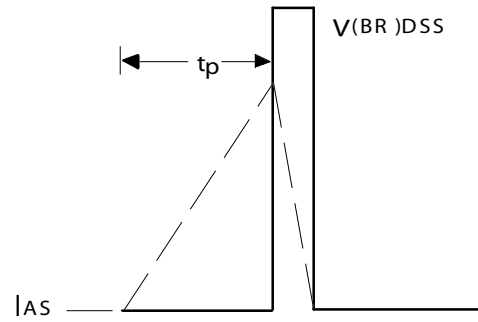
STD12L01A

Ver 2.0



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

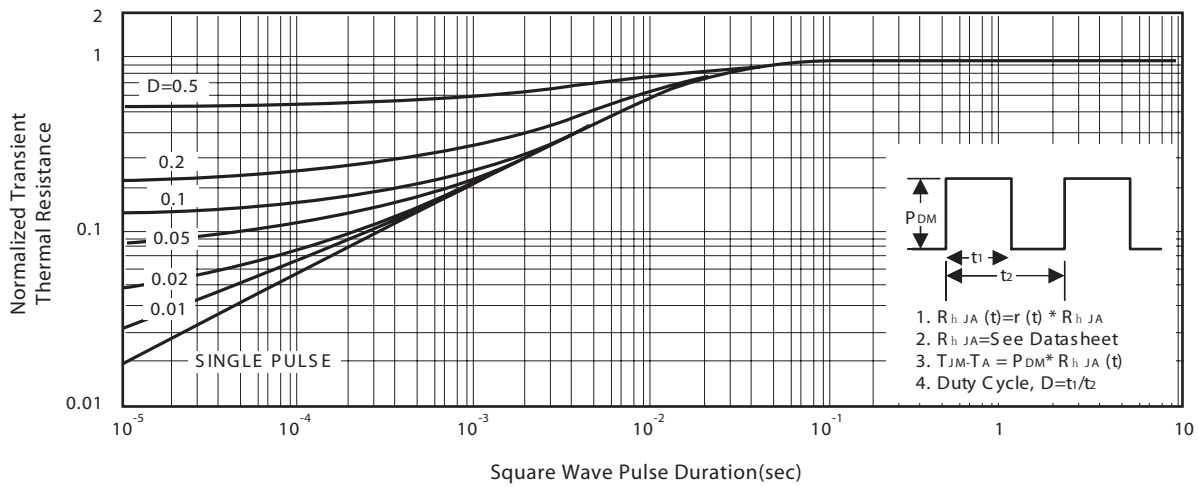


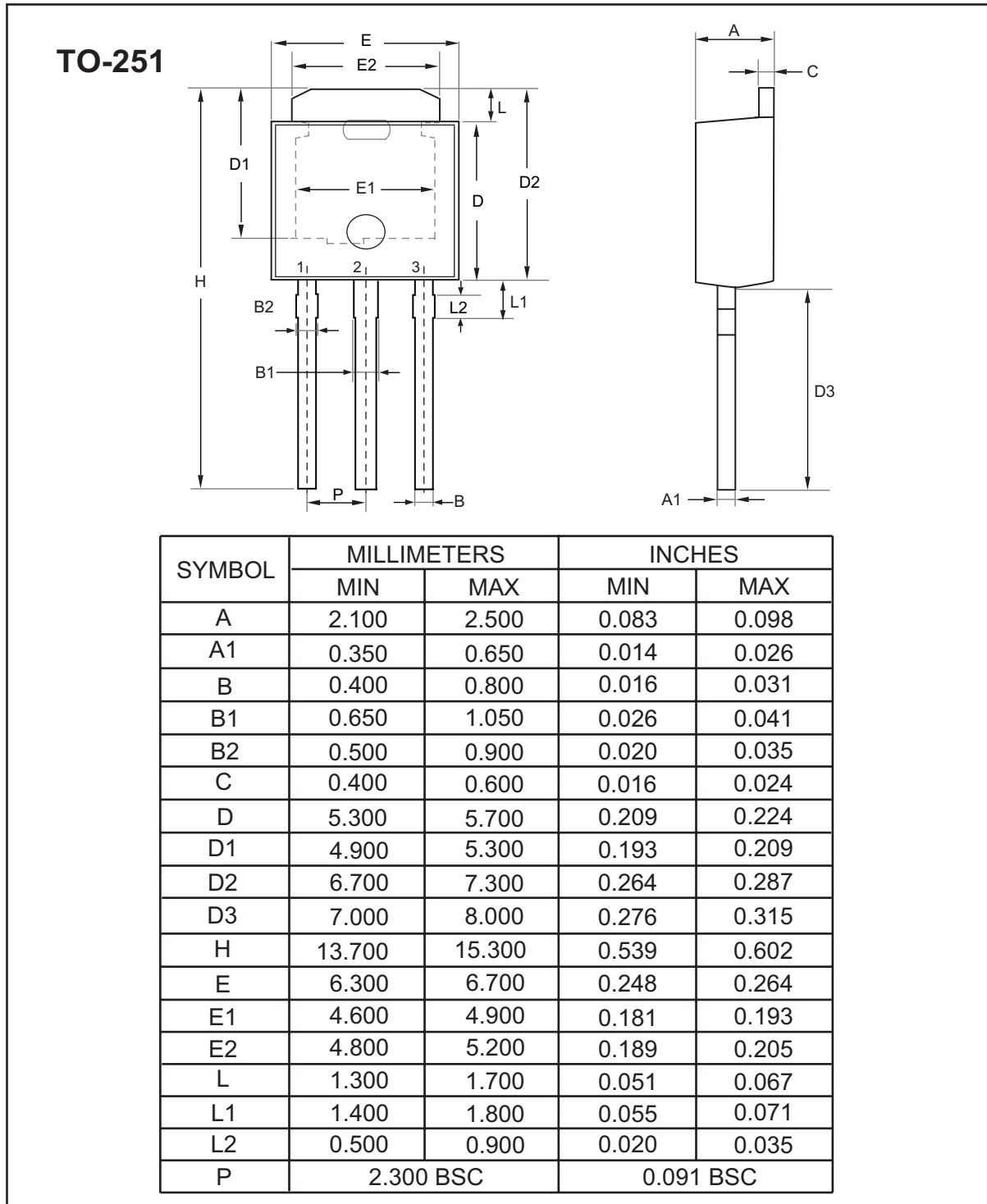
Figure 14. Normalized Thermal Transient Impedance Curve

Oct,15,2010

STD12L01A

Ver 2.0

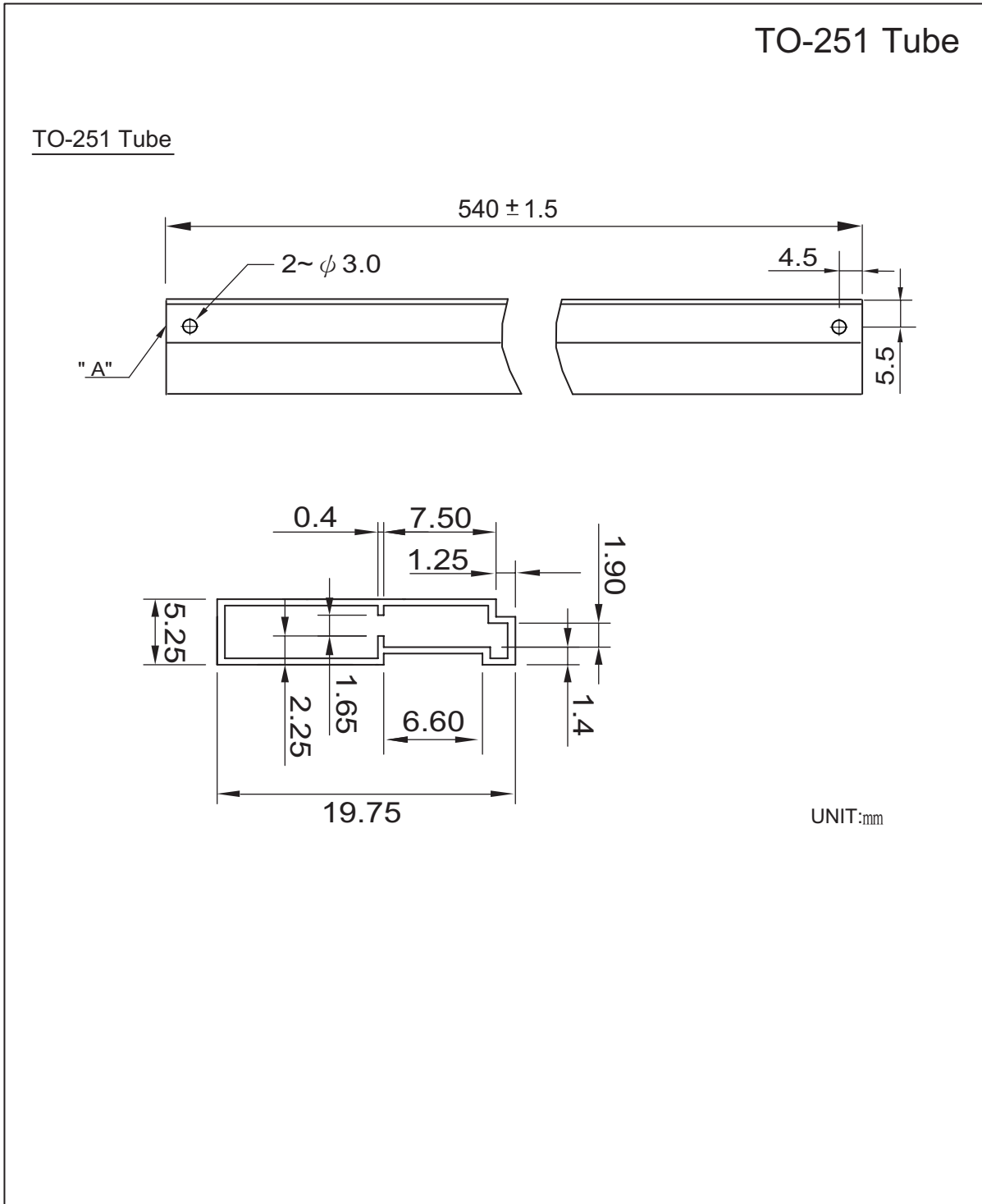
PACKAGE OUTLINE DIMENSIONS



Oct,15,2010

STD12L01A

Ver 2.0



Oct,15,2010