SamHop Microelectronics Corp.

STG8810

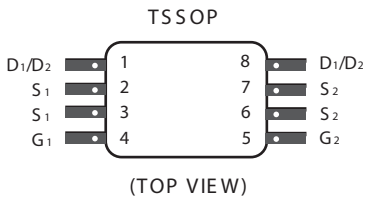
Ver 2.0

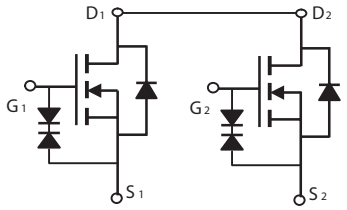
Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V_{DSS}	I_D	$R_{DS(ON)}$ (mΩ) Max
20V	7A	18.5 @ VGS=4.5V
		19.5 @ VGS=4.0V
		20.0 @ VGS=3.7V
		23.0 @ VGS=3.1V
		28.5 @ VGS=2.5V

FEATURES

- Super high dense cell design for low $R_{DS(ON)}$.
- Rugged and reliable.
- Suface Mount Package.
- ESD HBM > 2KV.





ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Symbol	Parameter		Limit	Units
V_{DS}	Drain-Source Voltage		20	V
V_{GS}	Gate-Source Voltage		±12	V
I_D	Drain Current-Continuous [a]	T_A=25°C	7.0	A
		T_A=70°C	5.6	A
I_{DM}	-Pulsed [b]		28	A
P_D	Maximum Power Dissipation [a]	T_A=25°C	1.5	W
		T_A=70°C	1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to 150	°C

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient [a]	85	°C/W

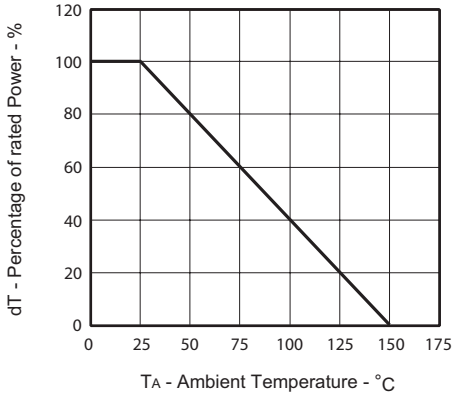
ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=16V , V_{GS}=0V			1	uA
I_{GSS}	Gate-Body Leakage Current	V_{GS}= ±12V , V_{DS}=0V			±10	uA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} , I_D=1mA	0.5	0.9	1.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=4.5V , I_D=3.5A	14.0	16.5	18.5	m ohm
		V_{GS}=4.0V , I_D=3.5A	14.5	17.0	19.5	m ohm
		V_{GS}=3.7V , I_D=3.5A	15.0	17.5	20.0	m ohm
		V_{GS}=3.1V , I_D=3.5A	16.0	19.5	23.0	m ohm
		V_{GS}=2.5V , I_D=3.5A	18.0	23.5	28.5	m ohm
g_{FS}	Forward Transconductance	V_{DS}=5V , I_D=3.5A		19		S
DYNAMIC CHARACTERISTICS [c]						
C_{ISS}	Input Capacitance	V_{DS}=10V,V_{GS}=0V f=1.0MHz		300		pF
C_{OSS}	Output Capacitance			151		pF
C_{RSS}	Reverse Transfer Capacitance			71		pF
SWITCHING CHARACTERISTICS [c]						
$t_{D(ON)}$	Turn-On Delay Time	V_{DD}=16V I_D=3.5A V_{GS}=4.5V R_{GEN}= 6 ohm		61		ns
t_r	Rise Time			295		ns
$t_{D(OFF)}$	Turn-Off Delay Time			821		ns
t_f	Fall Time			580		ns
Q_g	Total Gate Charge	V_{DS}=16V,I_D=7A, V_{GS}=4.5V		9		nC
Q_{gs}	Gate-Source Charge			1.5		nC
Q_{gd}	Gate-Drain Charge			5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_S=1.0A		0.78	1.2	V

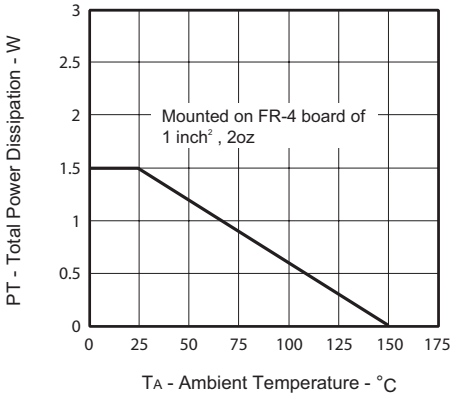
Notes

a.Surface Mounted on FR4 Board,t ≤ 10sec.
b.Pulse Test:Pulse Width ≤ 10us, Duty Cycle ≤ 1%.
c.Guaranteed by design, not subject to production testing.

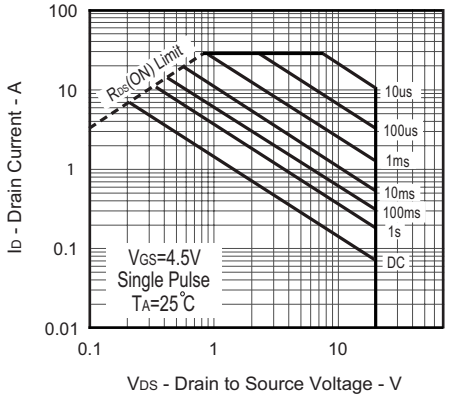
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



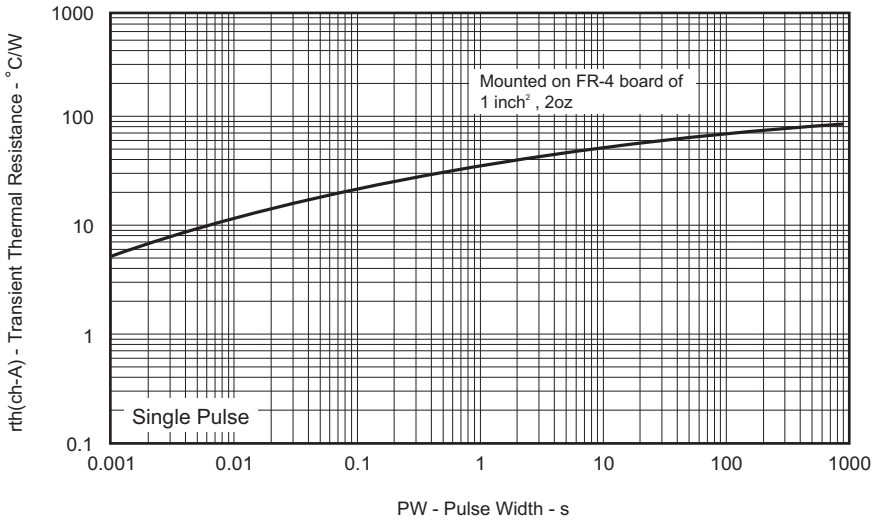
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



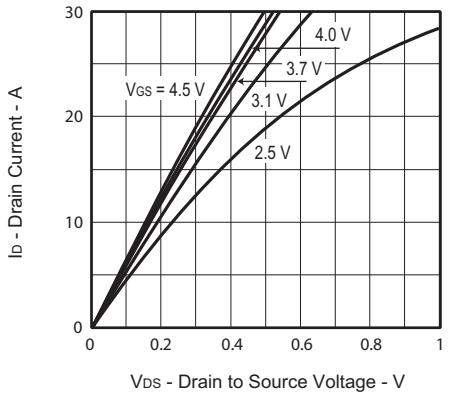
FORWARD BIAS SAFE OPERATING AREA



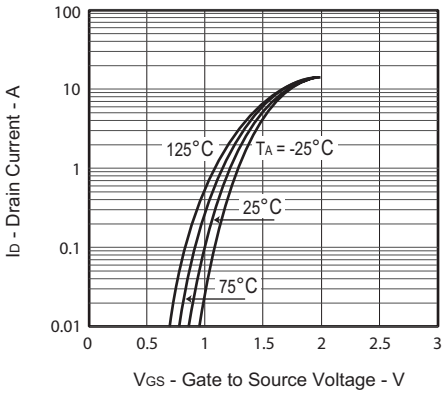
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



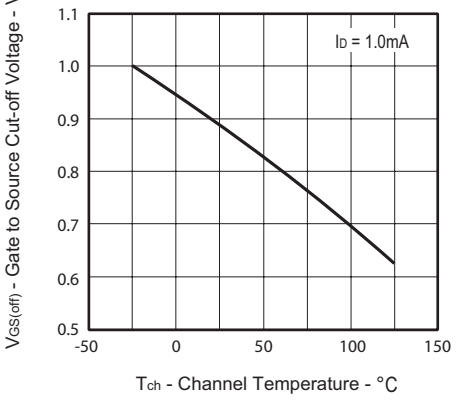
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



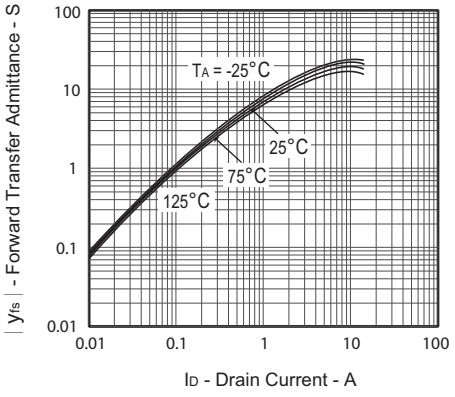
FORWARD TRANSFER CHARACTERISTICS



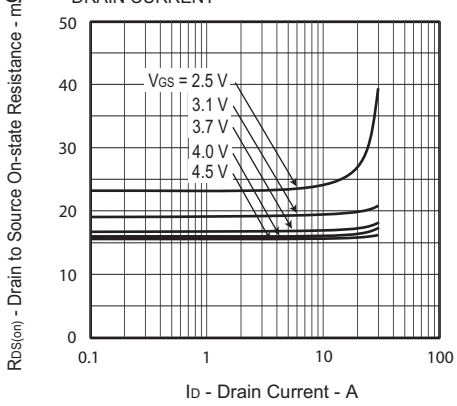
GATEBTO SOURE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



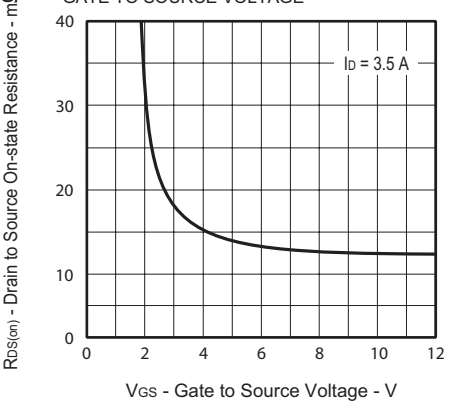
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



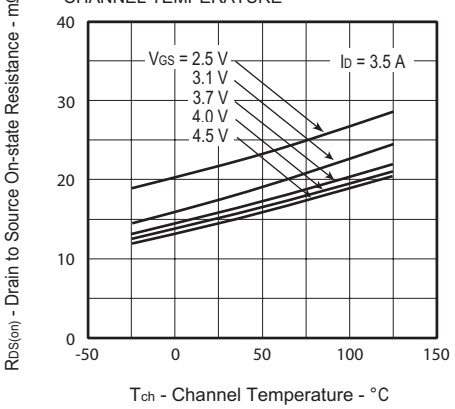
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



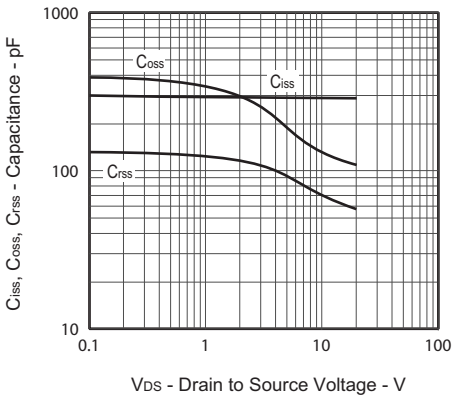
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



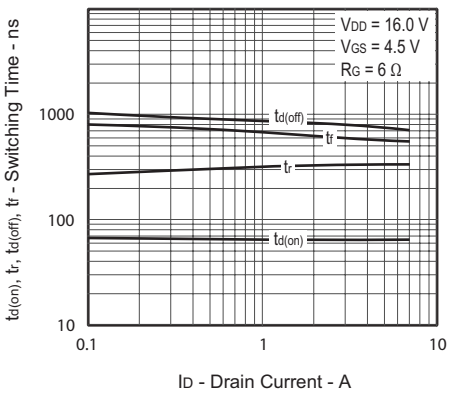
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



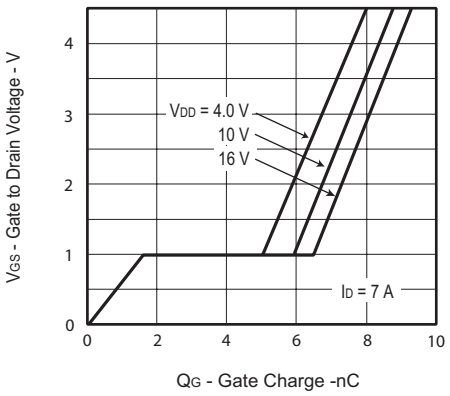
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



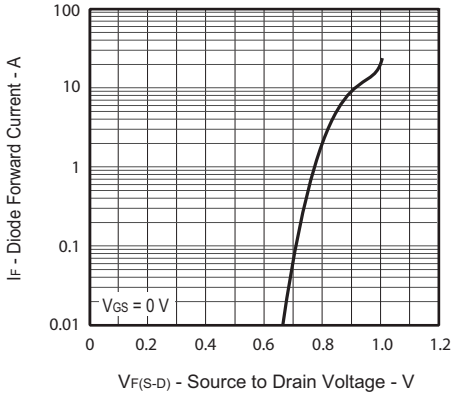
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS

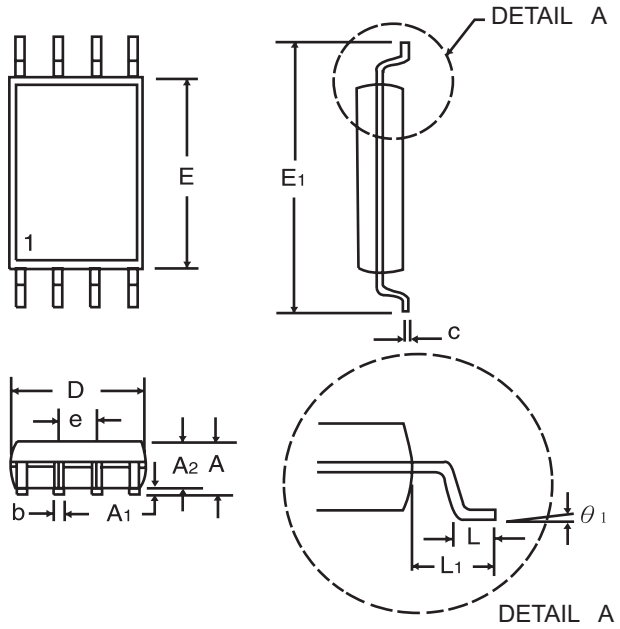


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



PACKAGE OUTLINE DIMENSIONS

TSSOP-8

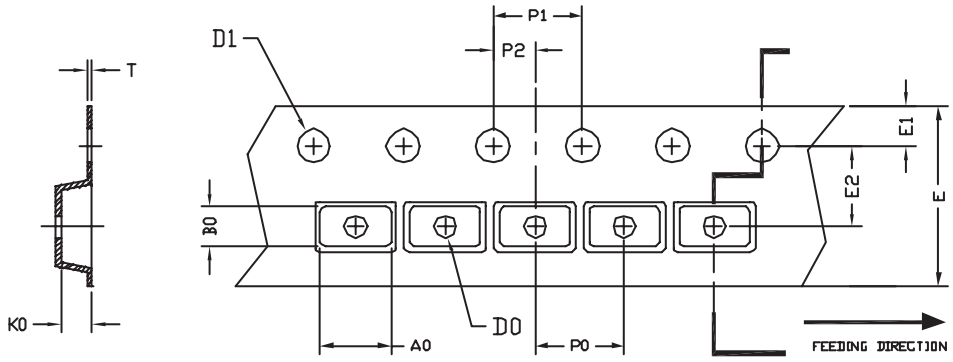


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	1.20	0.033	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.127		0.005	
D	2.90	3.10 ②	0.114	0.122 ②
E	4.30	4.50 ③	0.169	0.177 ③
E1	6.20	6.60	0.244	0.260
e	0.65BSC		0.025BSC	
L	0.50	0.70	0.020	0.028
L1	1.00		0.039	
θ_1	0°	8°	0°	8°

Notes:
1. This drawing is for general information only.Refer to JEDEC Drawing MO-153,Variation AA,for proper dimensions,tolerances,datums,etc.
2. Dimension D does not include mold Flash,protrusions or gate burrs.Mold Flash,protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E does not include inter-lead Flash or protrusions.Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion.Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition.Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E to be determined at Datum Plane H.

TSSOP-8 Tape and Reel Data

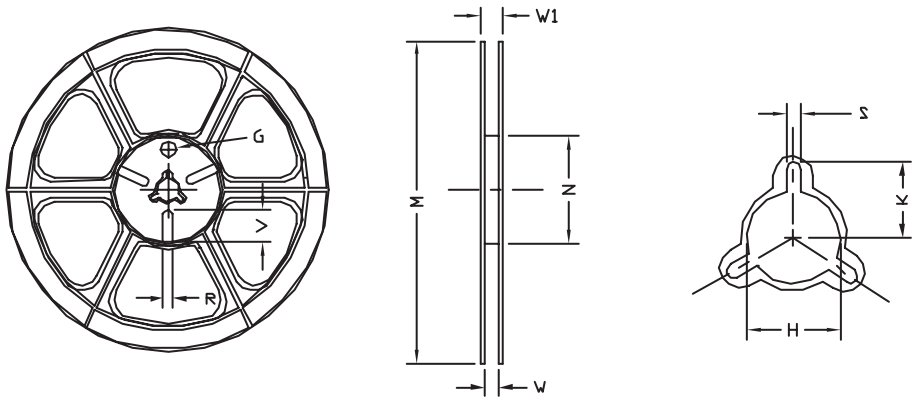
TSSOP-8 Carrier Tape



UNIT : mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TSSOP 8	6.08	4.40	1.60	ϕ 1.50 + 0.1 - 0.0	ϕ 1.50 + 0.1 - 0.0	12.00 ± 0.3	1.75	5.50 ± 0.05	8.00	4.00	2.00 ±0.05	0.30 ±0.05

TSSOP-8 Reel



UNIT : mm

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ϕ 330	330	100	12.5	16.0	ϕ 13.0 + 0.5 - 0.2	10.6	2.0 ±0.5	---	---	---