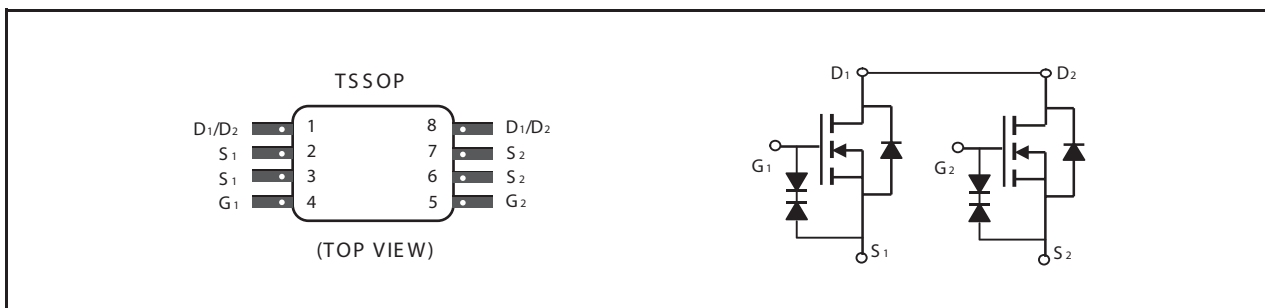


**Dual N-Channel Enhancement Mode Field Effect Transistor**

PRODUCT SUMMARY		
VDSS	ID	RDS(ON) (mΩ) Max
20V	7A	20 @ VGS=4.0V
		27 @ VGS=2.5V

FEATURES

- Super high dense cell design for low RDS(ON).
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.

**ABSOLUTE MAXIMUM RATINGS** ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Limit	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current-Continuous ^a	$T_A=25^{\circ}\text{C}$	7
		$T_A=70^{\circ}\text{C}$	5.6
I_{DM}	-Pulsed ^b	28	A
P_D	Maximum Power Dissipation ^a	$T_A=25^{\circ}\text{C}$	1.5
		$T_A=70^{\circ}\text{C}$	1
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	Limit	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ^a	85	$^{\circ}\text{C/W}$

STG8820

Ver 1.1

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =16V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±12V, V _{DS} =0V			±10	μA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.5	0.8	1.5	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =4V, I _D =7A		17	20	m ohm
		V _{GS} =2.5V, I _D =6A		20	27	m ohm
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =7A		23		S
DYNAMIC CHARACTERISTICS ^c						
C _{ISS}	Input Capacitance	V _{DS} =10V, V _{GS} =0V f=1.0MHz		470		pF
C _{OSS}	Output Capacitance			164		pF
C _{RSS}	Reverse Transfer Capacitance			142		pF
SWITCHING CHARACTERISTICS ^c						
t _{D(ON)}	Turn-On Delay Time	V _{DD} =10V I _D =1A V _{GS} =4V R _{GEN} =10 ohm		17		ns
t _r	Rise Time			54		ns
t _{D(OFF)}	Turn-Off Delay Time			63		ns
t _f	Fall Time			45		ns
Q _g	Total Gate Charge	V _{DS} =10V, I _D =7A, V _{GS} =4V		10		nC
Q _{gs}	Gate-Source Charge			2.1		nC
Q _{gd}	Gate-Drain Charge			4.5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Diode Forward Current				2.0	A
V _{SD}	Diode Forward Voltage ^b	V _{GS} =0V, I _S =2.0A		0.79	1.2	V

Notes

- a. Surface Mounted on FR4 Board, t ≤ 10sec.
 b. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
 c. Guaranteed by design, not subject to production testing.

Mar, 29, 2010

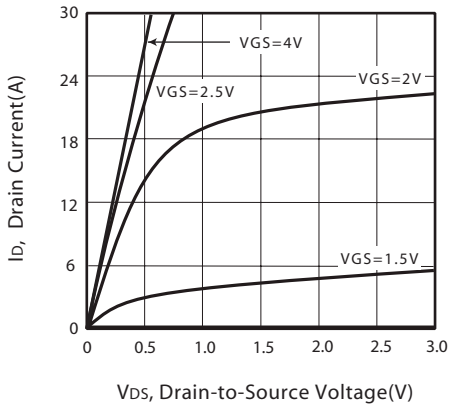


Figure 1. Output Characteristics

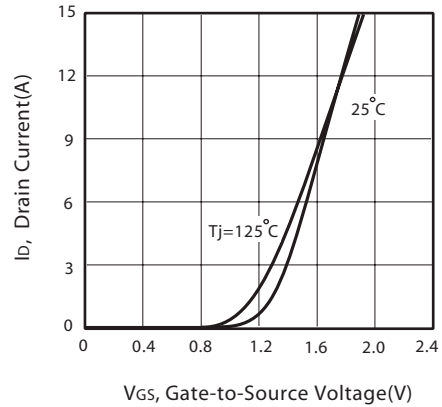


Figure 2. Transfer Characteristics

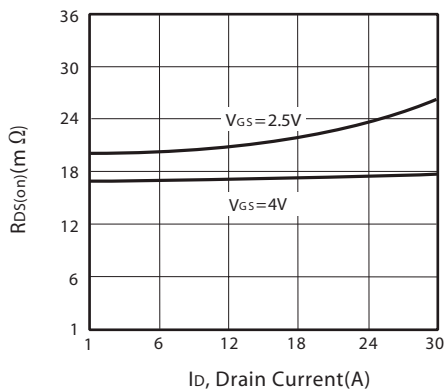


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

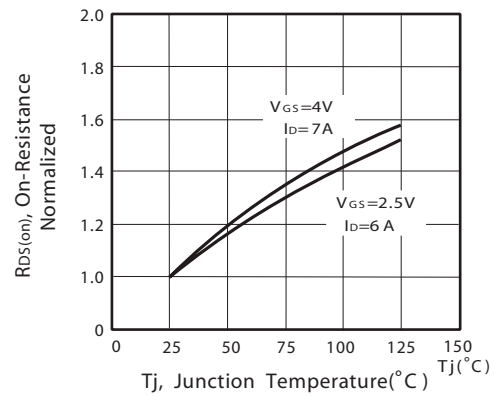


Figure 4. On-Resistance Variation with Drain Current and Temperature

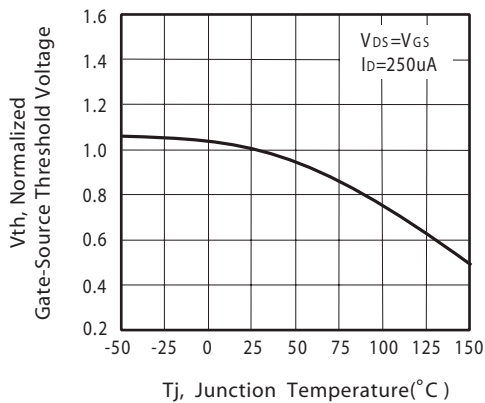


Figure 5. Gate Threshold Variation with Temperature

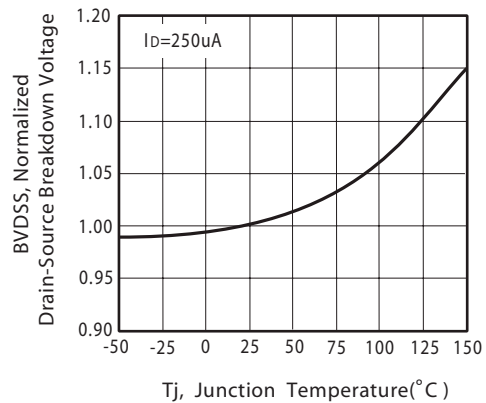


Figure 6. Breakdown Voltage Variation with Temperature

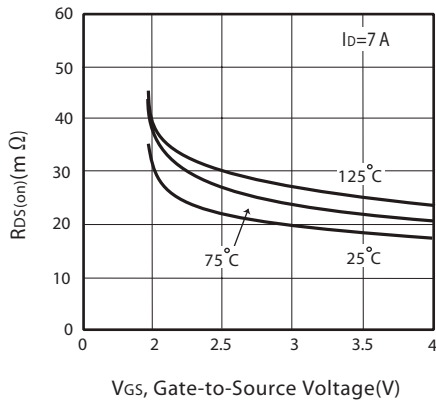


Figure 7. On-Resistance vs. Gate-Source Voltage

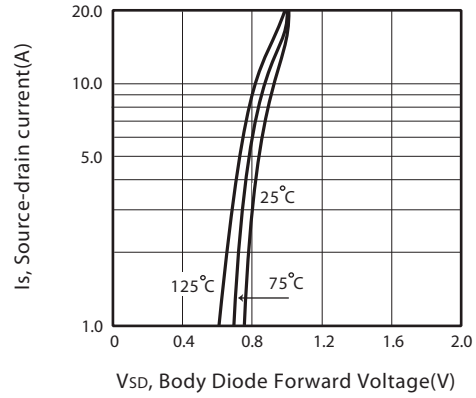


Figure 8. Body Diode Forward Voltage Variation with Source Current

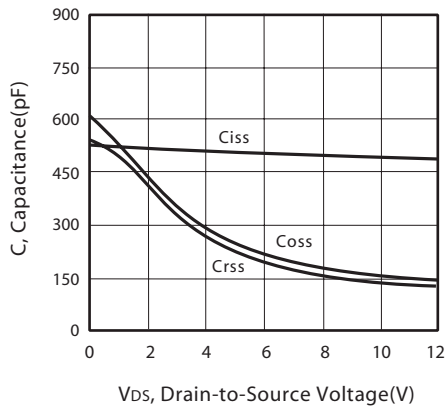


Figure 9. Capacitance

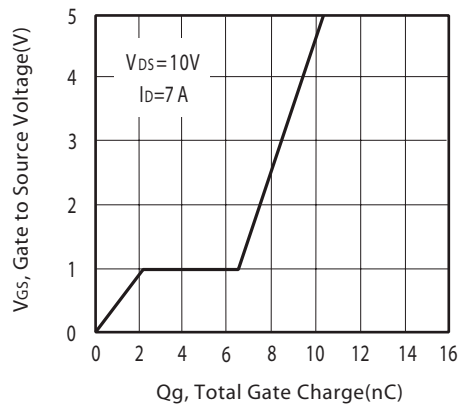


Figure 10. Gate Charge

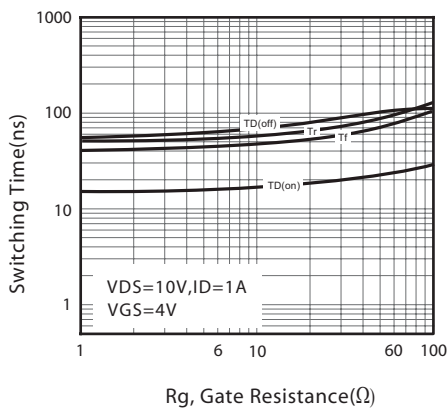


Figure 11. switching characteristics

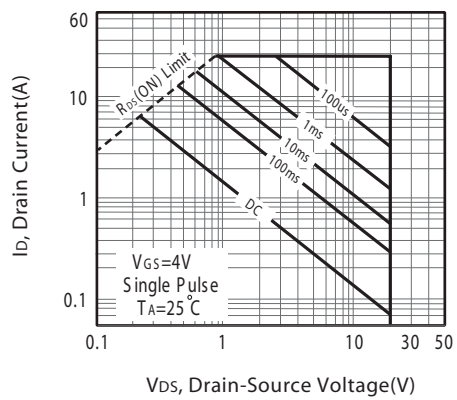


Figure 12. Maximum Safe Operating Area

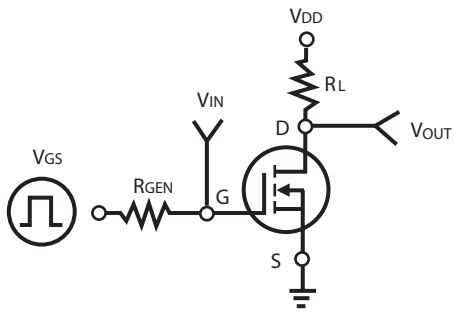


Figure 13. Switching Test Circuit

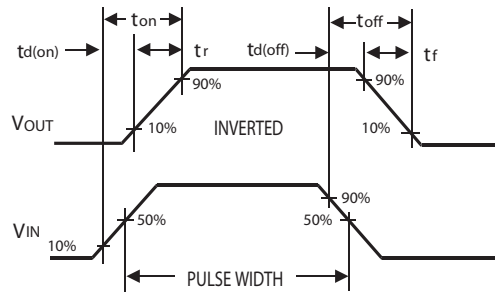
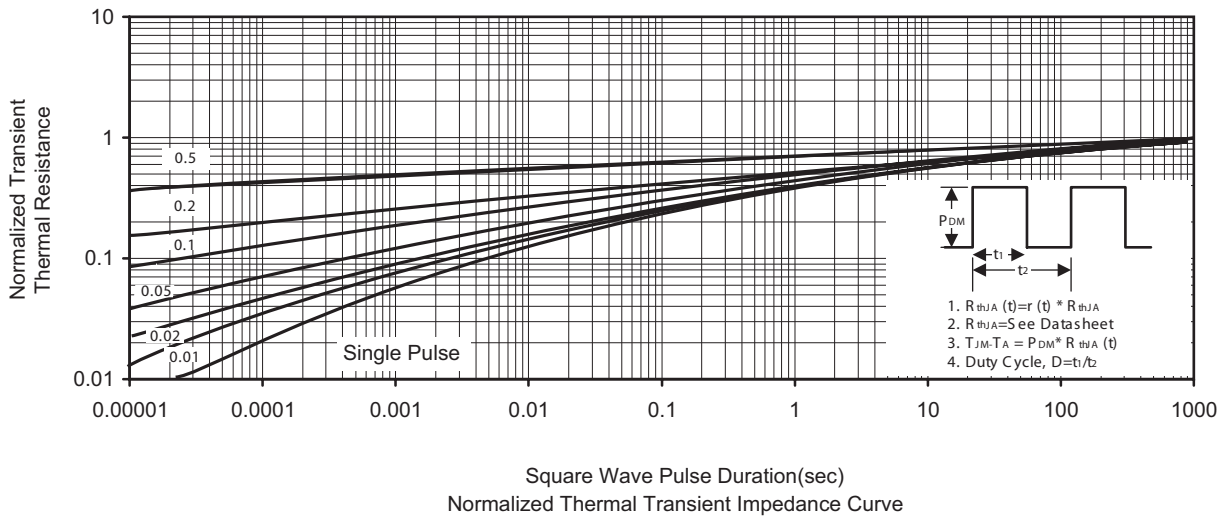


Figure 14. Switching Waveforms



PACKAGE OUTLINE DIMENSIONS

TSSOP-8

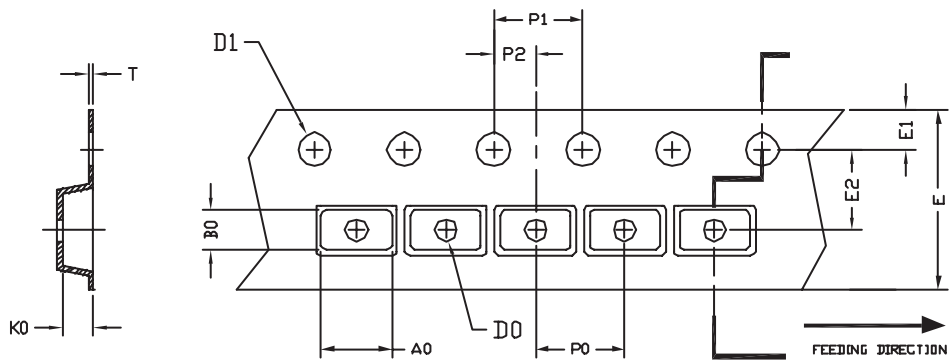
The drawing includes a top view showing a rectangular package with eight leads, a side view showing the lead profile, and a detailed view of the lead tip. Dimensions are labeled as follows: A (lead thickness), A1 (lead thickness at the base), A2 (lead thickness at the base), b (lead width), c (lead thickness at the base), D (package width), E (package height), E1 (lead height), e (lead pitch), L (lead length), L1 (lead length at the base), and θ_1 (lead angle).

SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	1.20	0.033	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.127		0.005	
D	2.90	3.10 [Ⓢ]	0.114	0.122 [Ⓢ]
E	4.30	4.50 [Ⓢ]	0.169	0.177 [Ⓢ]
E1	6.20	6.60	0.244	0.260
e	0.65BSC		0.025BSC	
L	0.50	0.70	0.020	0.028
L1	1.00		0.039	
θ_1	0°	8°	0°	8°

Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
 2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
 3. Dimension E does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010 in) per side.
 4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
 5. Dimension D and E to be determined at Datum Plane H.

TSSOP-8 Tape and Reel Data

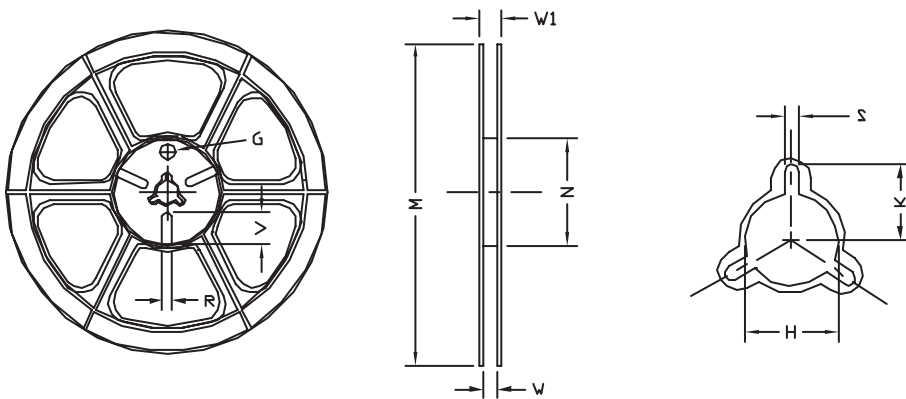
TSSOP-8 Carrier Tape



UNIT : mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TSSOP 8	6.08	4.40	1.60	$\phi 1.50$ +0.1 -0.0	$\phi 1.50$ +0.1 -0.0	12.00 ± 0.3	1.75	5.50 ± 0.05	8.00	4.00	2.00 ± 0.05	0.30 ± 0.05

TSSOP-8 Reel



UNIT : mm

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	$\phi 330$	330	100	12.5	16.0	$\phi 13.0$ +0.5 -0.2	10.6	2.0 ± 0.5	---	---	---